Power Reduction Techniques In VLSI Using 8x10 Encoder & 10x8 Decoder Without Ripple Counter

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Abstract-*In today's time the VLSI industry is growing rapidly and it demands for the devices which consume less power and there is no impact on their performance. Maintaining the performance with less power consumption is the big task for the engineers. Therefore, the maximum time is spent on the power reduction without affecting the performance by the VLSI engineers. There are many techniques used to reduce the power consumption of the design. The design and the implementation of 8x10 encoder and 10x8 decoder. We can reduce the power consumption of hardware. Less power consumption will certainly leads to less cost of the hardware. The VLSI industry growing very rapidly with the advantages of reducing power, speed and area without modifying the given system specifications. The main task in VLSI is to reduce the power consumptions as much as possible. Power can be reduced by clock gating is one of the method to reduce the power consumption. Clock gating and to maintain the disparity is (+2 to -2) method reduce the power consumption by reducing the unwanted transitions in the applied clock signal without changing system specifications. In this paper we are used pulse triggering method and disparity of DC Balance to save the power. The communication system consists of encoder and decoder blocks along with parallel to serial and serial to parallel converter with respective.*

These techniques can also be used to reduce the clock skew problem and due to removal of clock skew power consumption can be reduced. In this we have designed the 8x10 encoder and 10x8 decoder using VHDL. The 8x10 encoder and 10x8 decoder have mainly two features due to which they are in great demand for high speed communication. First is low transmission rate and second is DC compensation. They have many applications such as PCI express, USB 3.0, gigabit Ethernet and many more.

Keywords-Xilinx; Verilog; Altera QUARTUS-II;8x10 encoder and 10x8 decoder; Pulseclock;

I. INTRODUCTION

The VLSI engineers offer extra emphasis at the assets utilized by the hardware. They try difficult to reduce the consumption of assets which ends up in the growth of the VLSI enterprise. The important aid comes into position is strength. Less electricity consumption will virtually leads to much less fee of the hardware. Lot of studies is going on reduction of power ate up with the aid of the hardware.

There are many strategies that are used to reduce the strength such as clock gating and clock divider etc These strategies also can be used to reduce the clock skew hassle and due to removal of clock skew electricity intake can be decreased. USB 3.0 adds the brand new transfer rate called Super Speed USB (SS) that could transfer facts at up to 5 Gbit/s (625 MB/s), which is about ten instances as rapid as the USB 2.0 popular. Manufacturers are recommended to distinguish USB 3.0 connectors from their USB 2.0 opposite numbers by means of blue color-coding of the Standard-A receptacles and plugs, and through the initials SS. In USB 3.0, twin-bus architecture is used to permit both USB 2.Zero (Full Speed, Low Speed, or High Speed) and USB three.0 (Super Speed) operations to take place concurrently, as a consequence presenting backward compatibility. Connections are such that they also permit ahead compatibility, this is, running USB 3.0 gadgets on USB 2.0 ports. The structural topology is the equal, together with a tiered big name topology with a root hub at level zero and hubs at decrease tiers to provide bus connectivity to devices In this paper, we have designed the 8x10 encoder and 10x8 decoder the use of Verilog HDL. The encoder and decoder is applied with 3-bit down ripple counter to improve the clock skew which truly ends in much less energy consumption of encoder and decoder. The 8x10 encoder and 10x8 decoder have specially functions due to which they're in extremely good call for for high speed verbal exchange. First is low transmission price and second is DC repayment . They have many applications together with PCI specific, USB three.0, gigabit ethernet and many extra.

II. ARCHITECTURE

In this paper, we implemented 3-bit down ripple counter that's one of the techniques to reduce the clock skew trouble. By reducing the clock skew we can capable of reduce the power intake of the hardware. We applied this ripple counter with the encoder and decoder layout using verilog HDL. There are many methods to put in force the ripple counter relying at the traits of the flip flops used and the necessities of the rely sequence. The running of encoder,

decoder and ripple counter design is illustrated later on this section.

The clock ports of the encoder and decoder block are driven via the output of the closing turn-flop of the 3-bit ripple counter. By using ripple counter the consumed electricity of encoder is reduced. The connection between the encoder and ripple counter block is more recognize by using the RTL view shown in Fig.1 and the relationship among the decoder and ripple counter block is proven by the RTL view in Fig.1

III. DEVELOPMENTS

The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as small-scale integration (SSI), improvements in technique led to devices with hundreds of logic gates, known as medium-scale integration (MSI). Further improvements led to large-scale integration (LSI), i.e. systems with at least a thousand logic gates.

Current technology has moved far past this mark and today's microprocessors have many millions of gates and billions of individual transistors.one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like ultra-large-scale integration (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinctions moot. Terms suggesting greater than VLSI levels of integration are no longer in widespread use.

In 2008, billion-transistor processors became commercially available. This became more commonplace as semiconductor fabrication advanced from the then-current generation of 65 nm processes. Current designs, unlike the earliest devices, use extensive design automation and automated logic synthesis to lay out the transistors, enabling higher levels of complexity in the resulting logic functionality. Certain high-performance logic blocks like the SRAM (static random-access memory) cell, are still designed by hand to ensure the highest efficiency.

Ripple Counter

A ripple counter is an asynchronous counter in which simplest the primary turn-flop is clocked by means of an outside clock. All next turn-flops are clocked by way of the output of the previous flip-flop. Asynchronous counters are also called ripple-counters because of the manner the clock pulse ripples it way through the flip-flopsIn the ripple counter layout, the succeeding turn flop clock port is pushed via the previous flip flop output port as shown in Fig.1. The clock skew is decreased by using this due to the fact the turn flops don't toggle at the same clock. The first flip flop is clocked at the high quality fringe of the CLK signal and the second one and the 1/3 level flip flops are clocked at the wonderful edge of the output of the previous flip flop

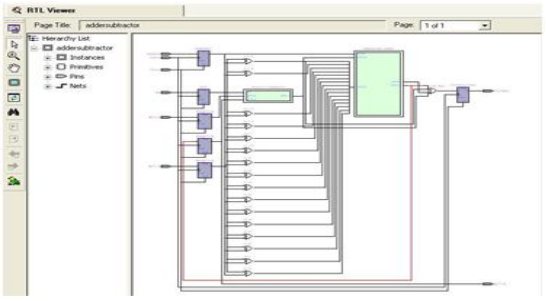


Fig:RTL Semantic Ripple Counter

IV. LITERATURE SURVEY

In today's time the VLSI industry is growing rapidly and it demands for the devices which consume less power and there is no impact on their performance. Maintaining the performance with less power consumption is the big task for the engineers. Therefore, the maximum time is spent on the power reduction without affecting the performance by the VLSI engineers. There are many techniques used to reduce the power consumption of the design. Less power consumption will certainly leads to less cost of the hardware. Lot of research is going on reduction of power consumed by the hardware.Clock Gating is a technique used for reduction of power in the digital design by clock net. In clock gating technique the clock is disabled at the situation where it is not necessary, thus this reduces the power consumption. Clock gating simply switch off the clock where it is unnecessarily consumes power. By doing this the power consumption is less without affecting the performance of the design. There are various techniques used for clock gating as: NAND gate, AND gate, latch based AND/NOR gate clock gating, multiplexer based clock gating. The latest technique for clock gating generation is using of negative/positive latch. There are many techniques which are used to reduce the power such as clock gating and clock divider etc these techniques can also be used to reduce the clock skew problem and due to removal of clock skew power consumption can be reduced. In this paper, we have designed the 8x10 encoder and 10x8 decoder using Verilog HDL. The encoder and decoder is implemented with 3-bit ripple counter to improve the clock skew which certainly

leads to less power consumption of encoder and decoder. The 8x10 encoder and 10x8 decoder have mainly two features due to which they are in great demand for high speed communication. First is low transmission rate and second is DC compensation. They have many applications such as PCI express, USB 3.0, gigabit Ethernet and many more.

The 8b/10b coding scheme was initially proposed by Albert X. Widmer and Peter A. Franaszek of IBM Corporation in 1983. This coding scheme is used for high-speed serial data transmission. The encoder on the transmitter side maps the 8-bit parallel data input to 10-bit output. This 10-bit output is then loaded in and shifted out through a high-speed Serializer (Parallel-in Serial-out 10-bit Shift Register). The serial data stream will be transmitted through the transmission media to the receiver. The high-speed Deserializer (Serial-in Parallel-out 10-bit Shift Register) on the receiver side converts the received serial data stream from serial to parallel. The decoder will then remap the 10-bit data back to the original 8-bit data. When the 8b/10b coding scheme is employed, the serial data stream is DC-balanced and has a maximum run-length without transitions of 5. These characteristics aid in the recovery of the clock and data at the receiver. Figure 3.2 shows the 8b/10b encoder/decoder usage in a communication system.

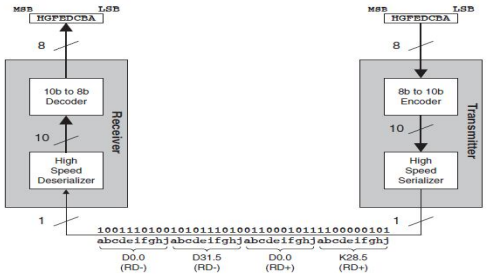


Fig 4.2: The 8b/10b Encoder/Decoder in a System.

4.2.1 DC Balance and Run Length:

A DC-balanced serial data stream means that it has the same number of 0s and 1s for a given length of data stream. DC-balance is important for certain media as it avoids a charge being built up in the media. The run-length is defined as the maximum numbers of contiguous 0s or 1s in the serial data stream. A small run length data stream provides data transitions within a small length of data. Data transitions are essential for clock recovery. The PLL of the CDR generates a phase-adjustable output clock from the reference clock input. Transitions on the serial data stream provide the transmission clock phase information to the PLL and allow the PLL to recover the transmission clock with the correct phase. Note that the reference clock input is always necessary for the CDR. The serial data stream embeds the phase of the transmission clock, not the clock itself. This reference clock comes from the receiver system, not the transmitter system.

4.3 8B/10B CODE MAPPING:

The 8b/10b encoder converts 8-bit code groups into 10-bit codes. The code groups include 256 data characters named Dx.y and 12 control characters named Kx.y.

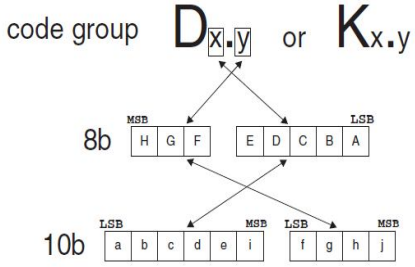


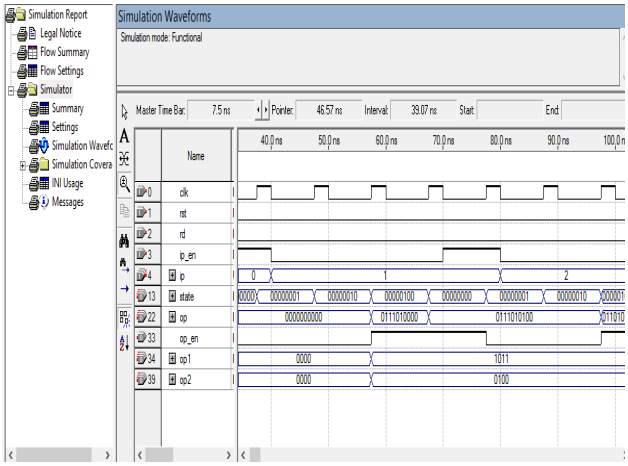
Fig 4.3: The 8b/10b Coding Scheme

The coding scheme breaks the original 8-bit data into two blocks, 3 most significant bits (y) and 5 least significant bits (x). From the most significant bit to the least significant bit, they are named as H, G, F and E, D, C, B, A. The 3-bit block is encoded into 4 bits named j, h, g, f. The 5-bit block is encoded into 6 bits named i, e, d, c, b, a. As seen in Figure 4.3, the 4-bit and 6-bit blocks are then combined into a 10-bit encoded value.

Simulation Result

The 8x10 encoder, 10x8decoder and ripple counter circuit are implemented using verilog HDL and stimulated on ModelSim 10.3c. The RTL and the technology view of the encoder with ripple counter and decoder with ripple counter is done in Quartus II software . Fig-2: Demonstrations the stimulation waveforms of the 3bit down ripple counter Fig-3: Stimulation Output of 3-bit Down Ripple counter The 8x10 encoder with ripple counter circuit is shown in Figs.4. In these figures the encoder clock port is driven by the output of the ripple counter

5.2.1 8b/10b encoder:



5.2.2 RTL schematic for encoder:

The 10x8 decoder with ripple counter circuit is shown in Figs.6, 7, 8. In these figures the decoder clock port is driven by the output of the ripple counter

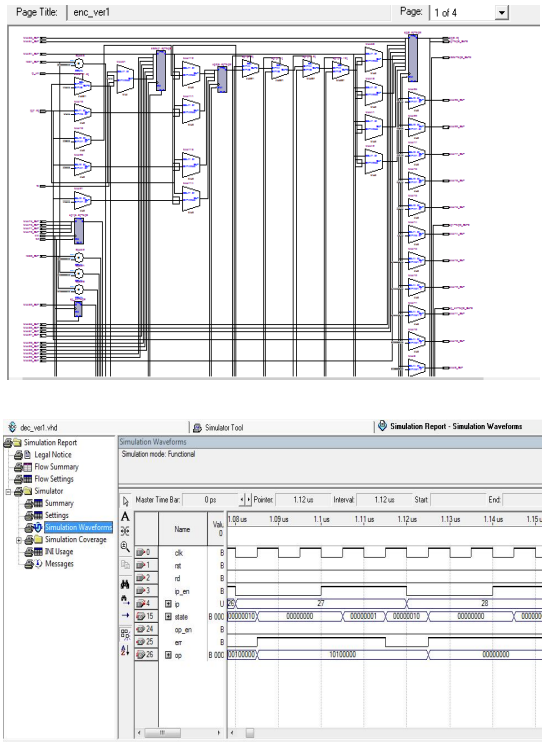


Fig 5.3: Decoder Simulation

V. CONCLUTION

In this paper we can reduce the power consumption of 8x10 encoder and 10x8 decoder. The encoder & decoder circuit consumes less power and also avoids the problem of clock skew and jitter problems by the method of clock gating and disparity (+2 to -2). The 8x10 encoder and 10x8 decoder are verified using FPGA and CAN in Quartus II version 9.1. These powers are calculated by using VHDL power analyser of Quartus II 9.1sp2. It improve the transmission characteristics of information to be transferred Coding Gain. The transitions in the PHY bit stream to make clock recovery possible at the receiver. It give special code-groups for easy analyze bit pattern which assists a receiver for USB 3.0 applications. In this paper among the 10bits data we are using only 8bits data and remaining 2 bits are used as a clock. And we can also implement the 64x66 encoder/decoder and 128x130 encoder/decoder.

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