Analysis and Design of Multi level Inverter: A Review

Anand Kumar Joshi[1], Devendra Dohre[2], Silpi Sisodia[3]
Department of Electrical Engineering
[1, 2, 3]MPCT Gwalior India

Abstract-*The multi-level technique is most acceptable technologies used in recently inverters, due to improvement of Total Harmonic distortion profile and use of higher magnitude voltage. These Multi level Inverter technologies Produces highly smooth approximately sine wave. This paper Present analysis of various types of Multi level Inverter Technology and one of a kind firing strategies as 1. Flying capacitor multilevel inverter 2. Cascaded multilevel inverter 3. Neutral point clamped inverter topology (NPC inverter)*

Keywords-Multilevel inverters, asymmetric and symmetric voltage source configuration, CHB, THD, phase shift pulse width modulation, MLI, PWM, sinusoidal pulse width modulation, hybrid topologies, phase opposition disposition.

I. INTRODUCTION

Recently increasing demand of electrical power, dependency increased on Renewal energy source as photovoltaic solar power, wind energy, Solar Thermal. Mostly used technology is photovoltaic solar produces DC voltage is convert the power into AC, this AC power fed into grid or compatible load. This conversion of power forced to research on Multi level inverter techniques, Multi-level technology is invented due to some advantage over the typical two level inverter as

1. possibility to direct connectivity of energy electronics switch to high voltage and medium voltage(2.3,3.3, 4.16, or 6.9 kV),
2. Highly smooth current without using any external filter.
3. Lower whole harmonics distortion profile,
4. Improvement of EMI Profile etc.

The term presented multilevel initial with the 3-level inverter [4]. thru increasing the variety of voltage levels inside the inverter, the o/p voltages have greater steps producing a staircase waveform, which has a discounted harmonic distortion.

The term presented multilevel initial with the 3-level inverter [4]. Thru rise the no. of voltage level in the inverter, the o/p voltages have additional stagegenerating a staircase waveform, that has a lessen harmonic distortion, Multi-level Inverter (MLI) is accept extra attention in industrial usage, etc As a outcome, the inverter output voltages have lessen harmonic distortions and high quality of waveform, MLI receive high DC voltage through addition phenomena from different DC voltage source, these DC voltage source can be used as symmetrically and asymmetrically, Asymmetric voltage is most preferred because of using less no. of DC voltage produces highest no. of voltages level main disadvantage of the MLI technique are

1. Increases number of power electronics switch also increases it Gate driver circuitry so that device cost increases
2. Increases Switching losses
3. System complex because of upper no. of power electronics switches
4. production of common-mode voltages

A number of multilevel inverter topologies have been invented during the last decades, major MLI topologies are cascaded H-bridges inverter (CHB) with divide dc sources, flying capacitors (capacitor clamped) and diode clamped (neutral l clamped). These topologies have several own advantage and disadvantage, cascaded High-bridges inverter is preferred.

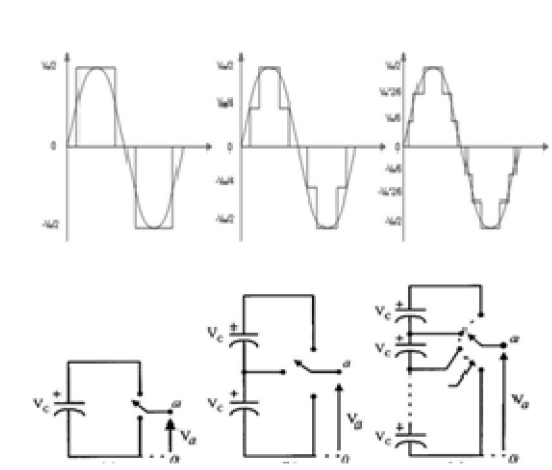


Fig.1 single phase of an inverter with (a) 2-levels, (b) 3-levels, and (c)nlevels.

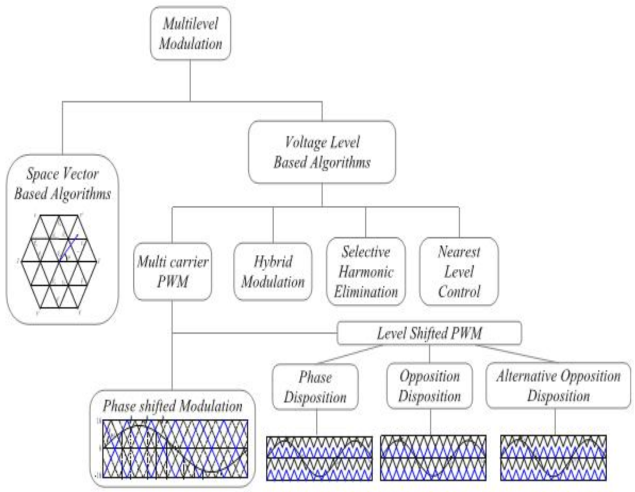


Fig.2 multilevel modulation and its types

II. DIODE-CLAMP MULTILEVEL CONVERTER

In this circuit, the dc-bus voltage is break up into 5 stage through four collection-related bulk capacitors, and the center point of the 4 capacitors can be defined due the impartial point.The o/p voltage has 5 voltage stage: Vdc/2,Vdc/4, 0, - Vdc/2, Vdc/4, for voltage stage Vdc/2 for Switch S1, S2, S3, S4, Necessity to be turned on and - Vdc/2 switch for S1, S2, S3, S4necessity to be turned on . The voltage throughout each capacitor is Vdc/4 and all tool voltage stress might be constrained to a capacitor voltage stage Vdc/4 thru clamping diodes.

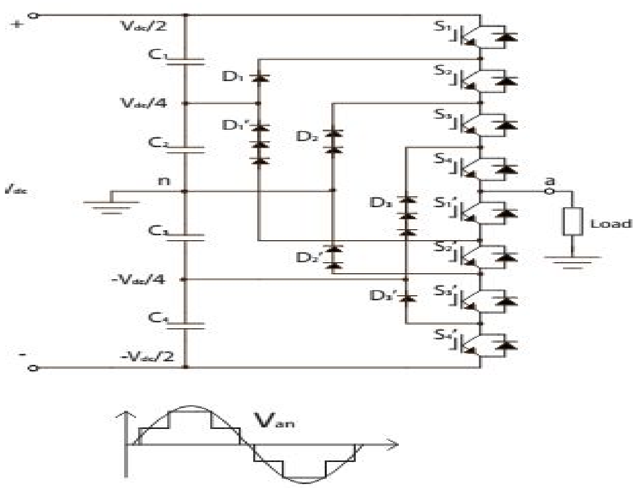


Fig. 3. Diode-clamped multilevel inverter circuit topologies of 5-level.

To provide an explanation for how the stair voltage is synthesized, the neutral factor n is taken into consideration because the o/p phases voltage reference point. There are certain switch mixtures to synthesize 5 stage voltages across a and n. Which provide an explanation for shown below in table.

Switch stats for five level capacitor clamped inverter, “1” means turned on and “0” means turn off switches

Output voltage	S_1	S_2	S_3	S_4	S_1 ‘	S_2 ‘	S_3 ‘	S_4 ‘
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/2$	0	0	0	1	1	1	1	0
$-V_{dc}/4$	0	0	0	0	1	1	1	1

Advantages:

a. When the no. of voltage phase is highest sufficient, whole harmonic content will be lowest sufficient to avoid the utilize for filters.
b. Working Efficiency is high because all working tool are switched at the major frequency
c. Reactive energy flow can be control thru technique.
d. The control technique is essay for a back-to-back system.

Difficulties

a. Highest no. of clamping diodes is essential when the no. of phase is highest.
b. It’sproblematicto do actualenergyflow control for th

III. MULTILEVEL CONVERTER USING FLYING-CAPACIT

The voltage synthesis in a 5-stage capacitor-clamped converter has further flexibility than a diode-clamped converter. Exploiting Fig. 3(b) as the instance, the voltage of the 5-level phase-leg a o/p with respect to the neutral point n , can be synthesized thru the subsequent switch groupings. : Vdc/2, Vdc/4, 0, - Vdc/2, Vdc/4, For voltage phaseVdc/2 switches necessity to turned on as S1, S2 ‘, S3’, S4’and - Vdc/2 switch for S1, S2, S3, S4necessity to be turned on.

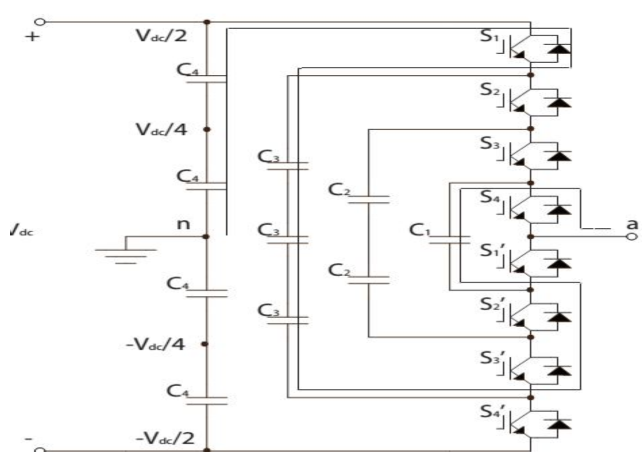


Fig. 4. Capacitor-clamped multilevel inverter circuit topologies of five-level.

Presented in parent utilize the crucial constructing block of capacitor clamp, the circuit has been called the flying capacitor inverter. The inverter in illustrate in figure generate5 voltage stagethat as Switch initial for 5 level capacitor clamped inverter, “1” means turned on and “0” means turn off switches

Output voltage	S_1	S_2	S_3	S_4	S_1 ‘	S_2 ‘	S_3 ‘	S_4 ‘
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-V_{dc}/2$	1	0	0	0	1	1	1	0
$-V_{dc}/4$	0	0	0	0	1	1	1	1

In the preceding rationalization, the capacitors with high-quality signs and symptoms are in discharging mode, even as those with terrible sign are in charging mode. By proper selection of capacitorcombinations, it is possible to balance the capacitor charge. Similar to diode clamping, the capacitor clamping necessitates ahugeno. of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch

Advantages:

a. Largest no. of storage capacitors gives additional ride thru capabilities during power o/p.
b. Provides switch combination redundancy for balancing different voltage levels.
c. When the no. of levels is higher, total harmonic content will be lowest enough to avoid the use for filters.
d. Both reactive and actual energy flow can be controlled, creating a possible voltage source converter candidate for highest voltage dc transmission.

Disadvantage

a. Highest no. of storage capacitors is necessary when the no. of converter voltage stages is highest. Highest-voltage stages systems are more problematic to package and much costly with the necessary bulky capacitors.
b. Themilti inverter control will be very complex, and the switching frequency and switching losses will be highest for actual power transmission.

IV. MULTILEVEL CONVERTER USING CASCADED-INVERTERS WITHSEPARATE DC SOURCE

Multilevel converter utilizing cascaded-inverters with separate dc source efficient to utilize in evaluation to the other two topology as there is no need of capacitor and diode to clamping and there used different asymmetric voltage source from renewal energy source as fuel cell, solar cell wind energy etc.

Higher of number of voltage degree may be carried out with the aid of adding inverter mobile, and convey easy sine wave and decrease THD ratio. One of disadvantage is highestno. of energy electronics switch use for controlling this switch use gate driver circuit due to this circuitis some place is complex .

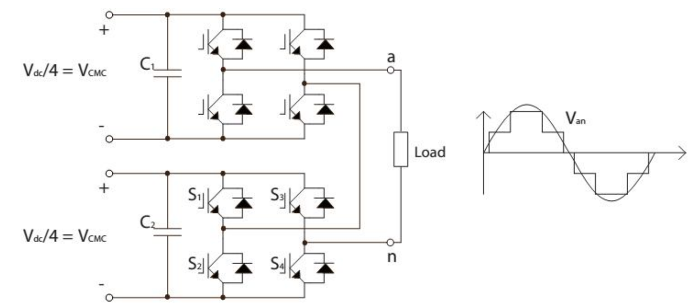


Fig. 6. Multilevel converter using Cascaded-inverters with separate dc source

Advantages:

a. Necessity the smallest no. of element among each multilevel converter to get the similar no. of voltage levels.
b. There is no need clamping diodes or voltage balancing capacitors.
c. Soft-switching can be utilized in this structure to evade bulky and loss resistor-capacitor-diode snubbed circuit.

Disadvantage

a. Needs separate dc sources for real power conversions, and so its applications are some time limited.

V. SWITCHING SCHEME

There is switching scheme divide in two methods 1. High switching scheme and 2. Fundamental switching scheme for both cases stepped o/p wave form is achieved.

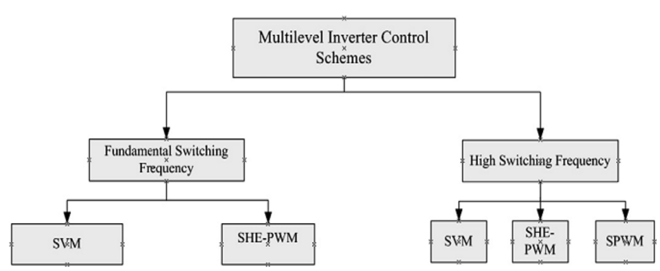


Fig. 5 Different PWM Techniques

Multi level inverter approaches utilize highest frequency carrier waves in evaluation to reference wave which generate switch gate pulses, and this modulation approach is aid to decrease entire harmonics profile

There is certain dissimilar approach in PWM as

a. Phase opposite Disposition (POD)
b. Phase disposition (PD)
c. Phaseshift (PS)
d. Phase disposition (PD)

This method presented in figure

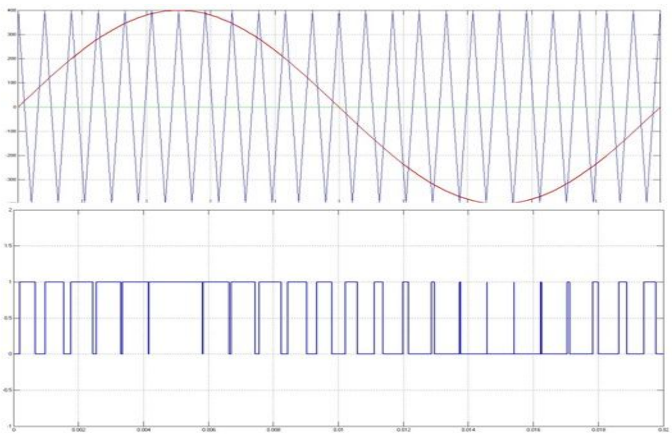
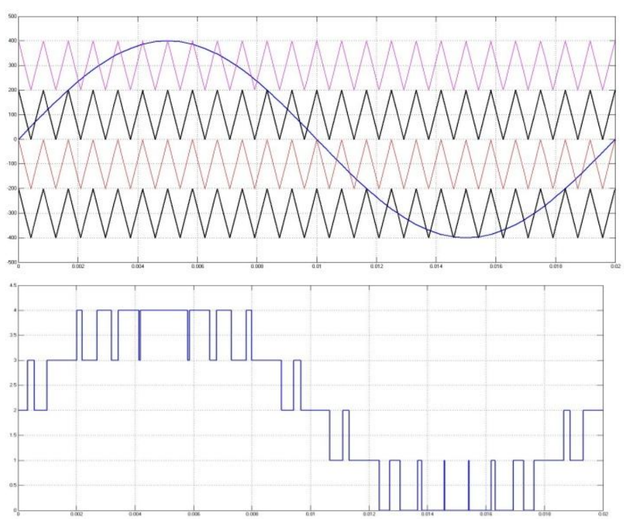


Fig.7 PWM carrier triangular and reference sinusoidal wave and pulses



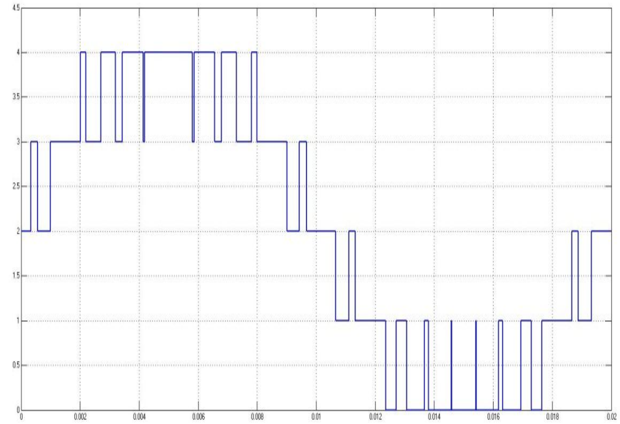


Fig 8 Phase Shift(PS)

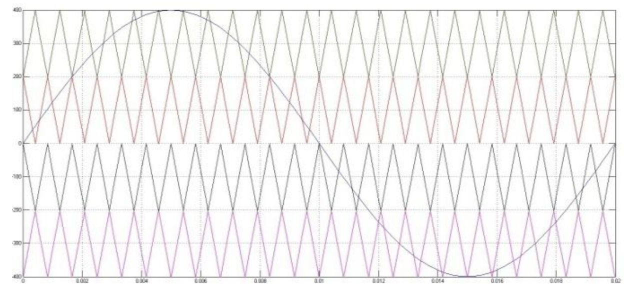


Fig 9 Alternate Phase Opposite Disposition(APOD)

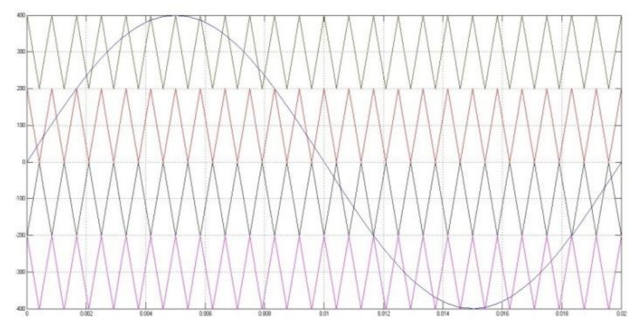


Fig 10. Phase opposite Disposition (POD)

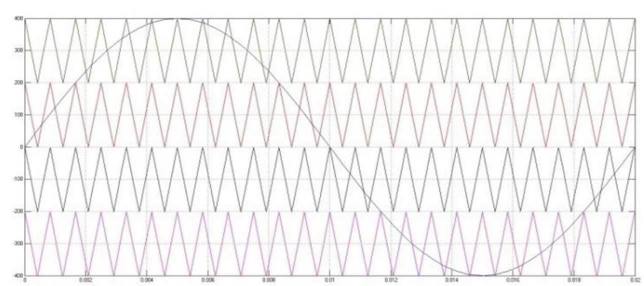


Fig 11. Phase Disposition (PD)

Applications

A. Reactive Power Compensation
B. Back-to-Back Intertie
C. Utility Compatible Adjustable Speed Drives Inverter

Inverter Configuration	Diode-Clamp	Flying-Capacitors	Cascaded inverters
Switching devices	2(m-1)	2(m-1)	2(m-1)
Main diodes	2(m-1)	2(m-1)	2(m-1)
Clamping diodes	(m-1)(m-1)	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2
Balancing capacitors	0	(m-1)(m-2)/2	0

VI. CONCLUSION

Multilevel inverters have matured from being a growing technology to a sound-established practical approached solution for low to medium voltage and high power application. The 3 foremost pronounced topology are cascaded H-bridge with separate DC source, impartial point clamp and flying capacitor. While in this paper a proposed cascaded H-bridge with a sole DC source was proposed and simulated and several hybrid multilevel inverters were also presented. Various Multilevel control strategy and application are also discussed.

REFERENCES

[1] Rodriguez J., Lai J.S., Peng F.Z.: 'Multilevel inverters: A survey of topologies, controls, and applications'. IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002

[2] Gupta, K.K.; Jain, S.; , "Topology for multilevel inverters to attain maximum number of levels from given DC sources," Power Electronics, IET , vol.5, no.4, pp.435-446, April 2012

[3] Jih-Sheng Lai , Fang ZhengPeng "Multilevel Converters-A New Breed of Power Converters" IEEE transactions on industry, VOL. 32, NO. 3, may june 1996.

[4] Malinowski, M.; Gopakumar, K.; Rodriguez, J.; Pérez, M.A.; , "A Survey on Cascaded Multilevel Inverters," Industrial Electronics, IEEE Transactions on , vol.57, no.7, pp.2197-2206, July 2010.

[5] Y. Suresh Anup Kumar Panda "Investigation on hybrid cascaded multilevel inverter with reduced dc sources" Renewable and Sustainable Energy Reviews 26 (2013) 49–59.

[6] Rodriguez J., Franquelo L.G., Kouro S., Leon, J.I., Portillo R.C., Prats M.A.M., Perez M.A.: 'Multilevel Converters: An Enabling Technology for High-Power Applications'. Proceedings of the IEEE , vol.97, no.11, pp.1786-1817, Nov. 2009.

[7] Gupta, K.K.; Jain, S "a novel multilevel inverter based on switching Dc source " IEEE transactions on industry, VOL. 61, NO. 7, July 2014.

[8] HEMA LATHA JAVVAJI, B. BASAVARAJA "Simulation & Analysis of Different Parameters of Various Levels of Cascaded H Bridge Multilevel Inverter" 2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia).

[9] "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems" IEEE Std 519-1992 (Revision of IEEE Std 519-198

[10] N.A. Rahim, J. Selvaraj*, C. Krismadinata" Five-level inverter with dual reference modulation technique for grid connected PV system" Renewable Energy 35 (2010) 712–720.

Books:

[1] Power Electronics Handbook Devices, Circuits, And Applications(Muhammad H. Rashid)