Three-Phase Inverter with Energy Buffer And DC-DC Conversion Circuits

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Abstract-*This paper proposes a new Three-phase inverter topology and describes the control method for the proposed inverter. The inverter consists of an energy buffer circuit, a dc-dc conversion circuit and an H-bridge circuit. The energy buffer circuit and H-bridge circuit enable the proposed inverter to output a multilevel voltage according to the proposed pulse width modulation (PWM) technique. The dc-dc conversion circuit can charge the buffer capacitor continuously because the dc-dc conversion control cooperates with the PWM. Simulation results confirm that the proposed inverter can reduce the voltage harmonics in the output and the dc-dc conversion current in comparison to a conventional inverter consisting of a dc-dc conversion circuit and H-bridge circuit. Experiments demonstrate that the proposed inverter can output currents of low total harmonic distortion and have higher efficiency than the conventional inverter. In addition, it is confirmed that these features of the proposed inverter contribute to the suppression of the circuit volume in spite of the increase in the number of devices in the circuit.*

Keywords-Energy buffer circuit, single-phase inverter, dc-dc conversion, pulse width modulation.

I. INTRODUCTION

Single-phase inverters are commonly used in many power applications. In recent years, single-phase inverters have been used as components of microgrid systems. In these systems, single-phase inverters are used as interfaces for renewable energy sources, such as fuel cells and photovoltaic energy, or for energy storage devices, such as batteries and ultracapacitors with the grid [1]–[7]. Various types of single-phase transformerless inverters, which have the advantages of a small size and a light weight [8], have been studied [9]–[12]. Among these, H-bridge inverters have a relatively simple structure. The H-bridge inverters,however, suffer from common-mode voltage unlike inverters such as H5 inverter, HERIC inverter and H6 inverters. In applications using batteries and ultracapacitors with output ratings of less than several hundreds of watts, the H-bridge inverter may be able to perform without the influence of the common-mode voltage. On the other hand, in applications with photovoltaic cells, the common-mode voltage causes a leakage current through parasitic capacitors between the photovoltaic cells and the ground. The leakage current degrades the performance and reliability of the inverter. However, this disadvantage can be mitigated with passive filters [13]–[15] and therefore the H-bridge inverter can be used in wide applications.

An inverter consisting of an H-bridge circuit involving a dc-dc conversion circuit can expand the voltage amplitude of the output. Therefore, this type of inverter is commonly used in applications for renewable energy sources and energy storage devices with voltages that are lower than the voltage amplitudes of the grid. The typical topologies for the dc-dc conversion are boost, and buck boost converters in addition to many other types of converters derived from these chopper topologies, including chopper inductors [16]–[18].

Inverters with an energy buffer circuit have been previously reported in [19]–[22]. An energy buffer circuit consists of switches and buffer capacitors and behaves like a charge pump circuit. Because the energy buffer circuit does not include any inductors, it can be designed with a compact form. The operation of the circuit allows the inverter to step up its dc link voltage with the help of the voltage across the buffer capacitors. Furthermore, it allows the inverter to yield a multilevel output voltage. It is well known that in multilevel inverters, the output voltage can reduce ripple in the output current, resulting in a lower output filter inductance [23]–[32]. Although the multilevel inverters have more output voltage vectors than the inverter with an energy buffer circuit, they generally cannot expand the voltage amplitude of the output.

However, inverters with only an energy buffer circuit have difficulty regulating the voltage of the buffer capacitor because the capacitor can be charged only when the inverter outputs a low voltage [20], [21]. Therefore, inverters containing both an energy buffer circuit and a dc-dc conversion circuit have been proposed [33], [34]. The variation in the energy of the buffer capacitor can be compensated for by the dc-dc conversion circuit. The multilevel energy buffer (MEB) inverter, which consists of the same circuit combination, has been proposed as part of the MEB micro-inverter in [33] and has been reported to have high efficiency and to allow a small filter inductance.

This paper proposes a new Three-phase inverter topology with an energy buffer circuit, a dc-dc conversion circuit, and an H-bridge circuit. It has different configuration from the MEB inverter in particular, in terms of connection of the dc-dc conversion circuit. The most important thing is that the difference brings the following strong advantages over the MEB inverter to the proposed inverter: Although the dc-dc conversion circuit in the MEB inverter cannot charge or discharge the buffer capacitor during the step-up operation because of the circuit configuration, the dc-dc conversion circuit in the proposed inverter can continuously charge of discharge it regardless of operation mode. For this reason, the voltage variation of the buffer capacitor of the proposed inverter can be suppressed (refer to Appendix A) or the capacitance of the proposed inverter can be a smaller value. Furthermore, in general, the continuous charge operation is more effective than the intermittent charge operation; therefore the proposed inverter can be operated with more effective performance than the MEB inverter.

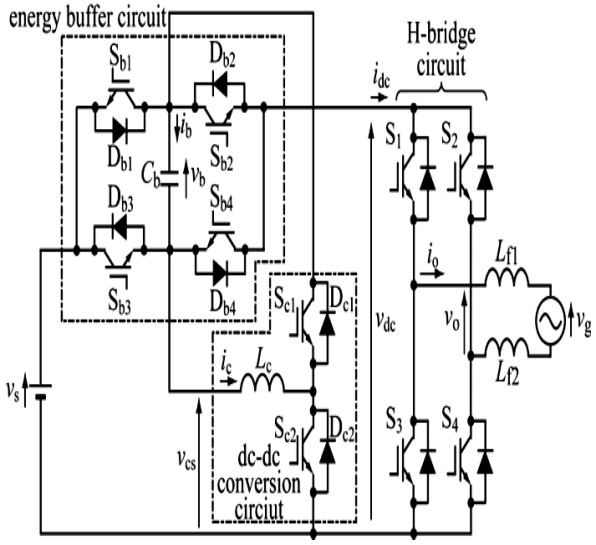

Fig.1Configuration of single-Phase inverter.

For the proposed inverter, a pulse width modulation (PWM) technique for dc-ac conversions and a control technique for the dc-dc conversion circuit are described in this paper. The energy buffer circuit and H-bridge circuit are operated according to the PWM technique and yield multilevel outputs following the voltage command signal. Control of the dc-dc conversion circuit enables the circuit to charge the buffer capacitor continuously by cooperating with the PWM Simulation results confirm that the proposed inverter can reduce the voltage harmonics in the output and the dc-dc conversion current in comparison to a conventional inverter consisting of a dc-dc conversion circuit and H-bridge circuit. Experiments demonstrate that the proposed inverter outputs a current with low total harmonic distortion (THD) and have higher efficiency than the conventional inverter. Furthermore, it is confirmed that these features contribute to the suppression of the circuit volume in spite of an increase in the number of devices.

Table I Modes Of Operation Of Energy Buffer Circuit.

	v_{dc}	Switching signals
Mode1	$v_s - v_b$	ON:Sb1and Sb4OFF :Sb2and Sb3
Mode2	v_s	ON:Sb3and Sb4OFF :Sb1and Sb2 or ON:Sb1and Sb2OFF :Sb3and Sb4
Mode3	$v_s + v_b$	ON:Sb2and Sb3OFF :Sb1and Sb4

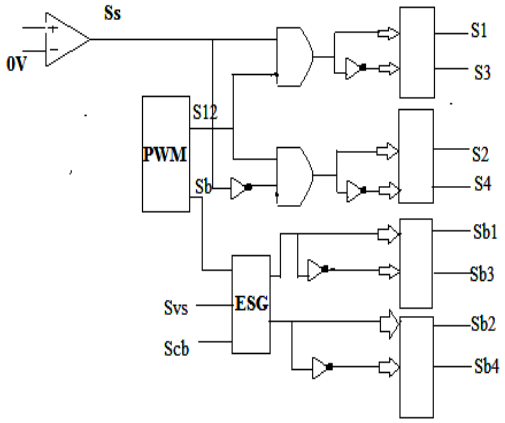

Fig.2 Block diagrams of output voltage control for dc- ac conversions.

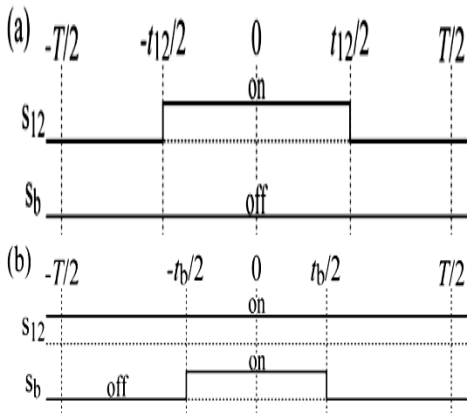

Fig.3 Signal sequences during PWM period when |voc |is in (a) Range I and (b) Range II or III.

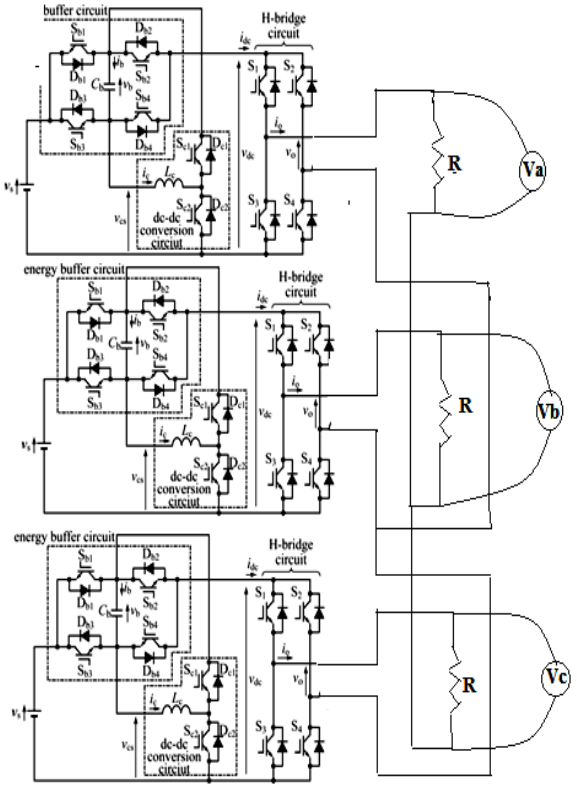

Fig.4Configuration of proposed Three-Phase inverter.

II. CIRCUIT CONFIGURATION AND CONTROL METHOD

A. Circuit configuration

Fig. 1 shows the configuration of the proposed inverter, which consists of an energy buffer circuit, a dc-dc conversion circuit, and an H-bridge circuit.. The energy buffer circuit has four switches, four diodes, and a buffer capacitor Cb. The capacitor Cb has a positive voltage vb. The energy buffer circuit positively or negatively superimposes vb on the supply voltage vs and sets the dc link voltage vdc to one of three levels depending on the state of the signals of switches Sb1 Sb4, as given by Table I. When the energy buffer circuit operates in Mode 1, it steps down the dc link voltage vdc to vs–vb. In Mode 2, the dc link voltage vdc is equal to vs. The stepped-up voltage vs+vb is provided when the energy buffer circuit operates in Mode 3. Although, in Modes 1 and 3, the energy in the buffer capacitor is changed by the dc link current idc, the dc-dc conversion circuit consisting of two switches, two diodes, and the chopper inductor Lc is operated to maintain vb at a constant level. The H-bridge circuit performs dc-ac or ac-dc conversion, cooperating with the energy buffer circuit.

B. Control for Closed loop operation

The signals are generated based on these durations, as shown in Fig. 3. Based on the energy buffer circuit signal generator (ESG), being a logic circuit, selects the appropriate mode for the energy buffer circuit, assigns corresponding states to sb13 and sb24, as given by Table II. When sb is in the on-state, the energy buffer circuit operates in Mode 2.

Using this control technique, the energy buffer circuit can generate the dc link voltage waveform conceptually shown in Fig. 5(a). While |voc| is in Range II or III, the dc link voltage vdc has a PWM waveform with levels of vs - vb, vs, and vs+vb. Conversely, while |voc| is in Range I, vdc is maintained at vs - vb. The variation of the dc level is converted to a voltage variation of the ac level by the H-bridge circuit and is formed into an approximately sinusoidal wave following as shown in Fig. 5(b). The H-bridge circuit is operated based on ss and s12. The signal ss, which express the sign of voc, is referenced to assign a polarity to the voltage with the dc level. The signal s12 is employed to convert the voltage of vs-vb to a portion of an approximately sinusoidal wave with three levels, i.e vs-vb, - vs+vb, and zero.

Input			output		Mode of energy buffer circuit
Sb	svs	scb	sb1	sb24	
0	0	0	1	0	Mode1
0	0	1	1	0	
0	1	0	0	1	Mode3
0	1	1	0	1	
1	0	0	0	0	Mode2
1	0	1	1	1	
1	1	0	0	0	
1	1	1	1	1	

Table Ii Truth Table For Esg

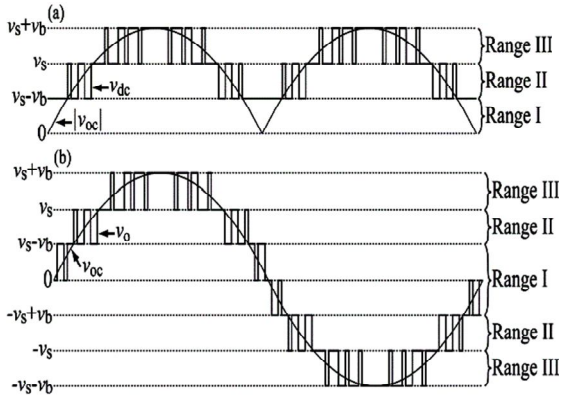

Fig. 5 Conceptual waveforms for (a) dc link voltage vdc and (b) Output voltage

C. Control for dc-dc conversion circuit

The operation of the energy buffer circuit in Modes 1 and 3 changes the capacitor voltage vb, which is controlled at a constant level by the dc-dc conversion circuit. Fig. 6 shows the modes of operation for the conversion circuit. The states of signals sc1 and sc2 for switches sc1 and sc2 in the circuit are complementary to each other. When sc1 is in the on-state, current through Lc, the path of which is depicted in Fig. 6(a), charges or discharges Cb. When sc2 is in the on-state, there are two possible current paths, depending on the states of sb1 and sb3 for the energy buffer circuit. When sb1 is in the on-state, the current flows as shown in Fig. 6(b). As a result of switching sc1 and sc2, the conversion circuit behaves either like a buck converter when Cb is charged or like a boost converter when Cb is discharged. Alternatively, when sb3 is in the on-state, the current path is illustrated in Fig. 6(c) and the conversion circuit acts like a buck-boost converter. The former behavior of the conversion circuit can more effectively regulate Vb because the current continues flowing through Vb during a complete PWM period.

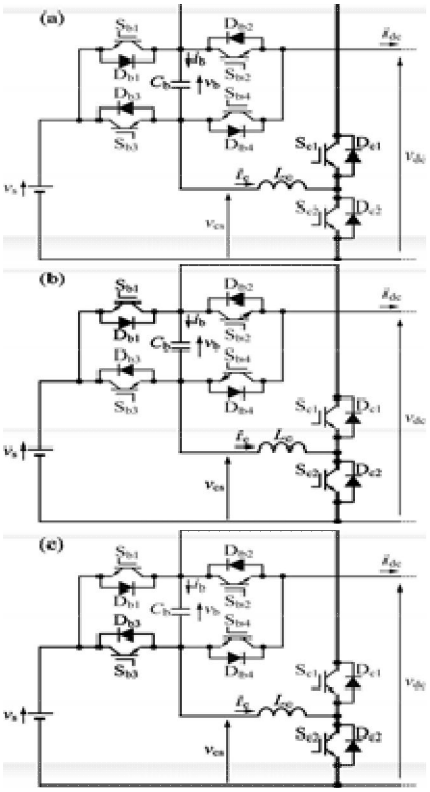

Fig. 6 Modes of operation of dc-dc conversion circuit: (a) on-state of sc1, (b) on-states of sc2 and sb1, and (c) on-states of sc2 and sb3.

Fig. 7 shows the control block diagram for the dc-dc conversion circuit. The current command signal icc is calculated to maintain Vb at the command value Vbc; then the current ic through the inductor Lc is controlled by each PI control block to follow icc. The resulting voltage command signal Vcc is used to generate the signals sc1 and sc2 in the PWM block.

Fig. 8 shows the sequences for sc1 and sc2 during a PWM period.

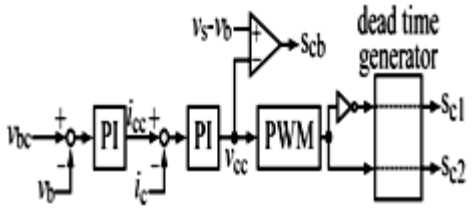

Fig. 7 Control block diagram for dc-dc conversion circuit

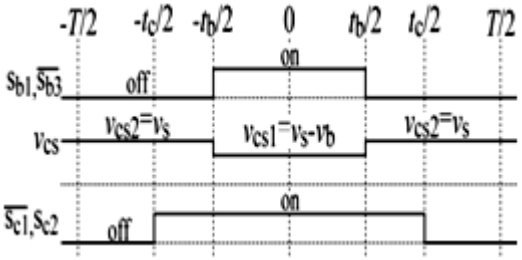

Fig. 8 Signal sequences for dc-dc conversion circuit during PWM period.

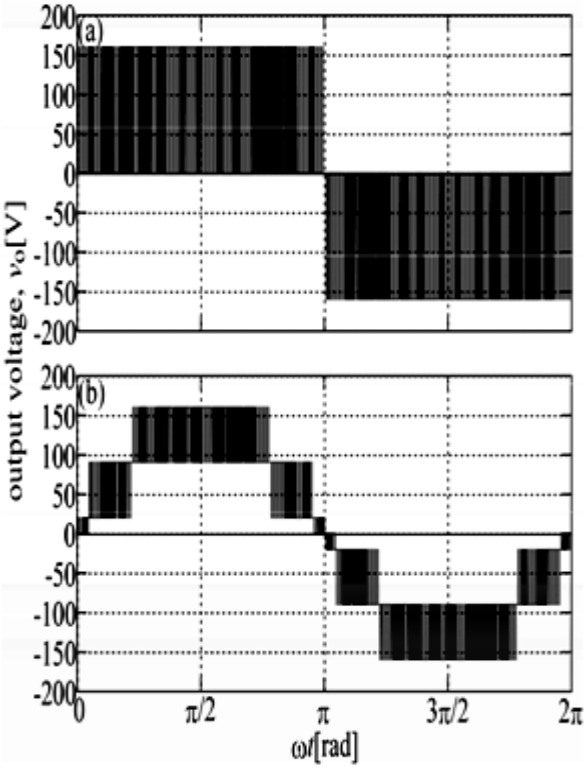

Fig. 9 Simulated waveforms of output voltages of (a) conventional inverter with Vs = 160 V and (b) proposed inverter with Vs= 90 V and Vb = 70 V. Effective value Voc of output voltage command signal is set at 100 V.

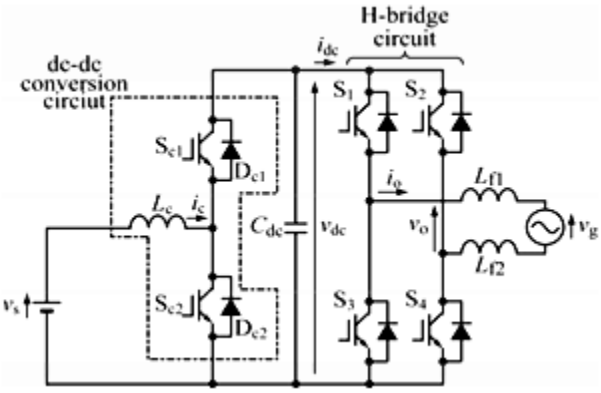

Fig. 10 Conventional inverter with dc-dc conversion circuit

III. SIMULATIONS

Output voltage and its harmonics

Fig. 9 compares the simulated waveforms of the output voltages of single phase inverter on the conventional inverter shown in Fig. 10 with those for the proposed inverter. Fig 11 shows the Simulated Waveform for three-phase inverter. The results confirm that the proposed inverter produces a multilevel output voltage.

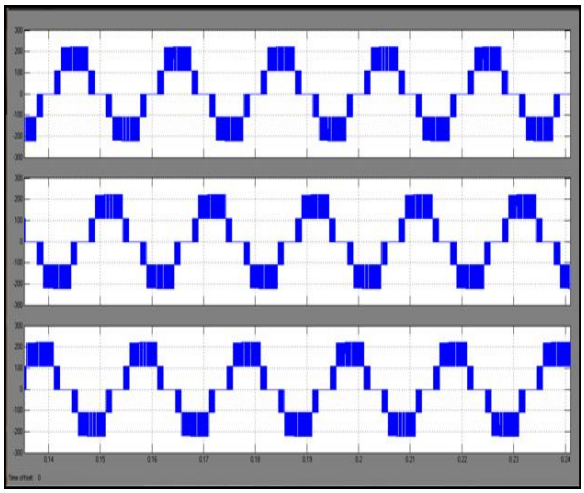

Fig 11: Simulated Waveform for Three-Phase Inverter

IV. EXPERIMENTS

Fig. 12 shows a test circuit of the proposed inverter. This test circuit can be changed to the conventional inverter by changing the connections. Therefore, comparison between the proposed and conventional inverters can be carried out because they use identical devices except for the capacitors as Cdc or the conventional inverter and Cb for the proposed inverter. Table III shows the experimental conditions.

Table III. Experimental Conditions.

Circuit constants	Filter inductance L_{f1} and L_{f2}	1.5mH
	Inductance L_c in dc-dc conversion circuit	2.5mH
	capacitance, C_b and C_{dc}	1.0mF

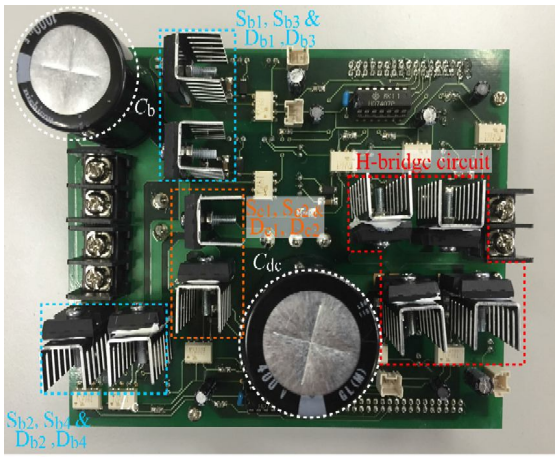

Fig. 12 Test circuit.

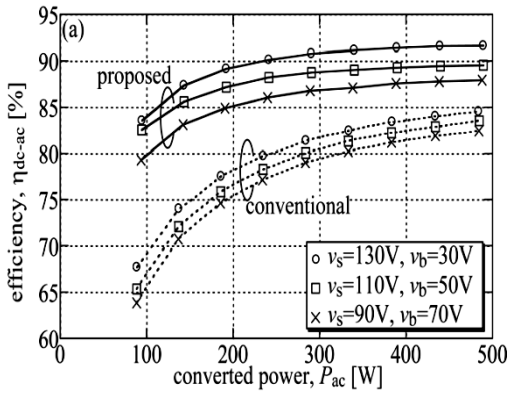

Fig. 13 Efficiencies for dc-ac conversions.

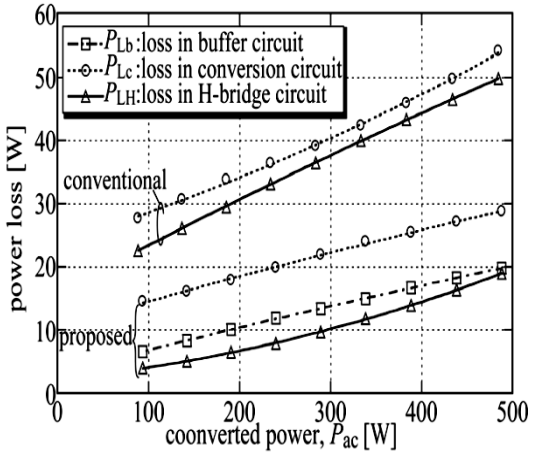

Fig. 14 Power losses in each circuit during dc-ac conversion

Fig 13 Efficiency of proposed inverter are smaller than those of the conventional inverter. The loss PLb is comparatively small. Fig. 18 shows the comparison between the detailed losses of the proposed and conventional inverters. Although the proposed inverter has larger conduction losses in the switches and diodes in total, the switching losses and the losses in the inductors are much smaller than those of the conventional inverter. Based on these results, the superiority of the efficiency of the proposed inverter is considered to occur because of the following factors:

1) The reduction of the current Ic through the chopper inductor Lc, which generates an energy loss because of the inner resistance of Lc.
2) The lower voltage applied to the switches and therefore the decreased switching loss. Therefore, the losses in the dc-dc conversion and the H-bridge circuits are reduced, and in particular, the loss of the H-bridge circuit is reduced to 18% in comparison to the conventional inverter.
3) The smaller ripple in the output current, which leads to a reduction in the iron loss in the filter inductors Lf1 and Lf2.

V. VOLUME CONSIDERATION

Tables IV and V give the voltages applied to the devices in the proposed and conventional inverters (refer to Appendix C). Considering that the voltages of vs+vb and vdc nearly correspond with the amplitude of the grid, the switches in the H-bridge and the dc-dc conversion circuits in the proposed inverter require the same voltage rating as the switches in the conventional inverter. On the other hand, the applied voltage to the switches Sb1-Sb4 in the energy buffer circuit is low. Therefore, switches Sb1-Sb4 can be exchanged with switches with smaller volume. In the test circuit, MOSFET FMW30N60S1HF of Fuji Electric Co., Ltd., which has a voltage rating of 600 V, is used as the switch.

Table Iv. Voltage Applied To Devices In Proposed Inverter

	applied voltage
S1–S4	vs+vb
Sb1–Sb4	*V*b
Sc1and Sc2	vs+vb
*C*b	*V*b

Table V. Voltage Applied To Devices In Conventional Inverter

	Applied voltage
S1–S4	vdc
Sc1and Sc2	vdc
*C*dc	vdc

VI. CONCLUSIONS

This paper proposed a new Three-phase inverter topology with an energy buffer circuit and a dc-dc conversion circuit, and described the control method for this proposed topology. The proposed inverter can output a multilevel voltage, which results in a decrease in the PWM harmonics in the output current. The proposed inverter can perform both dc-ac conversions with higher efficiency than a conventional inverter. The switches, the heat sinks attached to the switches and thecapacitor used in the proposed inverter can all be downsized, because of the small applied voltage, and low loss dissipated in these devices. Furthermore, as a result of its multilevel output, the proposed inverter has a reduced filter inductance at the same THD of about 10%. In addition, because of the reduction of the dc-dc conversion current, the chopper inductor can also be downsized. Consequently, the volume increase caused by the increase in the number of devices can be suppressed significantly. The proposed inverter is confirmed to be useful in practical applications.

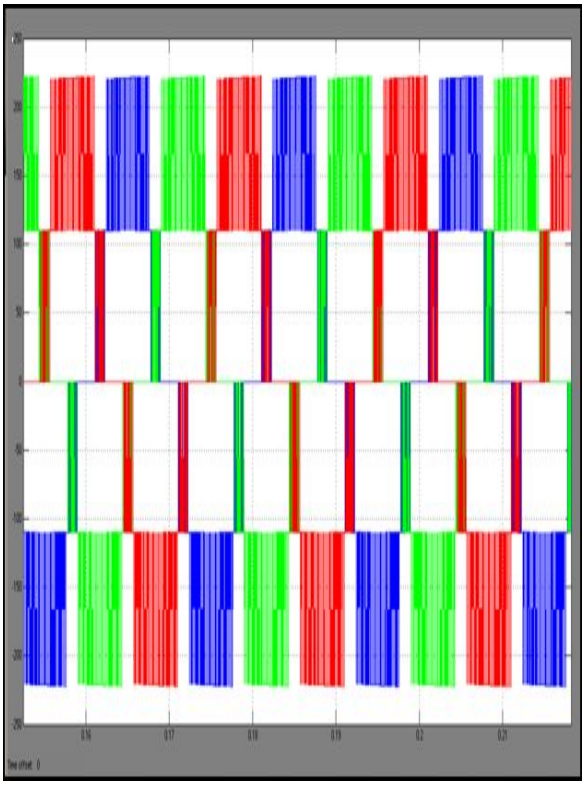

Fig 15: simulated waveform for proposed 5-level three phase inverter

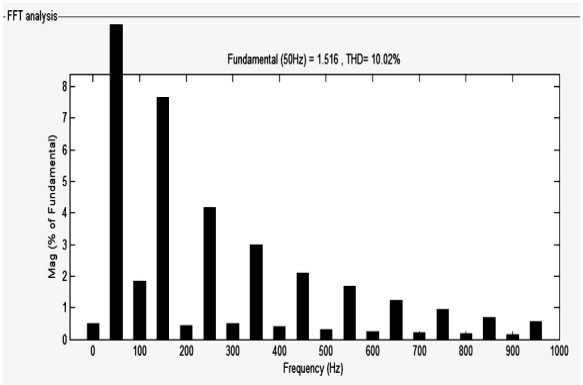

Fig 16: THD analysis for proposed three phase inverter

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