Study and Analysis Probability of Soft Error in Combinational Circuits Using NOR Gate

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Abstract-*As the model technology is being scaled down, physical defects occur. Physical defects are those that can occur in a circuit. During fabrication of chip many types of imperfection can occur, for example, breaks in signal lines, lines shorted. Soft Error are not the permanent error's, they only occur for some time period in a circuit. The soft error's can be resolve by using fault detection techniques. Stuck-at-fault is one of the fault detection technique, the stuck-at-fault is an logical type detection. This paper attempts to reduce the soft error from circuit. The Proposed technique is based on stuck-at-fault in NOR gate for two condition's i.e stuck-at-0 and stuck-at-1 in circuit.*

Keywords-Soft error, stuck-at-faults, tolerate, probability of failure, masking factors.

I. INTRODUCTION

A soft error is a "glitch" in a semiconductor device. These glitches occurs randomly, usually not catastrophic, and normally they do not damage the circuit. They are caused by an external elements outside of the designer's control. Many systems can tolerate some level of soft error. These soft errors may or may not be neglected by the user. The probability of failure indicates where the fault of present i.e in PMOS or NMOS. The Probability of Failure can be considered by using Masking Factors. The Masking Factor consists of three types; Logical masking, Electrical masking, Temporal masking. In this paper the Logical masking is used. The Logical masking occurs in the absence of a functionally sensitized path from the gate to the primary outputs/latches/flip-flops. This can be estimated by fault simulation [4]. The proposed algorithm is to reduce the soft error from the circuit from 3-input NOR gate and to detect the probability of fault occurrence in PMOS and NMOS. Source and drain region are the most sensitive modes to such events due to the large field around the junction regions, which sweeps in the generation electron-holes and results in large current. The fault can be calculated more near drain as compared to source due to more sensitivity presence. The soft errors can be reduces by increasing or decreasing the number of transistors in circuits.

II. RELATED WORK

The proposed technique consists of sizing rules, PMOS and NMOS transistors directly related to the SET attenuation. It is known that PMOS and NMOS transistors have different characteristics in relation to mobility, impurity concentration and, as consequence, the delay with power. For a given particle with charge *Q*, PMOS and NMOS transistors present different attenuation characteristics. Thus, the model considered independently PMOS and NMOS blocks. This model takes into account propagation characteristics in the degradation of the transient pulse is considered in order to reduce sizing rules. Results show smaller area, and timing rule if compared to a symmetrical sizing methodology[1]. The algorithm protects sensitive transistors whose probability of failure (POF) is relatively high. The proposed algorithm can be utilized as follows : 1) apply protection until the Probability of Failure of circuit reaches a certain threshold and 2) apply protection until certain area overhead constraint is met. This methodology gives the optimal solutions are achieved within given area budget provided to the designer. However, generating most favourable solution requires very high CPU time. Therefore, we propose a heuristic based method which upsizes only selected transistor network in sensitive gates based on soft error sensitivity of each gate[2]. The two sizing methods proposed in this paper upsize only PMOS and NMOS transistors in complementary network in a gate to improve SER of nanometer technologies. Our optimization based technique formulates the SER minimization as a nonlinear optimal problem. The optimal results from this approach guarantee the best area distribution within a given budget. The algorithms for weighting the gate area and limiting gate POF are adapted to enhance its operational capability. More importantly, the fault-sensitivity based technique requires relatively small computation time, 10s of milliseconds for large circuits consisting of thousands of gates, compared to the nonlinear optimization problem which may require several hours to generate the optimal solution[3]. In this paper, a versatile SER tolerance optimization framework is developed and employed to optimize the circuit's SER, area and delay simultaneously. The main achievements of this paper can be categorized as follows.1) Versatile SER evaluation algorithm is developed, which can analyse Verilog synthesized netlist automatically and be applicable for not only pure combinational logic circuit but also the

combinational part of sequential logic circuit. 2) Multi-objective genetic algorithm is introduced to the SER optimization realm. The comparison to the other works show that Multi objective genetic algorithm is a better algorithm for SER tolerance, which can optimize the SER, area and delay simultaneously and get better results than the heuristic methods. 3) The framework is developed for industry standard cell library which make it more applicable and can be integrated with the standard digital design flow for SER tolerance design[4]. The proposed technique has an average overhead area, power, and delay for worst case single-event upsets (SEUs) across four process technologies. Since the proposed approach has significantly minimum overhead than approaches based on fault detection and tolerance, and since it also does not require any runtime support in hardware, it is an attractive option to reduce the soft error failure rate with minimal impact to performance. An area for future research is to investigate how the proposed technique can be integrated with other technology-dependent optimization algorithms with multiple objectives[5]. Technology trends are unfortunately such that SEE are likely to become even more of a concern for the future. Decreasing feature sizes, lower operating voltage, and higher speeds all conspire to increase susceptibility to SEU. Upset in avionics is an established concern. Upset at the ground level will continue to be an increasing concern for manufacturers of microelectronics for terrestrial applications. The use of flip-chip packaging and multiple levels of metals will further exacerbate the problem. .Typical methods of mitigation that either increase the transistor count or reduce IC performance will likely not be acceptable to commercial manufacturers, and new methods will need to be developed[6].

III. PROPOSED METHODOLOGY

A. Design Considerations:

- 3-input CMOS NOR gate.
- This CMOS NOR gate consists of three PMOS and three NMOS in it.
- Truth table of NOR gate.

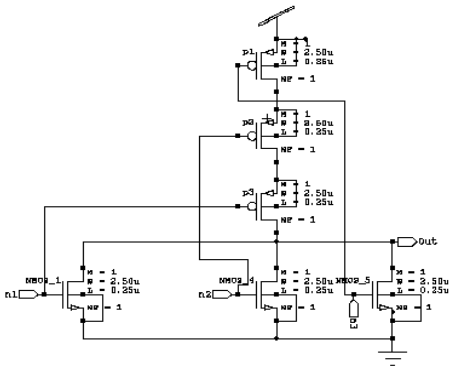


Figure 1: 3-input CMOS NOR gate

B. Description of the Proposed Algorithm:

Aim of the proposed algorithm is to reduce the soft error from the circuit. The proposed algorithm is consists which is as follows:

Algorithm:

Step 1) Select a most sensitive gates.
Step 2) Fault stuck-at-0.

The Fault stuck-at-0 indicates the probability of failure of PMOS in 3-input NOR gate.

Step 3) Fault stuck-at-1.

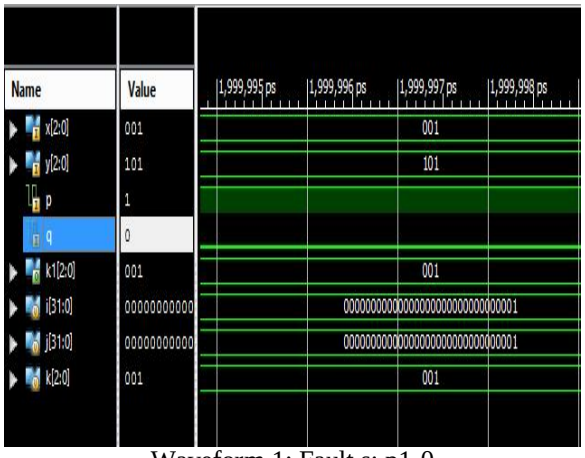
The Fault stuck-at-1 indicates the probability of failure of NMOS in 3-input NOR gate.

Step 4) Simulation count.
Step 5) Failure count 'k'

IV. SIMULATION RESULTS

The simulation studies involve the deterministic 3-input NOR gate figure(1). The proposed algorithm is implemented in Xilinx Software. Source and drain region are the most sensitive modes to such events due to the large field around the junction regions, which sweeps in the generation electron-holes and results in large current. When the inverter input is LOW and the energetic particle strike the drain of an NMOS transistor, the output voltage is temporarily lowered. When the inverter input is HIGH and the energetic particle strike the drain of an PMOS transistor, the output voltage is temporarily raised.

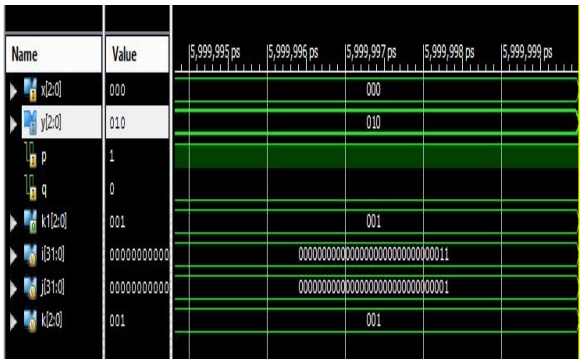
1) Case fault s: p1-0;
Waveform 1: If x=001 and y=101 then k=1
If x=010 and y=110 then k=1
If x=011 and y=111 then k=1
If x=000 and y=100 then k=1



Waveform 1: Fault s: p1-0

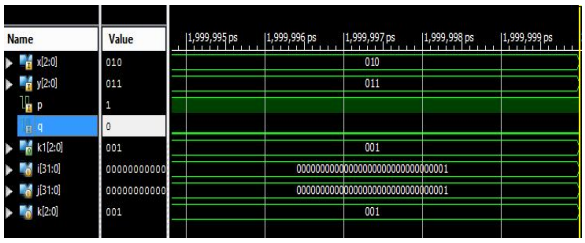
2) Case fault s: n1-1;

Waveform 2: If x=000 and y=100 then k=1
If x=001 and y=101 then k=1
If x=010 and y=110 then k=1
If x=011 and y=111 then k=1



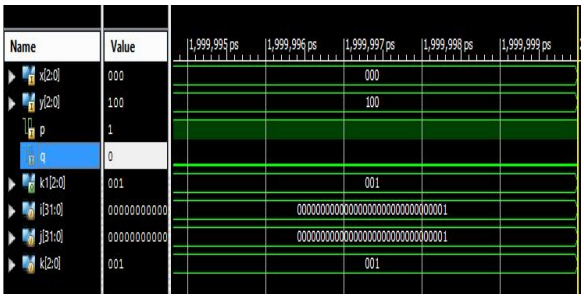
Waveform 2: Fault s: n1-1

3) Case fault s: p2-0;
Waveform 3: If x=100 and y=110 then k=1
If x=001 and y=011 then k=1
If x=101 and y=111 then k=1
If x=000 and y=010 then k=1



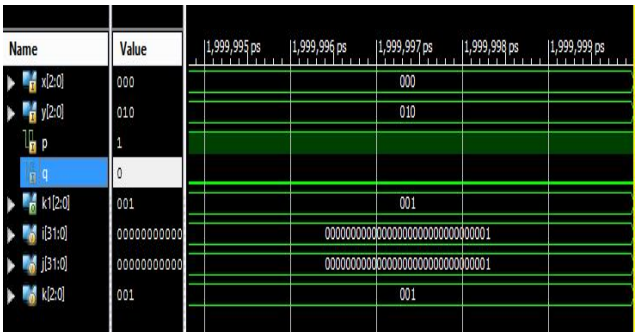
Waveform 3: Fault s: p2-0

4) Case fault s: n2-1;
Waveform 4: If x=000 and y=010 then k=1
If x=001 and y=011 then k=1
If x=100 and y=110 then k=1
If x=101 and y=111 then k=1



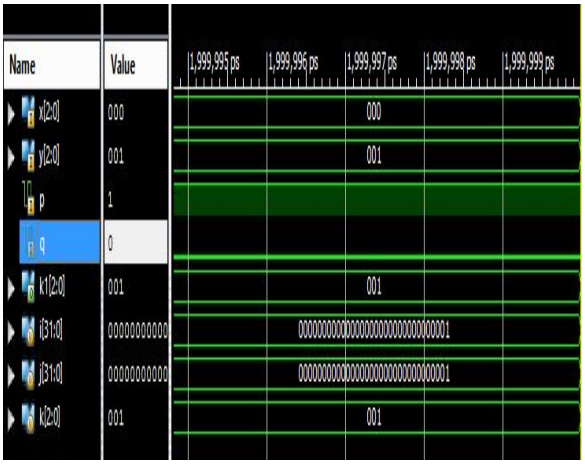
Waveform 4: Fault s: n2-1

5) Case fault s: p3-0;
Waveform 5: If x=100 and y=101 then k=1
If x=000 and y=001 then k=1
If x=110 and y=111 then k=1
If x=010 and y=011 then k=1



Waveform 5: Fault s: p3-0

6) Case fault s: n3-1;
Waveform 6: If x=000 and y=001 then k=1
If x=001 and y=011 then k=1
If x=101 and y=101 then k=1
If x=110 and y=111 then k=1



Waveform 6: Fault s: n3-1

V. CONCLUSION AND FUTURE WORK

The Simulation shows the fault stuck-at-0 and fault stuck-at-1 of PMOS and NMOS, the detection of fault is done. The soft errors are detected and reduced in the circuit by neglecting the minor faults and considering the major faults of the circuit. Once the soft error is detected it is easy to reduce it by increasing or decreasing the number of transistors in circuit. The Fault stuck-at-0 indicates the probability of failure of PMOS in 3-input NOR gate. The Fault stuck-at-1 indicates the probability of failure of NMOS in 3-input NOR gate.

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