Discontinuous Conduction Mode Parallel SEPIC with Wide Output Voltage for Power Factor Pre-Regulator

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Abstract-*A power factor pre-regulator (PFP) usually serves as the first stage of an active two-stage AC/DC converters in a variety of applications including inductive heating systems, wireless charging systems, and onboard chargers for plug-in electric vehicles (PEVs). Conventionally, boost-type PFPs are utilized to regulate the DC-link voltage at a fixed voltage; however, a variable DC-link voltage can enhance the overall efficiency of the converters. In this paper, an interleaved single-ended primary inductor converter (SEPIC) with coupled inductors is proposed as the PFP stage for two- stage AC/DC converters. The converter is designed to operate in discontinuous conduction mode (DCM) in order to achieve soft switching for switches and diodes. The directly coupled inductors are utilized to reduce the number of magnetic components and decrease the input current ripple. A 500W interleaved SEPIC PFP prototype is designed to verify the benefits of this converter. The experimental results show that the converter can maintain high efficiency over a wide range of DC-link voltage.*

Keywords-Power factor pre-regulator (PFP), single- ended primary inductor converter (SEPIC), discontinuous conduction mode (DCM), coupled inductors, interleaved converter.

I. INTRODUCTION

To improve the power quality of the gird, high power factor (PF) and low total harmonics distortion (THD) are required for the grid-connected AC/DC converters. Nowadays, two-stage active AC/DC converters have been widely used in a variety of applications such as onboard chargers for plug-in electric vehicles (PEVs), inductive heating systems, and wireless charging systems. The two-stage AC/DC converters are typically composed of a PFP stage followed by an isolated DC/DC stage, as shown in

Fig.1. A DC/DC resonant converter is usually selected as the second stage due to its attractive features such as soft switching, galvanic isolation, and high efficiency near resonant frequency.

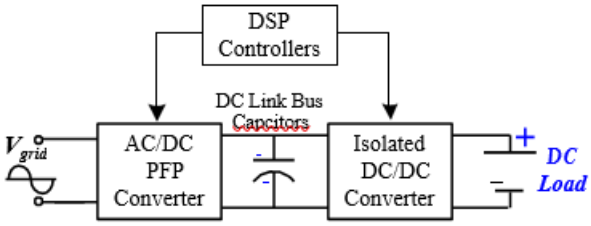


Fig. 1. Typical structure of two-stage active AC/DC converters.

The objective of PFP stage is to improve power quality and reduce harmonic contamination. The topology for the PFP stage is a diode bridge followed by a boost-type converter. Although the boost-type PFP converters can provide efficiencies over 98% , the overall efficiency of the two-stage converter is reduced significantly if the second-stage resonant converter cannot operate near the resonant frequency.

In the application of onboard battery chargers for PEVs, as shown in Fig. 2, a LLC resonant converter stage follows a boost-type PFP stage. The output voltage of the LLC converter is regulated by pulse frequency modulation. The resonant frequency is the optimal operation frequency associated with the highest efficiency. The operating frequency of the LLC converter moves away from the resonant frequency when the battery voltage is lower than the rated voltage at a lower state of charge (SOC). Consequently, the efficiency of the LLC converter drops significantly. To achieve the highest possible efficiency, i.e. ensure operation at resonant frequency, the input voltage of the LLC converter can be regulated to follow the output battery voltage. Due to the wide variation of the battery pack, the DC-link voltage should be regulated over a wide range and sometimes b ecome less than the PFP's input voltage. However, the output voltage of boost-type topologies cannot be lower than the input voltage.

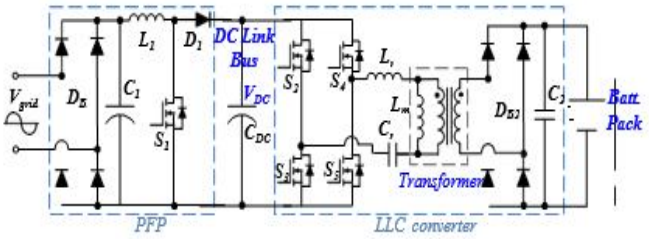


Fig. 2. Two-stage battery charger system.

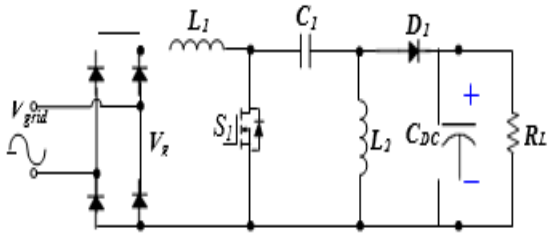


Fig. 3. Traditional SEPIC PFP converter.

Additionally, the boost-type PFPs are not the most suitable topologies for inductive heating applications, where the high frequency AC magnetic field should be generated to deliver power over a distance by a subsequent resonant converter stage. A wide output voltage variation is required in this application due to a need for variable power levels for heating. Similar to onboard charger application, a fixed DC-link voltage would result in lower overall efficiency particularly in light loads by using a resonant DC/DC converter stage controlled by pulse frequency modulation. For such applications, a PFP stage capable of providing a wide regulated DC-link voltage, such as a single-ended primary-inductor converter (SEPIC) PFP, can improve the overall efficiency of the systems to a great extent.

The SEPIC topology, shown in Fig. 3, has been investigated as the PFP in AC/DC converters in various applications including standalone photovoltaic systems and LED lighting systems. In a SEPIC PFP, the output voltage can be either higher or lower than the input voltage. The voltage and current stresses of diodes and switches, in a traditional SEPIC converter, are much higher than a boost- type topology at the same power level. Thus, the traditional SEPIC topology is not widely used for high power applications. The bridgeless SEPIC PFP converters have been investigated to reduce the conduction loss of the diode bridge. However, the voltage and current stresses of switches are not reduced, and the power level is usually limited to less than 150W, due to voltage and current limitations of switches in the orders of 300V and 10A, respectively. In addition, in the continuous conduction mode (CCM), the SEPIC converters have large hard-switching losses, especially in high frequency operation. Therefore, the efficiencies are low for a traditional SEPIC converter operated in CCM. In [3], the power level is increased by interleaving two SEPIC converters. However, this topology is constructed by directly paralleling two traditional SEPIC converters, and consequently the input current ripple is large in discontinuous conduction mode (DCM) operation.

In this paper, a two-phase interleaved SEPIC AC/DC converter with coupled inductors is proposed to serve as the PFP stage with a wide range of output DC-link voltage. Its topology is shown in Fig. 4. The input power is shared evenly between two phases to reduce the current stresses of the switches and diodes; and consequently, the power level can be increased. Since the CCM operation causes large switching losses, the DCM operation is selected to enable soft switching. The ZVS can be realized for the MOSFET's to reduce the switching losses, while the ZCS can be realized for diodes, D1 and D2, to eliminate reverse recovery losses [14]. In order to reduce the number of magnetic components, the corresponding inductors in two phases are directly coupled. The input current ripple could be significantly reduced through proper design of the coupled inductors.

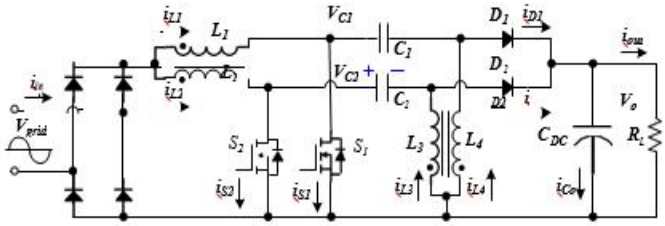


Fig. 4. Proposed interleaved SEPIC PFP converter.

This paper is organized as follows. The principle of operation is presented in Section II. The theoretical analyses are elaborated in Section III. Furthermore, experimental results of a 500W prototype are demonstrated in Section IV for validation of the analyses. Finally, Section V concludes the manuscript.

II. OPERATION PRINCIPLE

In Fig. 4, the rectified voltage after the diode bridge can be modeled as an equivalent variable DC source Vg. Assuming that the DC-link capacitor CDC and two middle capacitors C1, C2 are large enough and their voltage ripples are negligible compared with their steady-state voltages. The output capacitor can be modeled with an equivalent DC source Vo. Since the middle capacitors C1 and C2 have the same steady- state voltages as the input rectified voltage Vg, the two

middle capacitors can be modeled as the equivalent variable DC source Vg [24], as shown in Fig. 5.

The analyses are separated into the higher output voltage case and the lower output voltage case as the output voltage of a SEPIC converter can be either higher or lower than the input peak voltage. These two cases are analyzed in this section using the derived equivalent model.

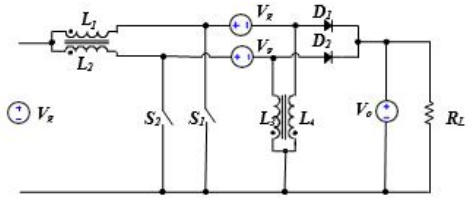


Fig. 5. Equivalent circuit of the proposed interleaved SEPIC converter.

A. Lower Output Voltage Case

The output voltage of PFP stage can be lower than the input peak voltage. In DCM operation, the duty cycle is less than 0.5, and it is also less than the duty cycle derived in CCM operation with the same output voltage .

The typical waveforms of the converter in DCM are shown in Fig. 6, in which there are six modes in one switching cycle. There are three modes in each of the positive and the negative half cycle operations. Here, only three modes in positive half cycle are analyzed due to the symmetry of operation. The equivalent circuit for each mode is shown in Fig. 7.

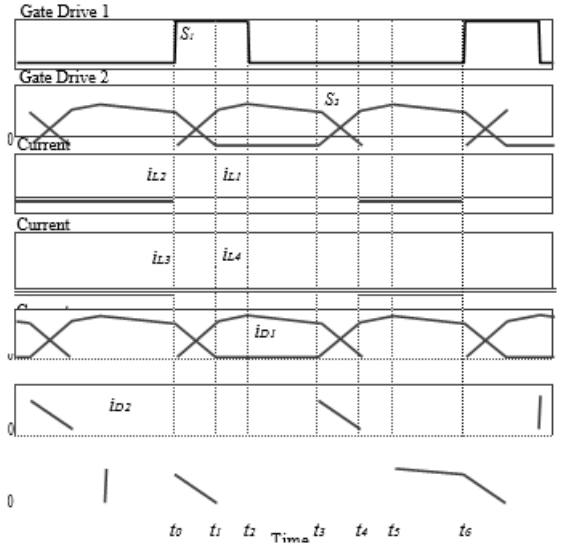


Fig. 6. Typical waveforms of the interleaved SEPIC converter in DCM.

In this two-phase interleaved topology, the corresponding inductors in two phases are coupled using the same cores with the same coupling coefficients. The inductor L1 is coupled with L2, while the inductor L3 is coupled with inductor L4. These four inductors have the same self-inductances and mutual inductances. In each operation mode, the voltages across inductors L1 and L4 are the same in each operation mode. Thus, the inductor currents iL1 and iL4 have similar waveforms as shown in Fig. 6. Similar waveforms are valid for inductors L2 and L3.

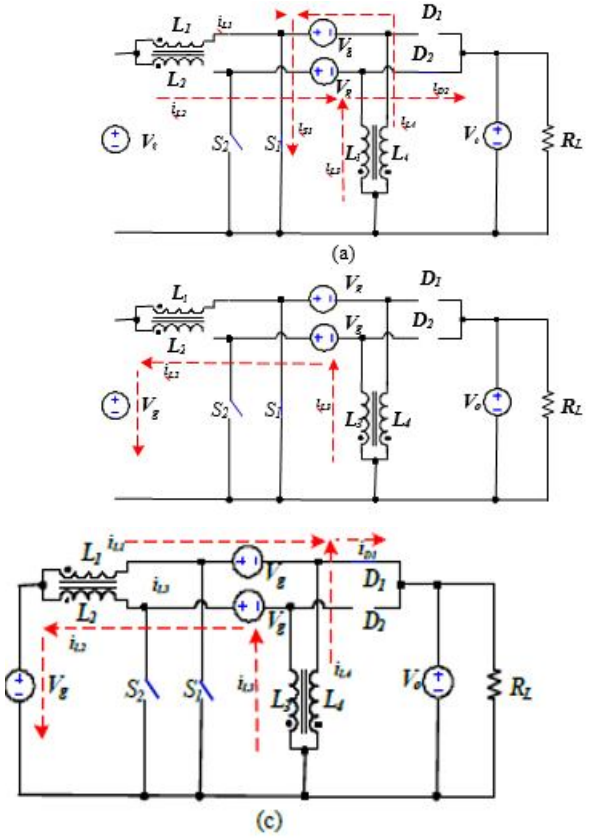


Fig. 7. Equivalent circuits in DCM, (a) Mode I, (b) Mode II, (c) Mode III.

1) Mode I (t0-t1):

In this mode, as shown in Fig. 7(a), the switch S1 is on, while the switch S2 is off. The diode D1 is off, and diode D2 is on. The voltages across both inductors L1 and L4 are Vg. Therefore, the inductor currents iL1 and iL4 increase at the same rates. The current through S1, iS1, is the sum of the inductor currents iL1 and iL4. Meanwhile, voltages across both inductors L2 and L3 are −Vo. Thus, the inductor currents iL2 and iL3 decrease at the same rates, and the current throughdiode D , i , is the sum of these two inductor currents.

As the inductors L1 and and L2are directly coupled, the core flux is affected by both inductor currents iL1 and iL2. The mutual inductance, M, is defined as

$$M=\sqrt{L_{12}\cdot L_{21}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where, L12 is the mutual inductance induced by the inductor current iL1 in inductor L2, and L21 is the mutual inductanceinduced by the inductor current iL in inductor L . Since themutual inductance of inductors L1 and L2 are the same, the mutual inductance M has the same value as L12 and L21. Additionally, the coupling coefficient, k, is defined as,

$$k=\frac{M}{\sqrt{L_1\cdot L_2}} \qquad (2)$$

where, L_1 and L_2 are self-inductances of the first coil and the second coil

The voltages and currents of the mutually coupled inductors can be expressed as,

$$V_g=L_1\frac{di_{L1}}{dt}+M\frac{di_{L2}}{dt} \qquad (3)$$

$$\frac{di_{L1}}{dt}=\frac{di_{L2}}{dt} \qquad (4)$$

Eq. (3) and Eq. (4) can be rearranged as,

$$\frac{di_{L1}}{dt}=\frac{V_g+kV_o}{(1-k^2)L_1} \qquad (5)$$

$$\frac{di_{L2}}{dt}=-\frac{V_o+kV_g}{(1-k^2)L_2} \qquad (6)$$

(b)

Seen from the Fig. 6, the inductor current iL2 decreases all the time and changes the flowing direction in this mode. The current through diode D2, iD2, keeps on decreasing. The

variations of inductor currents, Δi_{L1} and Δi_{L2}, can be expressed as,

$$\Delta i_{L1}=\frac{V_g+kV_o}{(1-k^2)L_1}D'T \qquad (7)$$

$$\Delta i_{L2}=\frac{V_o+kV_g}{(1-k^2)L_2}D'T \qquad (8)$$

here, T is the switching period, and $D'T$ is the time interval between t_0 and t_1.

2) Mode II (t1-t2):

At t1, the current through diode D2, iD2, which is the sum of inductor currents iL2 and iL3, drops to zero. Then, the diode turns off with ZCS. Meantime, the inductor currents iL3 and iL2 flow in a loop composed of the inductor L3, the capacitor C2, the inductor L2, and the equivalent voltage source Vg, .

The variations of inductor currents iL3 and iL2 are the same due to the same voltages across inductors L3 and L2. In addition, the average current of iL3 is higher than the average current of iL2 [17]. Thus, at t1, when the inductor currents iL3 and iL2 drop to minimum, the inductor current iL3 is higher than iL2 with iL3 as positive value and iL2 as negative value, as shown in Fig. 6. The current flows from inductor L3 to inductor L2 in the aforementioned loop containing inductors L3 and L2. Assuming that the resistances of inductors and capacitors in this loop are negligible, the loop current remains constant from t1 to t2, as expressed in Eq. (9).

$$i_{L3}=-i_{L2}=const \qquad (9)$$

The inductor current iL1 changes with a higher rate in comparison to Mode I as expressed in Eq. (10). The current of coupled inductor L2 is constant, and only sets the flux bias.

$$\frac{di_{L1}}{dt}=\frac{V_g}{L_1} \qquad (10)$$

Consequently, the variation of inductor current, ΔiL1, can be expressed as,

$$\Delta i_{L1}=\frac{V_g}{L_1}(D-D')T \qquad (11)$$

where, D is the duty cycle. Similar expressions are valid for the inductor L4.

3) Mode III (t2-t3):

As shown in Fig. 7(c), both switches are off in this mode. The diode D2 is off, while the diode D1 turns on. The constant current flows in the aforementioned loop consisting of inductors L2 and L3. The inductor currents iL1 and iL4 decrease from maximum values, and the sum of them flows through the diode D1. The voltages across both inductors L1 and L4 are −Vo. The inductor current iL1 decreases at a rate expressed as,

$$\frac{di_{L1}}{dt}=-\frac{V_o}{L_1} \qquad (12)$$

Consequently, the variation of inductor current, Δi_{L1}, can be shown as,

$$\Delta i_{L1}=-\frac{V_o}{r_1}(0.5-D)T \quad (13)$$

Similar expressions are applicable for the inductor L_4.

B. Higher Output Voltage Case

The waveforms of higher output voltage case are similar to those of lower output voltage case. In DCM, the operation principles of higher output voltage case are similar to those of lower output voltage case. In a switching cycle, there are six modes, among which only three modes are analyzed due to the symmetry of operation.

1) Mode I:

The inductor currents i_{L1} and i_{L2} increase simultaneously at small rates. Similar to the lower output voltage case, the slew rate of inductor current i_{L1} and i_{L2} are expressed as,

$$\frac{di_{L1}}{dt}=\frac{V_g}{(1+k)L_1} \quad (14)$$

$$\frac{di_{L2}}{dt}=\frac{V_g}{(1+k)L_2} \quad (15)$$

Thus, the inductor current variations, Δi_{L1} and Δi_{L2}, can be expressed as,

$$\Delta i_{L1}=\frac{V_g}{(1+k)r_1}(D-0.5)T \quad (16)$$

$$\Delta i_{L2}=\frac{V_g}{(1+k)r_2}(D-0.5)T \quad (17)$$

Since the L_3 and L_4 have the same inductance values as L_1 and L_2, similar equations can be derived for the inductor currents i_{L3} and i_{L4}.

2) Mode II:

Similar to the lower output voltage case, the slew rate of inductor current i_{L1} can i_{L2} are expressed as,

$$\frac{di_{L1}}{dt}=\frac{V_g+kV_o}{(1-k^2)L_1} \quad (18)$$

$$\frac{di_{L2}}{dt}=-\frac{V_o+kV_g}{(1-k^2)L_2} \quad (19)$$

The inductor current i_{L3} decreases and changes the direction in this mode. The current through diode, D_2, keeps on decreasing. $D'T$ is the time interval between the diode D_2 turn-on and turn-off. The variations of inductor currents, Δi_{L1} and Δi_{L2}, can be expressed as,

$$\Delta i_{L1}=\frac{V_g+kV_o}{(1-k^2)L_1}D'T \quad (20)$$

$$\Delta i_{L2}=\frac{V_o+kV_g}{(1-k^2)L_2}D'T \quad (21)$$

3) Mode III (t_2-t_3):

At t_2, the current through diode, D_2, drops to zero. Then, the diode turns off with ZCS. Meanwhile, the currents of inductors L_2 and L_3 circulate in a loop composed of the inductor L_3, the capacitor C_2, the inductor L_2, and the equivalent voltage source V_g. The constant current flows from inductor L_2 to inductor L_3. Thus, Eq. (22) can be obtained as,

$$i_{L3}=-i_{L2}=const \quad (22)$$

The inductor current i_{L1} changes with a higher rate in comparison to Mode I as expressed in Eq. (23). The current of coupled inductor L_2 is constant, and only sets the flux bias.

$$\frac{di_{L1}}{dt}=\frac{V_g}{L_1} \quad (23)$$

Therefore, the inductor current variations, Δi_{L1}, can be expressed as,

$$\Delta i_{L1}=\frac{V_g}{r_1}(D-D')T \quad (24)$$

Similar expressions are valid for inductor L_4.

III. ANALYSIS OF THE PROPOSED PFP TOPOLOGY

Based on the operation principles for higher output voltage and lower output voltage cases, the detailed analysis can be conducted to set the critical parameters of power components and to assess the circuit performance. Relevant expressions are derived in this section. The analyses are based on the assumption of unity power factor and a constant output voltage due to a large output filter capacitance.

A. Reduced Input Current Ripple by Coupled Inductors

In this section, the input current ripple is calculated in DCM operation. Although the two SEPIC converters work in DCM operation individually, the input current maintains CCM features with a small input current ripple.

As shown in Fig. 6, from t_0 to t_1, the current of L_1 increases, and the current of L_2 decreases. In this interval, the input current variation, Δi_{in}, is the sum of the current variations of inductors L_1 and L_2. It can be expressed as,

$$\Delta i_1=\left(\frac{V_g+kV_o}{(1-k^2)L_1}-\frac{V_o+kV_g}{(1-k^2)L_2}\right)D'T \quad (25)$$

From t_1 to t_2, the current of L_2 becomes constant, and the current of L_1 increases at a different rate. The input current variation, Δi_2, is expressed as,

$$\Delta i_2=\frac{V_g}{r_1}(D-D')T \quad (26)$$

The input current ripple is the sum of the two variations, Δi_1 and Δi_2. Thus,

$$\Delta i=\Delta i_1+\Delta i_2=a\cdot D'T+b\cdot(D-D')T \quad (27)$$

where, a and b are the weighted coefficients.

$$a=\frac{V_g-V_o}{(1+k)L},\quad b=\frac{V_g}{L} \tag{28}$$

where, $L=L_1=L_2$.

The coefficient a is much smaller than coefficient b, and consequently the input current ripple is mostly determined by second term based on Eq. (27). Thus, the input current becomes larger as the converter works in deeper DCM operation. In order to reduce the input current ripple, the converter should operate under DCM in close proximity to boundary conduction mode (BCM). When D' becomes equal to D, the converter works in BCM with minimum input current ripple.

Compared with the input current ripples of traditional SEPIC and interleaved SEPIC with non-coupled inductors, the input current ripple is significantly reduced. The expressions for input current ripples are listed in Table I.

TABLE I
INPUT CURRENT RIPPLES OF THREE TOPOLOGIES

Topology	Input current ripple
Traditional SEPIC	$T\frac{V_g}{L}D$
Interleaved SEPIC (non-coupled)	$\frac{V_g-V_o}{L}D'T+\frac{V_g}{L}(D-D')T$
Interleaved SEPIC (coupled)	$\frac{V_g-V_o}{(1+k)L}D'T+\frac{V_g}{L}(D-D')T$

B. *Worst Case for DCM Operation and Minimum Coupling Coefficient*

As shown in Fig. 6, most of the inductor current variations happen when the currents in the mutually coupled inductors change rapidly in opposite directions. Thus, the inductor current variation can be simplified as,

$$\Delta i_L \approx \frac{V_g+kV_o}{(1-k^2)L_2}DT \tag{29}$$

Assume the output voltage, Vo, is constant. With fixed k and L2 parameters, Eq. (30) shows that the inductor current variation monotonically increases with the duty cycle. At peak input voltage, the duty cycle would reach its minimum value, and the current ripple would be minimum. Meantime, the instantaneous value of current Ig would be maximum at peak input voltage, as shown in Eq. (31).

$$I_g=I_p\sin(\theta) \tag{31}$$

where, θ is equal to $\pi/2+k\pi$ radian, and k is an integer.

In other words, the peak input voltage corresponds to the largest instantaneous current and the smallest current ripple. Thus, the peak input voltage is the worst case to maintain the DCM operation in a grid cycle. Designing the circuit to operate under DCM in this worst case can ensure DCM operation for the entire period.

The coupling coefficient, k, is critical for ensuring DCM operation. According to Eq. (29), given a smaller coupling coefficient, the inductor current variation would become smaller, and it would be harder for the converter to operate in DCM. Hence, there exists the minimum coupling coefficient, kmin, corresponding to operation in BCM, which shares the same soft-switching features as the DCM operation. Fig. 8 shows the typical waveforms of BCM operation in higher output voltage case.

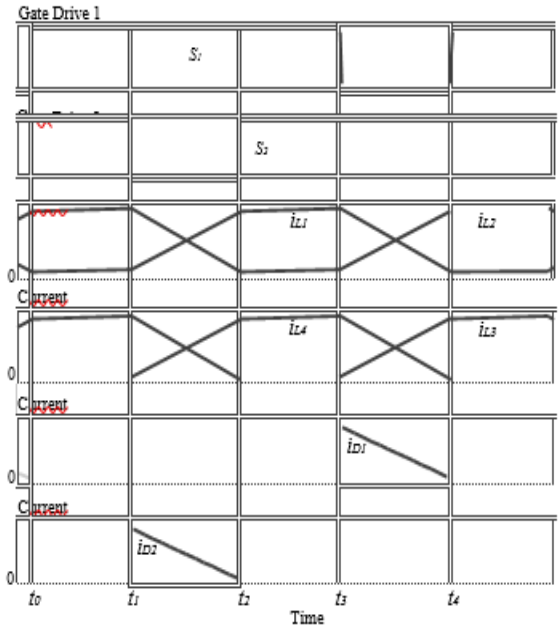


Fig. 8. Typical waveforms of the converter with k_{min} in higher output voltage case.

In Fig. 8, there are four modes in one switching cycle. At t2, the inductor currents iL2 and iL3 reach minimum values, and the sum of these two currents is the current through diode D2, which drops to zero. At the same time, the switch S2 turned on, and the diode D2 turned off with ZCS. Thus, it is proved that the converter operates in BCM.

The kmin can be obtained by simulation. In Table II, the kmin, is obtained for different inductances of inductor L2 in both higher output voltage case and lower output voltage case.

TABLE II

Inductance L_2	k_{min} (lower *Vout* case)	k_{min} (higher *Vout* case)
200μH	0.6693	0.1397
300μH	0.7837	0.4475
400μH	0.8391	0.5909
500μH	0.8719	0.6749
600μH	0.8936	0.7301

According to Table II, kmin increases with inductance L2. Based on Eq. (29), with the inductance of L2 increasing, the coupling coefficient has to increase to keep the inductor current variation unchanged so that the inductor current iL2 can enter DCM in the worst case. The same principle is valid for other inductors.

When designing the components, the coupling coefficient k has to be set higher than the minimum value for specially chosen inductances to ensure DCM. However, k cannot betoo much higher than the calculated minimum value. Otherwise, the converter would work in deep DCM resulting in large input current ripple according to Eq. (27) and Eq. (28).

C. Theoretical Estimation of Circuit Performance

For simplicity of analysis, it is assumed that the coupled PFP operates under DCM in close proximity to BCM. The analysis is conducted in BCM for the proposed converter. In BCM operation, the diodes turn off with ZCS when the currents through them decrease to zero. Hence, the reverse recovery losses are eliminated due to ZCS turn-off. As for the two MOSFETs, the ZVS turn-on is enabled since the currents through the switches decrease to zero before they turn on. Consequently, the turn-on switching losses are ignored.

The current ripples of the coupled inductors are assumed to be triangular waveforms. The ripple is assumed to be half of the peak value for CCM operation, which is a common assumption in designing inductors in SEPIC circuits [21]. Table III shows the comparison of three different topologies to highlight the benefits of the proposed topology.

As it can be seen from Table III, the proposed topology has much lower current ripple and output voltage ripple compared with the traditional SEPIC PFP. The interleaved topology has reduced input current ripple and output voltage ripple. The use of coupled inductors allows the converter to have the same count of magnetic cores as the traditional SEPIC converter. The DCM operation reduces the switching losses to a large extent while the input current ripple and output voltage ripple are kept close to the CCM operation. Hence, the efficiency is improved significantly.

TABLE III
COMPARISON OF THREE TOPOLOGIES

Topology	Interleaved SEPIC BCM-PFP	Interleaved SEPIC CCM-PFP	Traditional SEPIC CCM-PFP
Input ripple Current (high frequency)	$\frac{V_g - V_o}{(1+k)L} D1$	$\frac{(2D-1)V_g}{(1+k)L}$	$\frac{DV_g}{L}$
Inductor RMS current	$\frac{\sqrt{30}\,P_{in}}{6\,V_{PK}}$	$\frac{\sqrt{21}\,P_{in}}{6\,V_{PK}}$	$\frac{\sqrt{21}\,P_{in}}{3\,V_{PK}}$
Output voltage ripple	$\frac{P_{in}}{4V_oC_of_s}$	$\frac{(D-0.5)P_{in}}{V_oC_of_s}$	$\frac{DP_{in}}{V_oC_of_s}$
Output Cap peak Current ripple (Low frequency)	$\frac{4V_{PK}P_{in}}{V_o(V_{PK}+V_o)}$	$\frac{4V_{PK}P_{in}}{V_o(V_{PK}+V_o)}$	$\frac{4V_{PK}P_{in}}{V_o(V_{PK}+V_o)}$

To validate the improved efficiency of the proposed PFP, theoretical loss analyses are conduct for the proposed PFP and the interleaved SEPIC CCM-PFP. The loss breakdowns are calculated for both topologies at full load condition at V_{in}=110Vac, V_{out}=190V (for higher V_{out} case) and V_{out}=90V (for lower V_{out} vase). output voltage case, resulting in significantly increased input current ripple in this case. On the other hand, the inductance L2 cannot be too large because the coil turns increase largely for higher inductance L2, resulting in much larger size of the coupled inductors.

According to Table II, the inductance of 400uH with a minimum coupling coefficient of 0.8391 is selected for both coupled inductors. To ensure the DCM operation, the coupling coefficient is chosen as 0.85.

To implement the coupled inductor, the ETD44 core is selected, and Litz wire is adopted to build the coils due to the high switching frequency. Coils of both coupled-inductors have 24 turns. The air gap is tuned to be 0.3mm to set the coupling coefficient as 0.85. As the voltage stress between the two coupled-inductors is really high, a large air gap (5mm) is incorporated between the two coils. An image of the coupled inductor, designed for this application, is shown in Fig. 11.

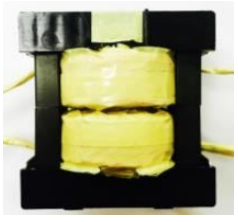
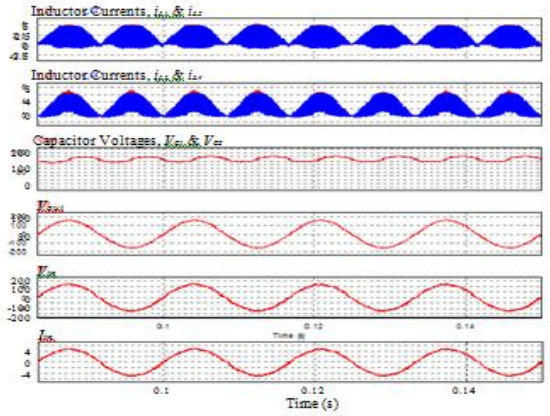


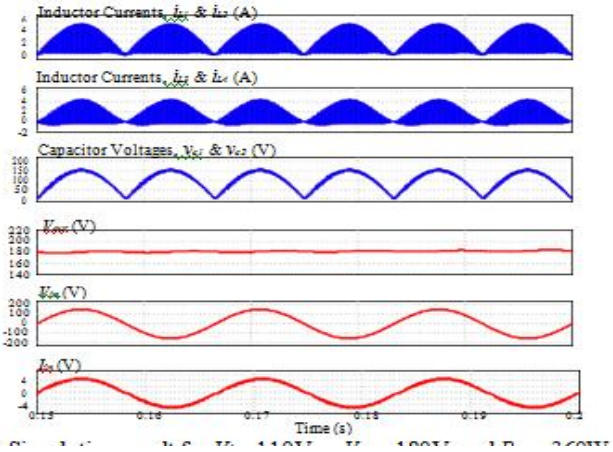
Fig. 9 Coupled inductor applied in the circuit.

The parameters of all the components in the two-phase interleaved SEPIC converter with coupled inductor s are listed in Table IV.

Parameter	Symb	Value
Input voltage	V_{in}	85Vac-135Vac,
Output voltage	V_o	50V-200V
SEPIC capacitor	C_1,	1uF
Input inductor	L_1, L_2	400uH
Output inductor	L_3, L_4	400uH
Coupling	k	0.85
Switching	f_s	150kHz
Output capacitor	C_{DC}	2mF



Simulation result for Vin=110Vac, Vo=90V, and Pout=370W.



Simulation result for Vin=110Vac, Vout=180V, and Pout=360W

C. Simulation Results

In order to validate the advantages of the proposed topology and the designed parameters, simulations are conducted for 90V output voltage and 180V output voltage cases. The inductance is set as 400μH for all the inductors with 0.85coupling efficient. The input voltage is 110Vac. The simulation results are shown in Fig. 12 and Fig. 13. The DCM operation can be observed from the inductors current waveforms. According to the simulation results in Fig. 12, the input voltage is in phase with the input current. The power factor is 0.998, and the THD of the input current is 3.5%. According to Fig. 13, the power factor is 0.996, and THD of the input current is 3.1%. As the output voltage is higher than the input voltage, the currents of L1 and L2 are mostly positive. In simulation, an ideal diode bridge is utilized to rectify the AC input voltage.85Vac, the output voltage can be stepped down to as low as 50V. When the input voltage is 135Vac, the output voltage can be stepped up to as high as 200V. The limits of output voltage vary with the input voltage. For simplicity, a typical scenario is demonstrated in the experimental section, in which the input voltage is set as 110Vac, and waveforms shown for output voltages at 90V and 190V to demonstrate the step-up and step-down features of the proposed interleaved SEPIC converter.

The AC input voltage at 110V,RMS (60Hz) is provided by a controllable Chroma 61605 AC power supply.fig 10 show the current and voltage waveforms for lower output voltage case. In Fig. 15, the waveforms of the inductor currents iL1 and iL2 in DCM operation are shown. With the switch S1 on, the inductor current iL1 increases rapidly. At the same time, the inductor current iL2 drops rapidly until the current through the diode decreases to zero. In Fig. 16, the waveforms of the inductor currents iL2 and iL3 in DCM operation are presented. Since the average input current was lower than the average output current, the inductor currents iL2 drops below zero, while the inductor currents iL3 is maintaining a positive minimum current value. The sum of inductor current iL2 and iL3 decreases and gets very close to zero. At this moment, switch S2 turns on. In other words, the converter almost works in BCM. Hence, the experimental results are consistent with the theoretical analyses.

In Fig. 17, the zoom-out waveforms of inductor current iL1 and iL2 are shown. The waveforms of the input voltage, input current and output voltage at steady state are shown in Fig. 18. The output voltage is regulated at 90V, and the output power is 370W with the power factor measured as 0.997.

Lower V_{out} Case		Higher V_{out} Case	
Power (W)	THD (%)	Power (W)	THD (%)
105	9.8	138	10.3
262	6.7	340	6.9
370	6.0	423	6.2
495	5.7	498	5.8

Table for THD of different Power ratig

The THD of input current is shown in above Table for Vout =90V and V_{out}=190V at V_{in}=110V at different power levels.

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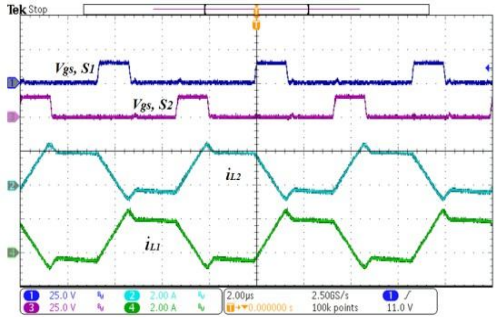

Fig 10.Waveforms of drive pulse, inductor currents iL1 and iL2 in lower output voltage case.

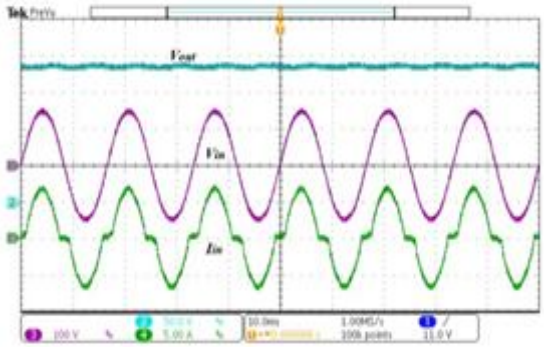

Fig 11. Steady-state waveforms of output voltage, input current and input voltage in higher output voltage case, Pout=402W

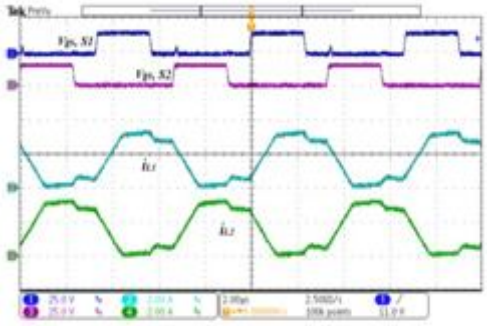

Fig 12 Steady-state waveforms of output current, input current and input voltage in lower output voltage case, Pout=370W

The zoom-out waveforms of inductor current iL1 and iL2 are shown in, the waveforms of the input voltage, input current and output voltage at steady state are shown. The output voltage is regulated at 190V, and the output power is 402W with the power factor equal to 0.991.

In Fig. 18 and Fig. 22, the zero-crossing distortion of input currents happens due to the forward voltage drop of diodes in the diode bridge, which is utilized to rectify the AC input voltage. Furthermore, when the input voltage is close to zero, the input current cannot ramp up quickly due to small voltages across inductors L1-L4. The current slew rate needed to reach the reference input current exceeds the available current slew rate, so the input current lags behind the reference input current for a short period of time, resulting in the zero-crossing distortion of the input current.

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III. CONCLUSION

This paper proposed a novel interleaved two-phase SEPIC PFP with inductors directly coupled. The directly coupled inductors can reduce the number of magnetic components, decrease the input current ripple. The key circuit and design features are summarized as follows. The power level of SEPIC PFP is improved by interleaving two SEPIC converters, the voltage and current stresses of the diodes and switches are largely reduced, improving the power level up to 500W. High efficiency is maintained over a wide range of DC-link voltage. The converter is designed to operate in DCM in order to achieve ZVS for switches and ZCS for diodes. The input current ripple is reduced by properly designing the coupled inductors. The inductance and coupling coefficient are carefully selected for the coupled inductors to ensure the DCM operation in close proximity to BCM operation over the wide range of DC-link voltage.

A 500W prototype is built to validate the advantages of this proposed PFP. The experimental results show the proposed interleaved SEPIC PFP can provide a wide output DC-Link voltage from 90V to 190V at 110Vac input voltage, and the efficiency is over 96% at 500W over a wide range of DC-link.

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works are Vehicle Number Plate Detection (VNPD) system algorithm based on template matching. They have devised an efficient method for recognition of Indian vehicle number plates.

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