A Near Sinusoidal Three Phase Five Level Voltage Source Inverter With Fundamental Switching Frequency

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Abstract- *In this paper, a near sinusoidal three phase five level voltage source inverter with fundamental switching frequency is proposed. The proposed topology is constructed of 12 power switches and 12 diodes to achieve a three-phase five-level AC Y-connected output. The output line-to-line voltage is five levels and total harmonic distortion is lower. Multilevel inverters are used in the place where filters are not required and less harmonics are needed. Compared to the traditional three-phase inverters, the proposed three-phase five level inverter can achieve the five output voltage levels with fewer components. In this paper, the details of the mode analyses and control schemes are discussed. An experimental prototype with input voltage 500 V, output power 6 kW, THD 3.62%, and efficiency 98.40% is implemented to verify the theory and feasibility of the proposed topology.*

Keywords- Multilevel Inverter, Inverter, Three-phase, Mat lab.

I. INTRODUCTION

With the energy crisis all over the world, renewable energy systems are now widely set up to provide energy to the utility grid. Along with the green energy systems getting widely spread, the interface between generators and utility grid becomes much more important than before [1]-[7]. Three phase topology has the advantage of high power density. And three-phase inverter can be used to drive motors directly as well. However, the traditional interface such as half-bridge inverter and H-bridge inverter may not be able to transfer the power into the grid efficiently. In order to transfer the power to the utility grid more efficiently, multi-level inverters are presented. The multi-level inverters have the advantages as below [8]-[10]:

1) The ability to handle power in a wide range.
2) Low output harmonic distortions.
3) Low switching loss on power switches.
4) Low voltage and current stress on power switches.

The first type is diode-clamped and capacitor-clamped inverter. The voltage stress of switches can be clamped by diodes. However, the higher output voltage levels, the more power components and diodes are needed. Thus, the reverse recovery time problem of diodes will lead to serious total harmonic distortion. Besides, the voltage balanced problem cannot avoid in high power applications [9]-[12]. Capacitor clamped inverter can be used to clamp the voltage stress of switches and solve voltage balance problem. However, the energy is passed by parallel connected capacitor. In high power applications, the efficiency is not good enough [9].

The second type of multi-level inverter based on H-bridge inverters is proposed. H-bridge inverters are used in cascade way. By cascading the H-Bridge Inverter, the output voltage can achieve multi-level. The more output voltage levels are needed, the more H-bridge inverters are added. However, each H-bridge inverters requires one independent and isolated source, and the numbers of source increase as the output levels get higher [9], [14]-[18].

The third type of multi-level inverter is to change the voltage of the terminal. Thus, the different voltage levels can be composed [21], [22]. The reverse recovery problem cannot avoid. Also, the conduction loss is decided by diode and switch. Compared with previous topologies, simplified multilevel inverter can achieve the same output levels with ZVS and loss reduced is proposed [24]-[26]. The concept of bidirectional circuit and floating neutral point are implemented together to achieve multi-level output. This topology is simple, easy to design, and the control system would not be so complicated.

Among the topologies introduced above, each circuit has its characteristics. The voltage stress on power switches would be clamped to the input capacitors and clamping capacitors in diode-clamped and capacitor-clamped inverter, and this would make the selection of switches become much easier. However, the cumbersome number of diodes,

capacitors and power switches would cause the whole system hard to design as the output levels get higher. Cascaded H-bridge inverter would need multi-sources when the output levels increase, however, the simple characteristic make this topology easy to design. At the simplified multi-level inverter, it implements the concept of bidirectional auxiliary circuit. By connecting the auxiliary circuit to the conventional H-bridge inverter, fewer components are needed at the same output voltage levels [9]-[18], [21]-[26].

To simplify the complexity of multi-level inverters, a near sinusoidal three phase five level voltage source inverter with fundamental switching frequency is presented. With the bidirectional auxiliary circuit being combined with the traditional three-phase six-switch inverter, this topology can achieve the same levels as the conventional multi-level topologies in minimum power elements numbers. The auxiliary circuit is only composed of six switches and six diodes. The control scheme is also easier and high power density. The proposed topology has been experimented with fundamental switching frequency scheme.

II. OPERATION OF PROPOSED INVERTER

The proposed inverter is shown in Fig. 1, which only needs one input voltage source, and consists of two series capacitors which are parallel with input voltage source, 12 switches, and 12 diodes. The diodes D1, D2, D3, switches S10, S11, and S12 provide routes for Vdc/2. Because the switches used in this paper would be turned on by inverse voltage over 30 V, it needs the diodes D4, D5, and D6 to prevent the switches S10, S11, and S12 from turning on during the wrong time. The line-to-line voltages Vab, Vbc, and Vca are five-level, Vdc, Vdc/2, 0, -Vdc/2, -Vdc. The phase-to-neutral voltages Van, Vbn, and Vcn are seven-level, 2Vdc/3, Vdc /2, Vdc /3, 0, -Vdc /3, -Vdc /2, and -2 Vdc /3.

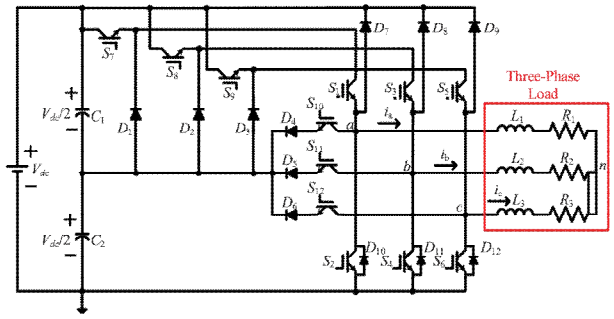


Figure 1. Proposed Three-Phase Five-Level Inverter Topology.

A. Fundamental Switching Frequency Control Scheme

Fig. 2 shows the mode of operation. This control scheme has twelve modes, and each mode is 30 degrees. The following analyses are based on the assumptions that the volumes of the capacitors C1 and C2 are big enough as two voltage sources equal to Vdc/2. All of the switches and diodes are ideal. Fig. 3 shows the status of the switches. The switching frequency is 50Hz.

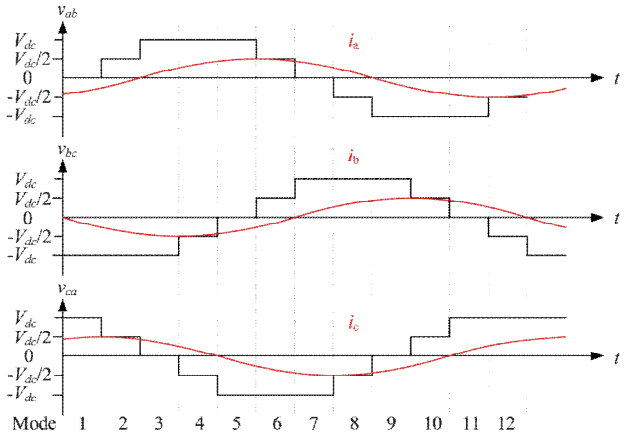


Figure 2. Mode of operation.

Mode 1: In this mode, the current ia is negative, ib is negative, and ic is positive shown as Fig. 4a. The switches S2, S4, S5, and S9 are on. The voltage of the node a is 0 V, the node b is 0 V, and the node c is Vdc. The output line-to-line voltage Vab is 0 V, Vbc is –Vdc, and Vca is Vdc. In order to prevent voltage spike during the dead time of S1 and S2 in next mode, turn on S10 to provide a route for inductor current.

Mode 2: In this mode, the current ia is negative, ib is negative, and ic is positive shown as Fig. 4b. The switches S4, S5, S9, and S10 are on. The diode D4 is on. Although S1 is turned on, the switch S10 and the diode D4 are on and S1 is off because the current ia is negative. The voltage of the node a is Vdc/2, the node b is 0 V, and the node c is Vdc. The output line-to-line voltage Vab is Vdc/2, Vbc is –Vdc, and Vca is Vdc/2. The capacitor C1 releases power to load in this mode

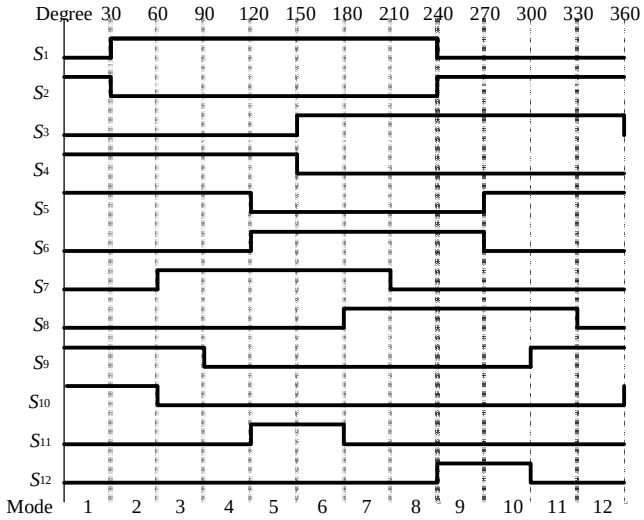


Figure 3. Switches status.

Mode 3: In this mode, the current ia is positive, ib is negative, and ic is positive shown as Fig. 4c. The switches S1, S 4, S5, S7, and S9 are on. The voltage of the node a is Vdc, the node b is 0 V, and the node c is Vdc. The output line-to-line voltage Vab is Vdc, Vbc is –Vdc, and Vca is 0 V.

Mode 4: In this mode, the current ia is positive, ib is negative, and ic is positive shown as Fig. 4d. The switches S1, S4, S5, and S7 are on. The diode D3 is on. The voltage of the node a is Vdc , the node b is 0 V, and the node c is Vdc/2. The output line-to-line voltage V ab is Vdc, Vbc is –Vdc/2, and Vca is Vdc/2. The capacitor C2 releases power to load in this mode.

Mode 5: In this mode, the current ia is positive, ib is negative, and ic is negative shown as Fig. 4e. The switches S1, S4, S6, and S7 are on. The voltage of the node a is Vdc, the node b is 0 V, and the node c is 0 V. The output line-to-line voltage V ab is Vdc, Vbc is 0 V, and Vca is -Vdc. In order to prevent voltage spike during the dead time of S 3 and S4 in next mode, turn on S11 to provide a route for inductor current.

Mode 6: In this mode, the current ia is positive, ib is negative, and ic is negative shown as Fig. 4f. The switches S1, S6, S7, and S11 are on. The diode D5 is on. Although S3 is turned on, the switch S11 and the diode D5 are on and S3 is off because the current ib is negative. The voltage of the node a is Vdc, the node b is Vdc/2, and the node c is 0 V. The output lineto-line voltage Vab is Vdc/2, Vbc is Vdc/2, and Vca is -Vdc. The capacitor C1 releases power to load in this mode.

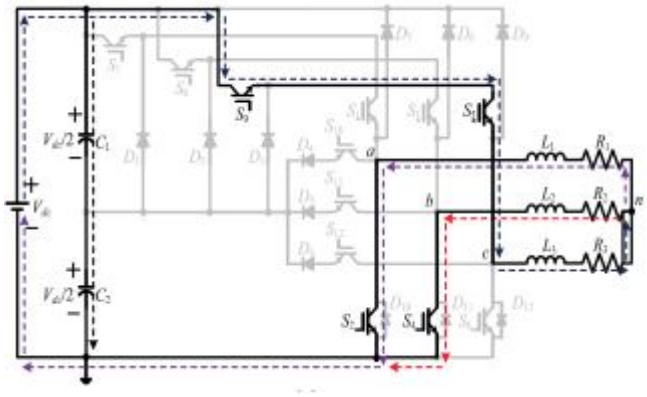
Mode 7: In this mode, the current ia is positive, ib is positive, and ic is negative shown as Fig. 4g. The switches S1, S3, S6, S7, and S8 are on. The voltage of the node a is Vdc, the node b is Vdc, and the node c is 0 V. The output line-to-line voltage Vab is 0 V, Vbc is Vdc, and Vca is –Vdc.

Mode 8: In this mode, the current ia is positive, ib is positive, and ic is negative shown as Fig. 4h. The switches S1, S3, S6 and S8 are on. The diode D1 is on. The voltage of the node a is Vdc /2, the node b is Vdc, and node c is 0V.the output line-to-line voltage Vab is - Vdc /2 , Vbc is Vdc, and Vca is Vdc /2. The capacitor C2 releases power to load in this mode.

Mode 9: In this mode, the current ia is negative, ib is positive, and ic is negative shown as Fig. 4i. The switches S2, S3, S6 and S8 are on. The voltage of the node a is 0V, the node b is Vdc, and node c is 0V.the output line-to-line voltage Vab is - Vdc, Vbc is Vdc, and Vca is 0V. In order to prevent voltage spike during the dead time of S5 and S6 in next mode, turn on S12 to provide a route for inductor current

Mode 10: In this mode, the current ia is negative, ib is positive, and ic is negative shown as Fig. 4j. The switches S2, S3, S8 and S12 are on. The diode D6 is on. Although S5 is turned on, the switch S12 and the diode D6 are on and the switch S5 is off because the current ic is negative. The voltage of the node a is 0V, the node b is Vdc, and node c is Vdc /2.the output line-to-line voltage Vab is - Vdc, Vbc is Vdc /2, and Vca is Vdc /2. The capacitor C1 releases power to load in this mode.

Mode 11: In this mode, the current ia is negative, ib is positive, and ic is positive shown as Fig. 4k. The switches S2, S 3, S5, S8, and S9 are on. The voltage of the node a is 0V, the node b is Vdc, and the node c is Vdc. The output line-to-line voltage Vab is -Vdc, Vbc is 0V, and Vca is Vdc. Mode 12: In this mode, the current ia is negative, ib is positive, and ic is positive shown as Fig. 4l. The switches S2, S 3, S5 and S9 are on. The diode D2 is on The voltage of the node a is 0V, the node b is Vdc /2, and the node c is Vdc. The output line-to-line voltage Vab is -Vdc/2, Vbc is -Vdc/2, and Vca is Vdc. C2 releases power to load in this mode.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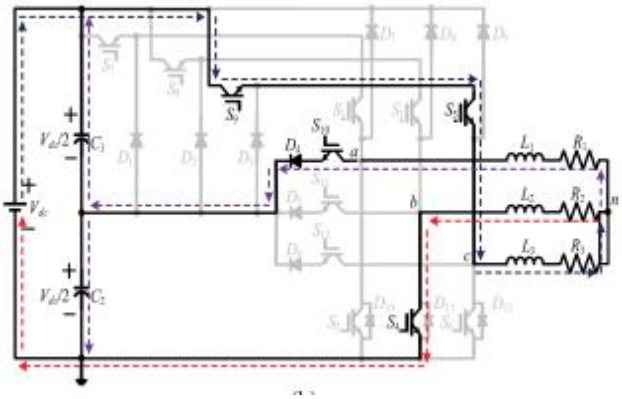

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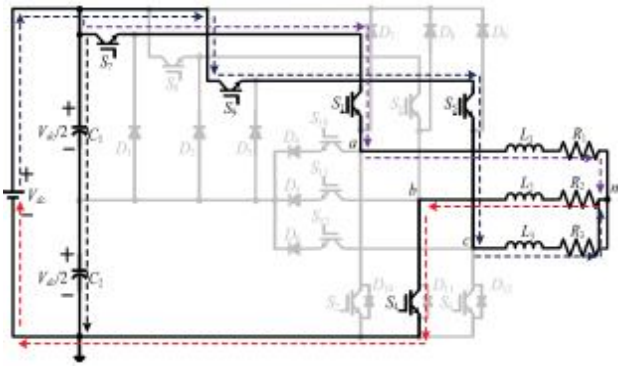

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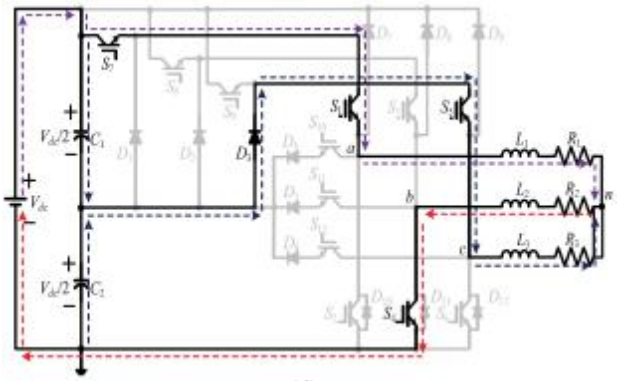

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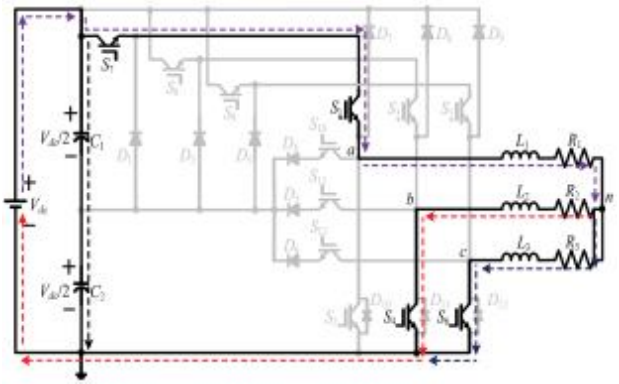

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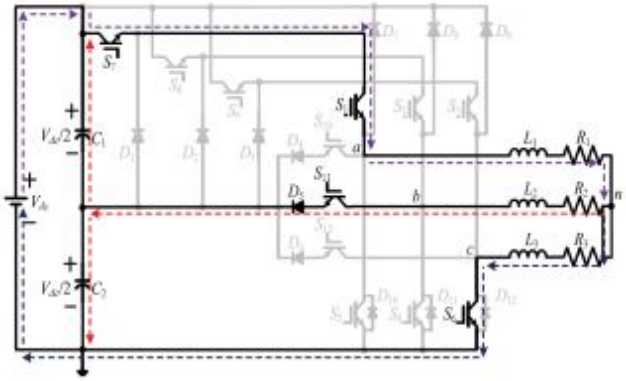

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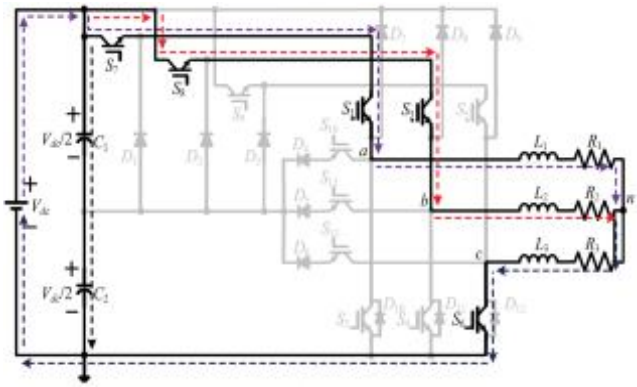

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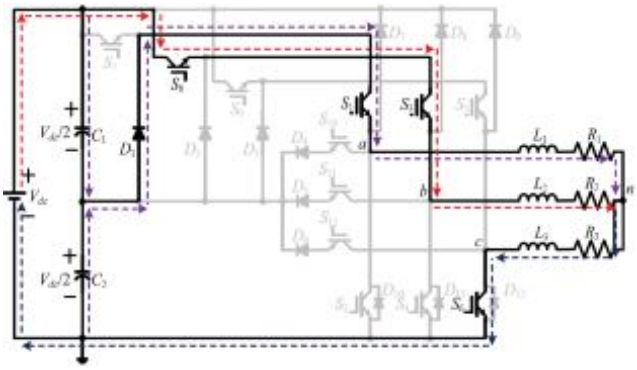

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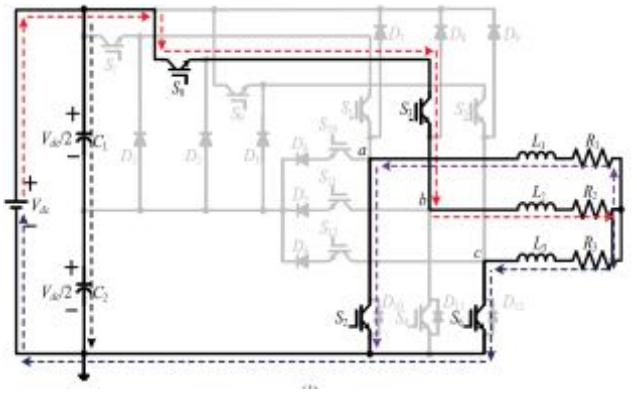

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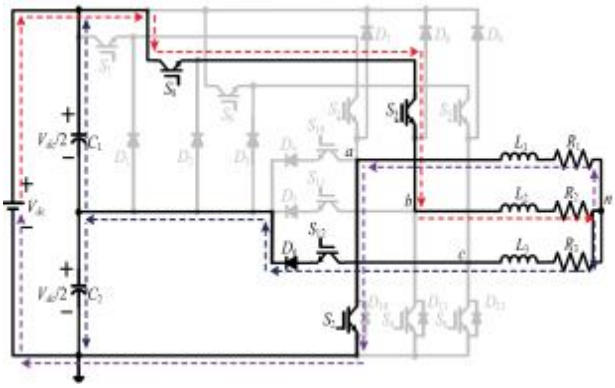

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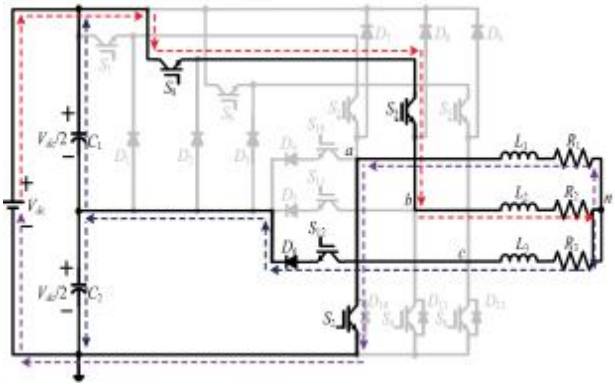

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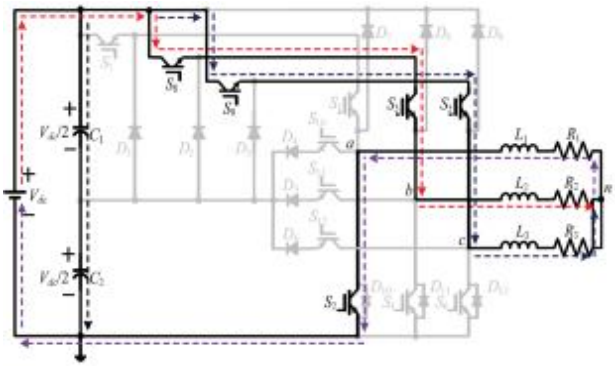

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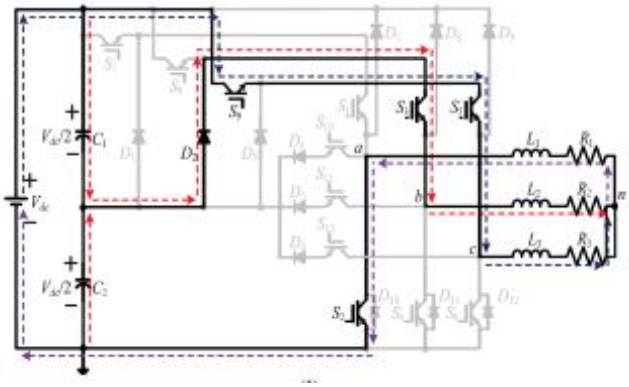

Figure 16.

Fig 4: Fundamental switching frequency control scheme Mode analysis. (4) Mode 1. (5) Mode 2. (6) Mode 3. (7) Modes 4. (8) Mode5. (9) Modes 6. (10) Modes 7. (11) Mode 8. (12) Mode 9. (13) Mode 10. (14) Mode 11. (15) Mode 12.

$$RMS = \frac{1}{T}\sqrt{\int_0^T f(x)^2 dt} \quad \text{.....(1)}$$

III. SIMULATION RESULTS OF THE PROPOSED INVERTER

Before experiment, the proposed topology was simulated by MATLAB. Fig. 5 and Fig. 6 are the simulation results of fundamental switching frequency control scheme. Fig. 5 shows the output line-to-line voltage waveforms Vab, Vbc, and Vca when the output power is 6 kW. Fig. 6 is the output phase-to-neutral voltage waveforms phase a, b, and c. Table I is the circuit specification, and Table II is the specifications.

In order to let output line-to-line voltage become sinusoidal, a low pass filter was designed with filter frequency 240Hz. By adding a filter capacitor along with the load inductor which is 20mH, the filter capacitor can be derived by equation (2).

$$C = 1 / 4\pi^2 f^2 L \quad \text{.....(2)}$$

Table 1. CIRCUIT SPECIFICATION

Control schemes / Characteristic	Fundamental switching frequency
Input voltage	500 V
Output voltage	380 V_{rms}
Switching frequency	50 Hz
Max. output power	6 kW

Table 2. SIMULATION ELECTRIC PARAMETERS

Control schemes / Characteristic	Fundamental switching frequency
C_1~C_2	330 μF, 315 V
S_1 ~ S_{12}	IXGH32N60A 600 V, 60 A
D_1 ~ D_{12}	DSEP30-06A 600 V, 30A
L_1 ~ L_3	20 mH

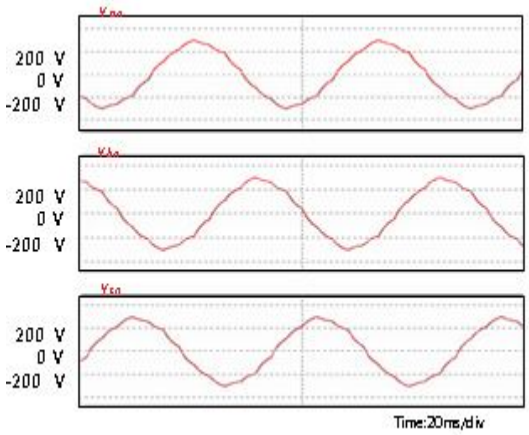

Figure 17. The output line-to-line voltage

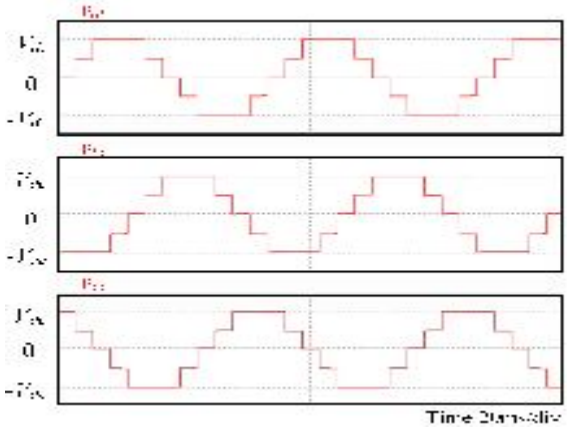

Figure 17. The output phase-to-neutral voltage

The simulation results have verified that the proposed inverter can reduce the THD effectively. The THD of filtered output current is 4.3% at the maximum output power 6 kW by using fundamental switching frequency control scheme.

IV. EXPERIMENTAL RESULTS OF PROPOSED INVERTER

After simulating, a prototype circuit was implemented to verify the performance of proposed multi-level inverter. The electric parameters are the same as we used in simulation. Fig. 7 and Fig. 8 are the experimental results of fundamental switching frequency control scheme. Fig. 7 is the output line-to- line voltage waveforms Vab, Vbc, and Vca. Fig. 8 is the output phase-to-neutral voltage and current waveforms. The experimental results of fundamental switching frequency control scheme are shown in table III

The experimental results have verified that the proposed inverter can reduce the THD effectively. The filtered THD is 3.62% at the maximum output power 6 kW. The maximum efficiency of the proposed inverter is 99.1% at 300W and the efficiency is above 98.40% under all load conditions.

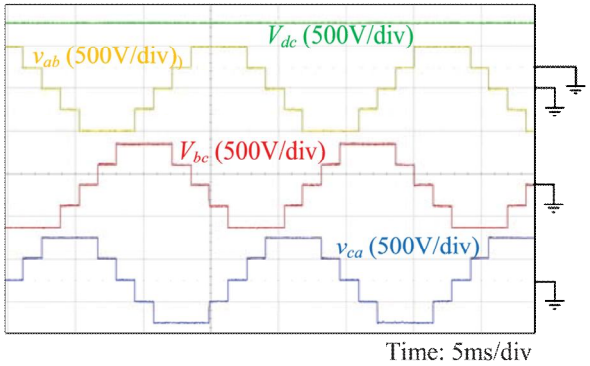

Figure 18. The output line-to-line voltage waveforms vab, vbc, and vca

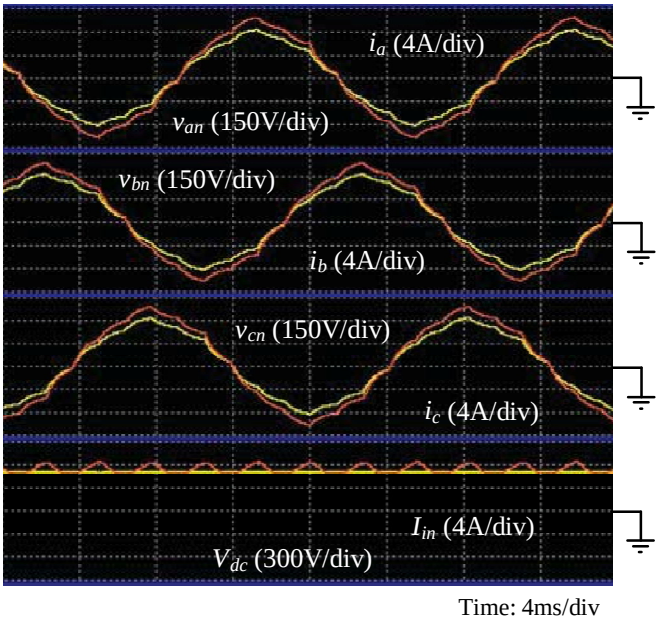

Figure 8. The output phase-to-neutral voltage and current waveforms.

Table 3. THE EXPERIMENTAL RESULTS

V_{dc}	500V					
V_o	380V_{rms}					
P_{in} (kW)	3.00	4.30	4.90	5.13	5.51	6.32
P_o (kW)	2.97	4.25	4.84	5.06	5.43	6.22
(%)	99.10	98.96	98.83	98.77	98.52	98.40

V. CONCLUSION

By adding auxiliary circuit to the three-phase six-switch inverter, less power components need to be used to achieve the same levels as other topologies. And the proposed topology don't have unbalance problem so that the control scheme are simpler and power density is higher. The experiment results show that the proposed inverter can achieve low THD and provide higher power. The maximum efficiency of the proposed inverter is 99.1% at 300W and the filtered THD of output current is 4.3% at the maximum output power 6 kW.

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