Design of Fast And Low Complexity Fault Tolerant FFTS Using Parseval Check

Dr.G.Vetrichelvi[1], S.Sandra[2]
[1, 2] Department of ECE
[1, 2] Jansons Institute of Technology, Coimbatore.

Abstract- *In most of the recent processors , multimode memory unit is used which needs digital filters to avoid unwanted faults in the process components and in some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. A soft error is an issue that causes a temporary condition in RAM that alters stored data in the FFT. First method, the Parity-Partial Summation and Error Correction Codes (ECC) uses one FFT with minimum Partial Sum blocks for reducing hardware area. Parallel Partial Summation ECC used for correcting errors in multiple FFTs protective methods. The result for 4-paralle1 FFTs shows that the proposed technique effectively reduces delay of fault tolerant design by detecting and correcting the multiple errors at a time. The existing methods used the methods to detect and correct the single error in FFT. We have proposed partial summation method to detect and correct multiple errors simultaneously. The result for proposed method shows that it effectively reduces the timing process in detecting and correcting the errors in FFT.*

I. INTRODUCTION

The general idea for achieving error detection and correction is to add some redundancy to a message, which receivers can use to check the originality of the transferred message. Even cosmic rays can cause the soft errors from time to time in the system. System-level errors may be caused by power issues, running out of specification (overclocked too far, for example) and software issues that occur when memory is written to incorrectly. Error detection was required, a receiver can simply apply the algorithm to the data bits received and its output was compared with the check bits received. The error control performance requires the data to be selected based on the characteristics of the communication channel. The CMOS technology scaling has made to designs more complex because of the induced soft errors. Automatic repeat request (ARQ) is mostly used in the internet.

Hamming codes are a family of linear error-correcting codes were invented by Richard Hamming in 1950.Hamming codes can able to detect up to two-bit errors or correct one-bit errors without correcting the faults in the system. Fourier analysis converts a signal from its tree value to a representation in the frequency domain and vice versa. Fast Fourier transforms are widely used for many applications in engineering, science, and mathematics. There are many different FFT algorithms involving a wide range of mathematics, from simple number to complex group theory and number theory.

The best-known FFT algorithms depend upon the factorization of N, but there are FFTs with O(N log N) complexity for all N, even for prime N. Many FFT algorithms only depend on the fact that is an N-th primitive root of unity, and thus can be applied to analogous transforms over any finite field, such as number-theoretic transforms. Since the inverse DFT is the same as the DFT, but with the opposite sign in the exponent and a 1/N factor, any FFT algorithm can easily be adapted for it. The FFT's used in this method is the decimation in frequency FFT.

This paper explains about the fast fourier transform and hamming codes in the starting of the paper. The second part explains about the related works of the paper and then the proposed method called partial summation method is explained in detail. The third part gives the explanation of the results and discussion part and the conclusion has given about the paper. The references used for this paper has given in the order based on the related works.

II. RELATED WORKS

Zhen Gao, Pedro Reviriego, Zhan Xu, Xin Su, Ming Zhao, Jing Wang, and Juan Antonio Maestro explained the two improved protection schemes that combine the use of error correction codes and parseval checks are proposed and evaluated [1]. Zhen Gao, Pedro Reviriego, Wen Pan, Zhan Xu, Ming Zhao, Jing Wang, and Juan Antonio Maestro explained the new scheme allows more efficient protection when the number of parallel filters is large[2].S.Sandra, Dr.G.Vetrichelvi has surveyed the error correction and detection method compared with the existing work[3]. Xin Fan explained the algorithm based on a multi-dimensional index mapping method but the algorithm also reduces the memory requirement for twiddle factors[4]. Abdelmohsen Ali and Walaa Hamouda explained the inverse fast Fourier

transform (IFFT)/FFT processor for single-user and multi-user multiple-input multiple-output orthogonal frequency-division multiplexing but less power is needed in our design compared with traditional software approach [5]. Jigisha Patel, Neeta Chapatwala and Mrugesh Patel explained that Low Density Parity Check (LDPC) codes have excellent error correcting performance it suggests parity check matrix of very small number of non-zero elements comparing with zero elements [6]. Hoyoung Tang and Jongsun Park explained the low-complexity unequal-error-protection error correcting code (UEEP-ECC) approach for the embedded memories in digital signal processor it achieves power savings and data quality [7]. Riaz Naseer, Rashed Zafar Bhatti, Jeff Draper explained the algorithm of Single Error Correction(SEC) Hamming code and Triple Modular Redundancy (TMR) provide a high-level mitigation solution for soft errors [8]. J.C. Fabre explained the algorithm for improving fault-tolerance in distributed systems using saturation method but it has the disadvantage of time complexity [9]. John M.C. Porcello explained the model of Low Density Parity Check correct the fault FFT. At a time single error can be detected and (LDPC) Codes offer remarkable error correction performance corrected because of this issue it has disadvantage of time delay. and therefore increase the design space for communication. The Parity-SOS-ECC fault-tolerant parallel FFTs is shown in systems [10]. Byonghyo Shim and Naresh R. Shanbhag the model explained the as algorithmic soft error-tolerance (ASET), employs low-complexity estimators of a main DSP block to achieve reliable operation in the presence of soft errors [11]. S. Sri Jamiya, Dr. P. G. Kuppusamy, P. Balavenkateshwarlu, and J. T. Arun Ragesh explained the FFT module using redundant module but it has disadvantage of power consumption [12].

III. PROPOSED METHOD

ERROR DETECTION AND CORRECTION BY PARTIAL SUMMATION METHOD

In this method, we use the parseval check method as the base method to check the fault. This method detects more than one error in the module. Then we use the parallel FFT redundant modules to correct those faults in FFTs. The values of two FFT is not same there is a fault in that FFT. In this method, parseval check module is enough to detect the faults in the FFTs and so there is no need for additional detection circuits the method is explained in the Fig 1. The expected result of this method reduces the timing because it detect and correct the two faults in a single process.

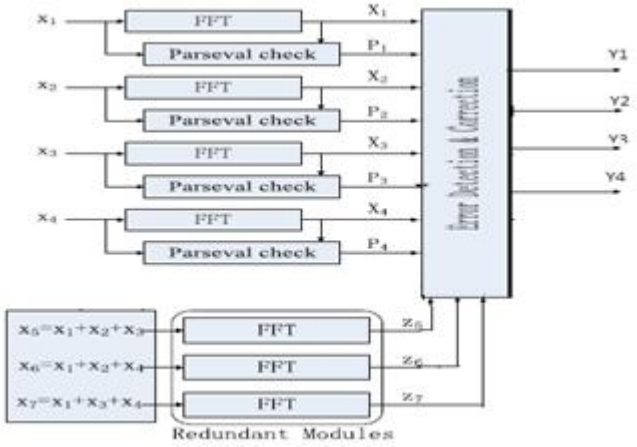

Figure 1. Partial Summation Method

For example, the binary values like are given as input and the output values are combination real and imaginary values showed in Fig 2. When, we add all the four input values the binary value we get was 01010.The fault free FFT gives the output value 01010 and if suppose due noise or any other problem the output data received is not equal to the transferred data sum of values then there fault occurs the fault FFT gives the value 01001.

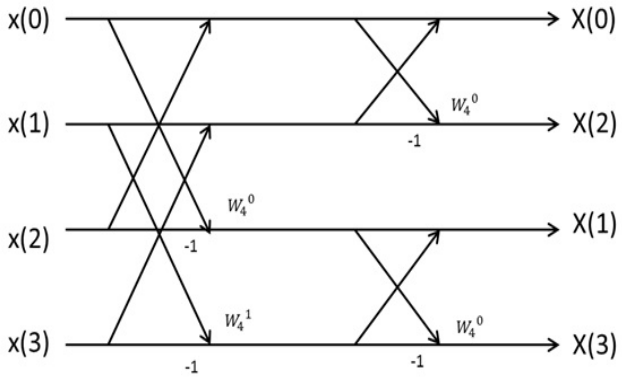

Figure 2. 4-point butterfly diagram

The starting point for our work is the protection scheme based on the use of ECCs and partial summation method that was presented in [1] for digital filters. The proposed scheme is shown in Fig.1. X5 is the output of summation three inputs x1,x2 and x3.In this example, a multiple error correction Hamming code is used. For example, the input the first redundant module is

X5 = x1 + x2 + x3

The output of the first redundant module z5, z6, z7 can be used to check the first module output X1,X2,X3 and X4.

z5=X1+X2+X3

z6=X1+X2+X4
z7=X1+X3+X4

Once the module errors are known, the errors can be corrected by reconstructing its output using the remaining modules. For an errors affecting X2 and X3, this can be done as follows

X2= z6-X1-X4
X3=z5-X1-X2

IV. RESULTS AND DISCUSSIONS

The result of the proposed method is being compared with the existing method by using Flip Flops and LUT parameters. The values and counts have been compared with the benchmark parameter and the advantage and disadvantage has been discussed in both the proposed and existing method. The disadvantage of the existing method was if the single FFT has the fault in it the whole process takes and then only we can able to find the fault in the received data because of this method the power, counts and other benchmark parameters are wasted and again the new process is started to receive the fault free data.The benchmark parameters are discussed in the Table 1.

Table 1. Comparison of Benchmark parameters

Parameters	Flip flops	LUT
ECC(Existing Method [1])	392	236
Parity-SOS (Existing Method [1])	612	508
Parity-SOS-ECC (Existing Method[1])	419	331
Partial Summation (Proposed method)	263	253

The input to the four FFT has been given as x1, x2, x3 and x4.The input of the FFT has given to the partial summation block and the FFT is checked parallely. The sum of squares input and output must be same for fault free FFT. The sum of squares of input and output are not same then the fault exist in the particular FFT.

V. CONCLUSION

The parallel FFTs implementation against soft errors has been surveyed and different methods has been used and checked. Two techniques have been evaluated. The proposed techniques are based on combining an existing ECC approach with the traditional SOS check. The SOS checks are used to detect and locate the errors and a simple parity FFT is used for correction. The detection and location of the errors can be done using an SOS check per FFT or alternatively using a set of SOS checks that form an ECC. The SOS checks are used to detect and locate the errors and a simple parity FFT is used for correction. The proposed method includes the method of finding the multiple fault in FFT's and correcting the multiple fault in FFT's. The partial summation method is used to detect the error in FFT and ECC method to correct the error in fault FFT. The proposed method has the disadvantage of power consumption and gate count but the delay is reduced.

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