A Review on Hybrid Topology Based DSTATCOM For Reactive And Nonlinear Load Compensation

Mr. Satish S. Tambe[1], Mr.E Vijay Kumar[2], Mr. Vivek Yadav[3]
[1, 2, 3] Department of Electrical Engineering
[1, 2, 3] RKDF group of institute, RGPV Bhopal (M.P.)

Abstract- *A distribution network of power system comprises of nonlinear load which affects the power quality by giving rise to many issues such as waveform distortion, voltage variations, flickers etc. A distribution static compensator was introduce recently to compensate such nonlinear load at distribution side. Further, many of researchers go through various topologies of DSTATCOM to improve performance and to reduce size, switching losses, power rating and etc. This paper reviews the hybrid DSTATCOM topology in which a series capacitor is added with coupling inductor to reduce DC link voltage rating without compromising the compensating performance. With reduce DC link voltage, the average switching frequency (ASF) of power electronic devices reduces and gives better reference tracking performance. With reference to hybrid topology the detailed survey for proposed entitled work is carried out in this paper.*

Keywords- Average Switching Frequency (ASF), DC link voltage, Distribution Static Compensator (DSTATCOM), Hybrid DSTATCOM topology, Nonlinear Loads.

I. INTRODUCTION

The poor power quality results in failure or misoperation of electrical equipment or machines which adds economic burden on consumer and ultimately it affects the productivity and growth of any nation. So as to resolve power quality problems a passive components like static capacitors, passive filters were used recently. But it has many drawbacks such as fixed compensating performance [1]. The development in power electronic devices (PEDs) provided a wide scope for Flexible AC transmission system (FACTS) controller. The improved switching performance with required rating is one of the development in PEDs. The proper arrangement of such PEDs and DC storage element such as capacitor forms voltage source converter (VSC). The application of such VSC based arrangement through coupling inductive element at PCC (point of common coupling) forms FACTS controller termed as DSTATCOM [2-8]. It injects harmonic and reactive components of load current in the PCC to make source currents and voltage balance and sinusoidal. The traditional DSTATCOM topology uses high rated VSC. The rating of VSC is directly proportional to the DC link voltage [9]. With increase in DC link voltage the power rating of VSC increases with increase in rating of PEDs, which makes it heavy, costly and oversized. Also the inductor is used to form L-type filter interface with PCC in traditional DSTATCOM topology for making the injected component sinusoidal which, in turn, has low slew rate for reference current tracking. It causes the large voltage drop across inductor and hence the higher value of DC link voltage is required to achieve better compensation. This will again adds in the cost, size and rating of L-type interfaced inductor [10-11] and [13].

To achieve satisfactory compensation the value of C link voltage should be maintained at much higher value than the Peak value of phase voltage (in three phase four wire system) or phase voltage (in three phase three wire system) [2] and [12-15]. Hence, based on the applications many researchers have used higher value of DC link capacitors for their study.

In this paper, a new DSTATCOM topology with reduced dc- link voltage is proposed. The topology consists of two capacitors: one is in series with the interfacing inductor and the other is in shunt. The series capacitor enables reduction in dc-link voltage while simultaneously compensating the reactive power required by the load, so as to maintain unity power factor without compromising DSTATCOM performance. The shunt capacitor, along with the state feedback control algorithm, maintains the terminal voltage to the desired value in the presence of feeder impedance.

II. CONVENTIONAL AND HYBRID DSTATCOM TOPOLOGY

The neutral clamped voltage source converter (VSC) topology based DSTATCOM is considered as conventional topology for the study [12]. The power circuit for conventional topology is shown in fig1. Here, V_{sa}, V_{sb} and V_{sc} are the voltages of source of phases a,b and c, respectively. The terminal voltages at PCC are V_{ta}, V_{tb} and

V_{ta} with respect to phases a, b and c, respectively. The respective phase source currents are represented by i_{sa}, i_{sb} and i_{sc}. Similarly, i_{la}, i_{lb} and i_{lc} are the load currents and i_{fa} i_{fb} and i_{fc} are the shunt active filter currents. The current in the neutral leg is represented by i_0. The feeder inductance (L_s) and resistance (R_s) with interfacing inductance (L_f) and resistance (R_f) are shown in circuit of fig 1. This topology uses two dc storage devices. Also in this topology each leg of VSC can be controlled independently. As compared to other VSC topology the current tracking is smooth with less number of switches [16]. Proper design of VSI gives better tracking performance, so the most important parameters such as DC link voltage (V_{dc}), DC storage device (C_{dc}), interfacing inductance (L_f) and switching frequency (f_{sw}) must be taken into consideration while designing conventional VSC. Author in [17] gives the detailed procedure of VSC design.

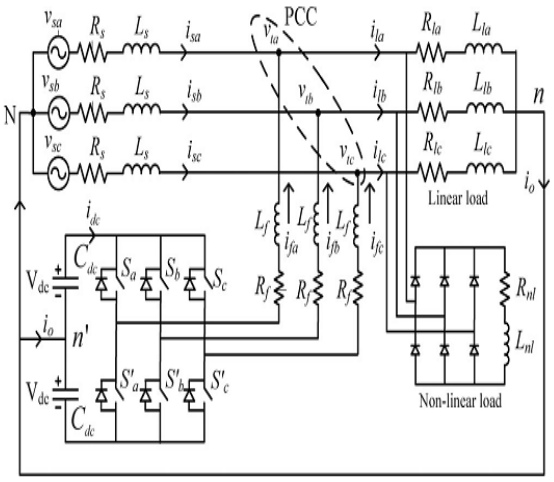

Figure 1. Neutral clamped VSI- based conventional DSTATCOM Topology

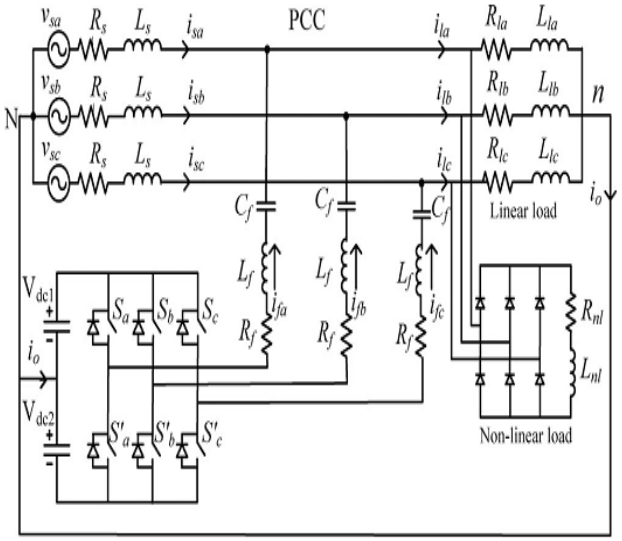

Figure 2. Neutral clamped VSI- based Hybrid DSTATCOM Topology

Fig. 2 shows the equivalent circuit of the proposed neutral clamped VSI topology-based DSTATCOM. It is a combination of the conventional DSTATCOM topology with a capacitor Cf in series with the interfacing shunt branch of the active filter and a capacitor Csh in shunt with the active filter. This topology is referred to as hybrid topology. The passive capacitor Cf has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load. The addition of capacitor in series with the interfacing inductor of the conventional topology will significantly reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. This concept will be illustrated with analytic description in the following section. The shunt capacitor Csh largely eliminates the switching frequency components of the VSI in the terminal voltages and source currents using state feedback control. The design of the series capacitor Cf and the shunt capacitor Csh have significant effect on the performance of the compensator [12]. The parameters chosen for conventional VSC topology in this study by [12] are based on following expressions.

The value of DC storage device i.e DC link capacitor is given by,

$$C_{dc} = \frac{\left(2X - \frac{X}{2}\right) nT}{(1.8V_m)^2 - (1.4V_m)^2} \quad \textbf{(1)}$$

Where,

V_m= Peak value of source voltage.

X= the kVA rating of system.

n= number of cycles.

T= the time period of each cycle.

$$L_f = \frac{1.6V_m}{4hf_{swmax}} \quad (2)$$

Where,

$$h = \sqrt{\frac{k_1}{k_2}\frac{(2m^2-1)}{4m^2 f_{swmax}}} \quad (3)$$

Where,

$$m = \frac{1}{\sqrt{1 - f_{swmin}/f_{swmax}}} \quad (4)$$

k_1 &k_2 =Proportionality constants.

f_{swmax} = maximum switching frequency

f_{swmin} = minimum switching frequency

The DC link voltage reference (V_{dcref}) of conventional VSI topology taken as $1.6V_m$ for each capacitor [16-18]. Using instantaneous symmetrical component theory the reference currents are generated [12] and [18]. Also the control circuitry is simple for this topology as on three commands for switching are generated along with the complementary signals to control all switches of converter [12].

III. PERFORMANCE ANALYSIS

The author [12] carried out simulation using a power systems computer-aided design (PSCAD) simulator. The results are plotted and discussed in [12]. In this section the theoretical and comparative analysis between traditional or conventional DSTATCOM topology and Hybrid DSTATCOM topology is discussed.

Before compensation, the load currents are unbalanced and distorted; the terminal voltages are also unbalanced and distorted because, these load currents flow through the feeder impedance in the system.

When the DSTATCOM using conventional topology is used for compensation, the source get balanced and sinusoidal. But these currents contain the switching frequency of the inverter. The dc-link voltage across both capacitors is maintained constant to the reference value.

With the compensation using hybrid DSTATCOM topology the dc-link voltage is found to be decreased than that of conventional topology. In hybrid topology, the peak to peak voltage across inductor is far lower than the voltage across the inductor using the conventional topology. As the voltage across the inductor is high in case of the conventional topology, the rate of rise of filter current dif /dt will be higher than that of the proposed topology. This will allow the filter current to hit the hysteresis boundaries at a faster rate and increases the switching, whereas in hybrid topology, the number of switching will be less. Thus, the average switching frequency of the switches in the hybrid topology will be less as compared to the conventional topology. Since the average switching is less, the switching loss will also decrease in the hybrid topology. One more advantage of having less voltage across the inductor is that the hysteresis band violation will be less. This will improve the quality of compensation and total harmonic distortion (THD) will be less in the hybrid topology.

IV. CONCLUSION

A hybrid DSTATCOM topology has been discussed in this paper, which has the capability of compensating the load at a lower dc-link voltage under nonstiff source. Theoretical comparative studies are made for the conventional and hybrid DSTATCOM topologies. From this study, it is found that the hybrid topology has less average switching frequency, less THDs in the source currents and terminal voltages with reduced dc-link voltage as compared to the conventional DSTATCOM topology. So, by making further modifications and hybridization in hybrid DSTATCOM topology may give better results in future.

REFERENCES

[1] S. Ostroznik, P. Bajec, and P. Zajec, “A study of a hybrid filter,” IEEE Trans. Ind. Electron., vol. 57, no. 3, pp. 935–942, Mar. 2010.

[2] A. Ghosh and G. F. Ledwich, Power Quality Enhancement Using Custom Power Devices. Norwell, MA, USA: Kluwer, 2002.

[3] H. Hu, W. Shi, Y. Lu, and Y. Xing, “Design considerations for DSPcontrolled 400 Hz shunt active power filter in an aircraft power system,” IEEE Trans. Ind. Electron, vol. 59, no. 9, pp. 3624–3634, Sep. 2012.

[4] B. Singh and S. Arya, “Back-propagation control algorithm for power quality improvement using DSTATCOM,” IEEE Trans. Ind. Electron., vol. 61, no. 3, pp. 1204–1212, Mar. 2014.

[5] B. Singh and S. Arya, "Implementation of single-phase enhanced phase locked loop-based control algorithm for three-phase DSTATCOM," IEEE Trans. Power Del., vol. 28, no. 3, pp. 1516–1524, Jul. 2013.

[6] J. Liu, P. Zanchetta, M. Degano, and E. Lavopa, "Control design and implementation for high performance shunt active filters in aircraft power grids," IEEE Trans. Ind. Electron., vol. 59, no. 9, pp. 3604–3613, Sep. 2012.

[7] M. Singh, V. Khadkikar, A. Chandra, and R. Varma, "Grid interconnection of renewable energy sources at the distribution level with power quality improvement features," IEEE Trans. Power Del., vol. 26, no. 1, pp. 307–315, Jan. 2011.

[8] A. Bhattacharya and C. Chakraborty, "A shunt active power filter with enhanced performance using ANN-based predictive and adaptive controllers," IEEE Trans. Ind. Electron., vol. 58, no. 2, pp. 421–428, Feb. 2011.

[9] R. Inzunza and H. Akagi, "A 6.6-kv transformerless shunt hybrid active filter for installation on a power distribution system," IEEE Trans. Power Electron., vol. 20, no. 4, pp. 893–900, Jul. 2005.

[10] R. Gupta, "Generalized frequency domain formulation of the switching frequency for hysteresis current controlled VSI used for load compensation," IEEE Trans. Power Electron., vol. 27, no. 5, pp. 2526–2535, May 2012.

[11] S. Karanki, N. Geddada, M. K. Mishra, and B. Kumar, "A DSTATCOM topology with reduced dc-link voltage rating for load compensation with nonstiff source," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1201–1211, Mar. 2012.

[12] B. Singh and S. Sharma, "Design and implementation of four-leg voltagesource- converter based VFC for autonomous wind energy conversion system," IEEE Trans. Ind. Electron., vol. 59, no. 12, pp. 4694–4703, Dec. 2012.

[13] P. Kanjiya, V. Khadkikar, and H. Zeineldin, "A noniterative optimized algorithm for shunt active power filter under distorted and unbalanced supply voltages," IEEE Trans. Ind. Electron., vol. 60, no. 12, pp. 5376–5390, Dec. 2013.

[14] S. Rahmani, N. Mendalek, and K. Al-Haddad, "Experimental design of a nonlinear control technique for three-phase shunt active power filter," IEEE Trans. Ind. Electron., vol. 57, no. 10, pp. 3364–3375, Oct. 2010.

[15] V. George and Mahesh K. Mishra, "DSTATCOM topologies for three phase high power applications," Int. J. Power Electron., vol. 2, no. 2, pp. 107–124, 2010.

[16] M. K.Mishra and K. Karthikeyan, "Design and analysis of voltage source inverter for active compensators to compensate unbalanced and non-linear loads," in Proc. Int. Power Eng. Conf., 2007, pp. 649–654.

[17] A. Ghosh and A. Joshi, "A new approach to load balancing and power factor correction in power distribution system," IEEE Trans. Power Del., vol. 15, no. 1, pp. 417–422, Jan. 2000.