Low Power Carbon Nano Tube Transistor based 8T Full Adder Using MTCMOS Technique

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Abstract- *In this article a low power carbon nano tube transistor based novel 10T full adder cell is designed. This design is simulated in 32nm technology node using H-SPICE simulator. In this article multi threshold technique is used, by which leakage power and leakage current of the circuit is compact. Here multiplexer based 8T full adder is used as a base circuit, then after applying the MTCMOS technique, a 10T full adder cell is designed.*

Keywords- MTCMOS, Carbon nano tube, H-SPICE, Leakage current, Leakage power etc.

I. INTRODUCTION

In this article the analysis of 1-bit 10T full adder cell is done. This cell is simulated in H-SPICE suit with 32 nm CNT technology. Here CMOS is replaced by carbon nano-tube (CNT) transistor. By using CNT the act of this circuit is highly improved in terms of leakage power, leakage current etc. The detailed discussion about the CNT transistor is completed in next section. The full adder cell used here, is made by using multiplexer and inverter circuits. That's why the size of this circuit is very nominal because it uses only 8 transistors. And then after applying MTCMOS technique on this circuit, a proposed design of 10 transistor full adder circuit with less leakage current and leakage power is finalized.

II. CARBON NANO TUBE

A carbon nanotube field-impact transistor (CNTFET) refers to a discipline-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes because the channel fabric in preference to bulk silicon inside the conventional MOSFET shape.First demonstrated in 1998, there have been major developments in CNTFETs since.

A carbon nanotube's band-gap is directly affected by its chirality and diameter. If those properties can be managed, CNTs could be a promising candidate for future nano-scale transistor devices. Moreover, due to the lack of obstacles in the best and hollow cylinder shape of CNTs, there may be no boundary scattering. CNTs are also quasi-1D substances in which handiest forward scattering and back scattering are allowed, and elastic scattering suggest free paths in carbon nanotubes are lengthy, usually on the order of micrometers. As a end result, quasi-ballistic transport may be found in nanotubes at distinctly lengthy lengths and coffee fields. Because of the strong covalent carbon–carbon bonding within the sp2 configuration, carbon nanotubes are chemically inert and are able to transport large amounts of electric current. In theory, carbon nanotubes are also able to conduct warmth nearly as well as diamond or sapphire, and due to their miniaturized dimensions, the CNTFET have to transfer reliably the usage of a lot much less energy than a silicon-based totally device.

III. MTCMOS

MTCMOS Technique when the physical design of the MTCMOS circuits is done, it is vital to keep in mind the large current flowing through the current preventing transistors in energetic mode and the electro-migration within the wires should be taken into consideration. The channel width is also very important due to the large current. There is a trade-off between the local and global sleep devices. The bottleneck with local sleep devices is that there will be a large area overhead due to the fact that there will be a lot of extra transistors.

The MTCMOS is easy on combinatorial circuits, but it can be difficult on sequential circuits. Should the power supply be turned off, all data stored in the circuit will be irreversibly lost. This is the main problem with MTCMOS circuits. To deal with this problem complex timing scheme must be used or extra circuits have to be added. Because of these added items the performance of the circuit would be degraded. This will also require a larger die area and impose higher power losses. MTCMOS (multithreshold CMOS) reduces leakage current during standby mode and attains high speed in active mode.

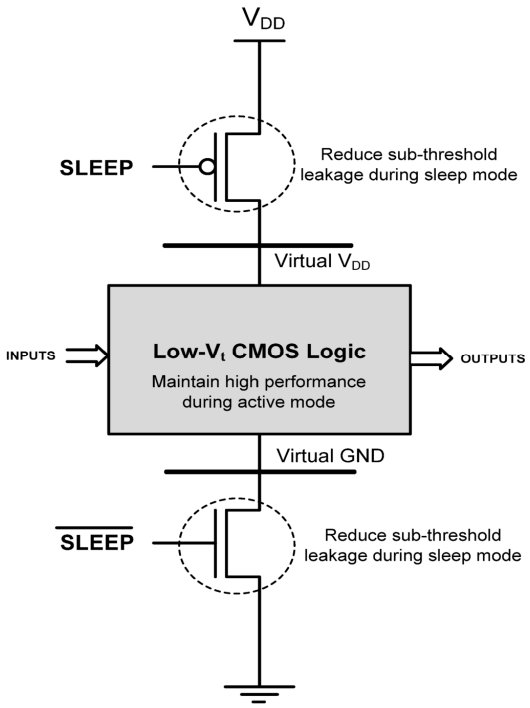

Figure 1. MTCMOS Technique.

In this technique high threshold voltage transistor are used to isolate the low threshold voltage transistor from supply and ground for the duration of standby mode. However by means of consisting of more transistor, MTCMOS circuit faces performance penalty compared to CMOS circuits, if the transistor aren't sized nicely.

The high threshold voltage transistor are turned off all through standby (sleep mode) , this result very low sub threshold passes from Vcc to floor. MTCMOS consists of high Vt transistor to gate energy and floor of a low Vt common sense blocks as shown in parent 1.Whilst the excessive Vt transistor are off ensuing in a completely low sub threshold leakage current. When the high Vt transistor are turned on, low Vt are connected to virtual ground and Vdd.

In this article implementation of MTCMOS technique on CNT transistor is takes place. By which very high improvement is seen in the results.

IV. 8T BASED FULL ADDER CELL

The full adder function can be described as follows: the addition of two 1-bit inputs A and B with forestage carry Cin calculates the two 1-bit outputs Sum and Cout, where

$$\text{Sum}=A\oplus B\oplus C_{\text{in}}, \quad (1)$$

$$C_{\text{out}}=A\cdot B+C_{\text{in}}\cdot(A\oplus B). \quad (2)$$

In our design, we rewrite the Boolean function as

$$\text{Sum}=(A\oplus C_{\text{in}})\cdot\overline{C_{\text{out}}}+\overline{A\oplus C_{\text{in}}}\cdot B, \quad (3)$$

$$C_{\text{out}}=(A\oplus C_{\text{in}})\cdot B+\overline{A\oplus C_{\text{in}}}\cdot A. \quad (4)$$

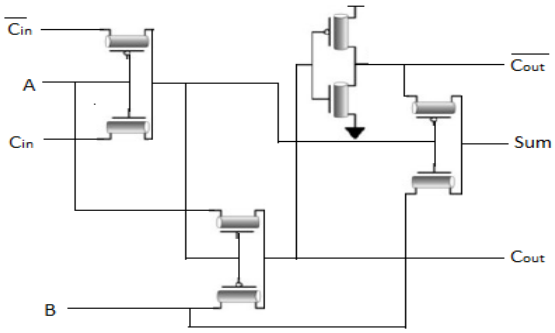

Figure 2. 8T CNT Based Full Adder Cell

From Eqs. (3) and (4), the 8T design is proposed in figure2.The base circuit have three 2:1 MUX and one inverter. As shown in figure we get the sum output from MUX3 and we get the carry output from MUX2. We simulate this circuit at 32nm technology. The proposed technique and circuit is shown in figure2.

V. PROPOSED CIRCUIT

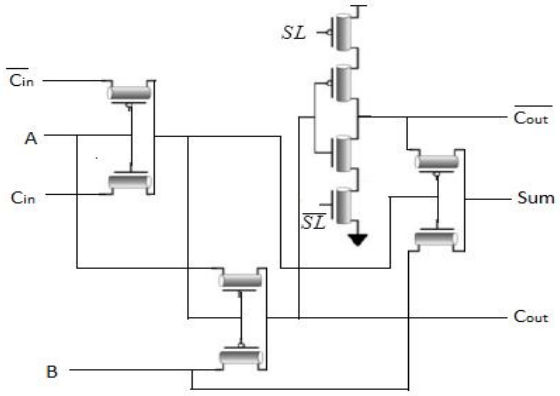

Figure 3. Proposed Circuit Using MTCMOS Technique

This circuit is used two extra transistor, when SL=1 the circuit goes in active mode and when SL=0, the circuit goes in sleep mode.

VI. RESULTS AND DISCUSSIONS

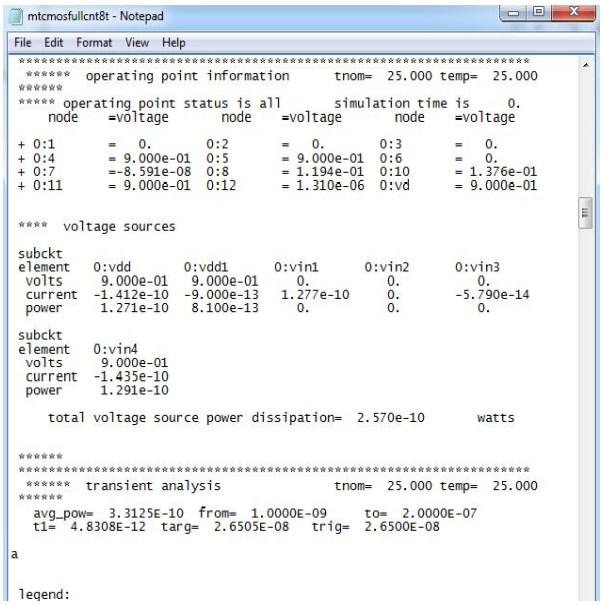

Figure 4. Simulated Results Window of 10T Full Adder Cell

VII. COMPARISON TABLE

Table 1. Comparison of results with previous work

Authors / Parameters	Yi WEI Journal of Zhejiang University 2011 [3]	Ali Ghorbani and GhazalehGhorbani 2014 [1]	FazelSharifi 2015[4]	**Proposed Work 1**	**Proposed Work 2**
Technology	180nm	32nm	32nm	**32nm**	**32nm**
Supply Voltage	1.8v	0.9v	0.9v	**0.9v**	**0.9v**
Leakage Current	-	-	-	**2.820E-10**	**1.412E-10**
Leakage Power	-	-	-	**2.538E-10**	**1.271E-10**
Propagation Delay	0.496 nW	1.1898E-10	112.76E-12	**4.6304E-12**	**4.8308E-12**
Average Power	36.47 µW	5.9341E-09	7.5347E-05	**4.4766E-08**	**3.3125E-10**
Power Delay Product	-	7.0604E-19	8.4959E-15	**20.729E-20**	**16.002E-22**

VIII. CONCLUSION& FUTURE WORKS

In this article a comparison between 8T MUX based full adder cell using CNT and proposed MTCMOS based full adder cell using CNT transistor is done. After comparison we found that CNT based circuit have a great advantage in terms of power consumption, propagation delay, leakage current and leakage power. During simulation it is founded that CNT based circuit have very good results in comparison to others. Here a comparison with previous published work is also done in table 1. Overall it can be says that CNT transistor can replace the CMOS transistor in future.

More power reduction techniques can be used to improve the results like SVL, AVL, LECTOR etc. Channel length can be reduced upto the 22nm, 12nm and so on for further improvements in results.

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