An Efficient Architecture of Carry Select Adder Using Brent Kung Adder

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Abstract- *In this paper, Carry Select Adder architecture is done using parallel prefix adders. Instead of using dual Ripple Carry Adders , parallel prefix adder i.e., Brent Kung adder is used to design Regular Linear CSA. Adders are the fundamental building blocks in digital integrated circuit oriented designs. Ripple Carry Adder gives the most compact design but takes high computation time. The time critical applications use Carry Look-ahead to obtain fast results but they results to increase in area. Carry Select Adder is a compromise between RCA and CLA in term of area and delay. Delay of RCA is high therefore we have replaced it with parallel prefix adder which gives quick results. We proposed structures of 16-Bit Regular Linear Brent Kung CSA and Modified SQRT BK CSA are designed. Power and delay of two adders' architectures are calculated at various input voltages. The results depict that Modified SQRT BK CSA is better than all the other adder architectures in terms of power but with little speed penalty. The designs have been done at 45nm technology using Tanner EDA tool.*

Keywords- Brent Kung Adder, Ripple carry adder, modified square root BK CSA, Binary to excess 1 converter, Multiplexer.

I. INTRODUCTION

An adder is a digital circuit that functions adding of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit, but also in some parts of the processor, where they are used to calculate addresses, table indices, and operations. Addition normally impacts widely the overall performance of digital system and an arithmetic function. Adders are used in multipliers, in DSP to perform various process like FFF, FIR and IIR . Millions of instructions per second are performed in microprocessors using adders. So, speed of operation is the most important parameter. Design are one of the most needed areas of research in VLSI. In CSA, all possible values of the input carry i.e. 0 and 1 are defined and the result is calculated in advance. Once the real value of the carry is known the result can be easily selected with the help of a multiplexer stage. Conventional Carry Select Adder is modified using dual Ripple Carry Adders (RCAs) and then there is a multiplexer stage. Here, one RCA is replaced by brent kung adder. As, RCA and Brent Kung adder.

II. BRENT-KUNGADDER

An optimal number of stages from input to outputs but with asymmetric loading on all intermediate changes is done by Brent-kung adder. It is one among the parallel prefix adders, which is based on the generate and propagate signals. In Brent-kung adders cost and complexity is less. But Brent-kung adder gate level depth is O(log2(n)), hence speed is lower. Fig.1 shows the block diagram of brent-kung adder.

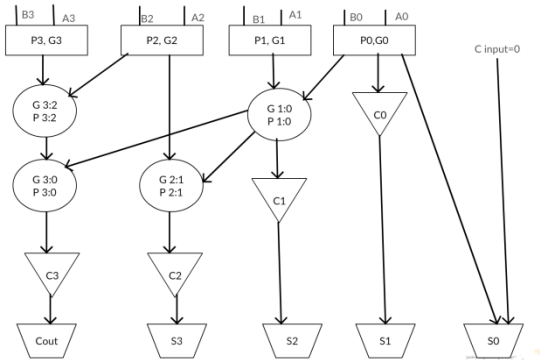

Figure 1. 4-Bit brent-kung adder

III. EXISTING SYSTEM

Conventional carry select adder made up of dual ripple carry adder and a multiplexer. Brent kung adder has minimum delay comparing with ripple carry adder. Regular linear BK CSA is designed using one brent kung adder of Cin=0 and a ripple carry adder for Cin=1. It has four blocks of same size. In order to increase the speed of arithmetic operation we are using a tree structure form. In a section of Regular linear BK CSA, one BK for Cin=0 and one RCA for Cin=1. Then the C3 tells whether the input carry is 0 or 1 and based on the value of output particular block is selected . Fig.2 represents the Regular linear Brent-kung Adder.

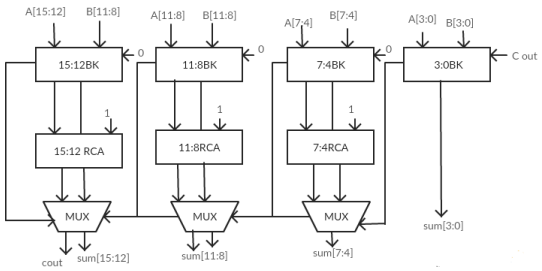

Figure 2. Regular linear BK CSA

IV. BINARY TO EXCESS-1 CONVERTER

Since, Ripple carry adder of Cin=0 and brent-kung adder of Cin=1 is more of area consuming in Regular linear brent-kung carry select adder. Hence, a different scheme called Binary to excess-1 convertor is used to decrease the area and power consumption. BEC is used to add 1 to input numbers. In order to minimize the area instead of Brent-kung adder of Cin=1, the BEC is used. Fig. 3 denotes the 4-bit BEC

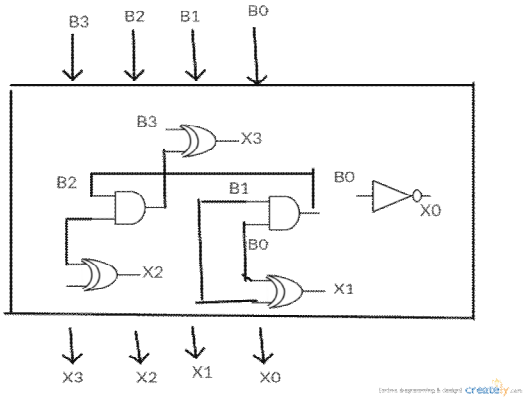

Figure 3. Binary to excess -1 convertor

The Boolean Expressions for the above BEC :
X0=~B0
X1=~B0(1)
X2=B2*(B0 &B1)
X3=B3*(B0 &B1 & B2)

Table 1. Power comparison in CSA

TECHNIQUE	POWER CONSUMPTION
CSA using RCA	326 W
CSA using BEC	302 W

V. PROPOSED SYSTEM

The proposed system is designed using a brent-kung adder of Cin=0, a BEC of Cin=1 and a multiplexer block. It has 5 blocks of various size using Brent-kung adder and BEC. Area consumption is less by designing with minimum number of logic gates as BEC and RCA. Each section has one BK , one BEC and MUX. In N bit bent kung adder, N+1 bit BEC is used. Only for 16 bit word size power and area consumption is calculated. Fig.4 shows the 16-bit modified square root BK CSA.

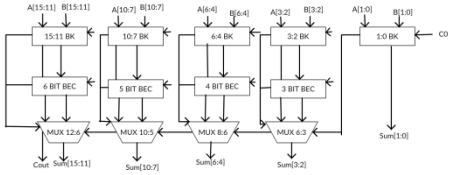

Figure 4. Modified Square root BK CSA

VI. SIMULATION RESULTS

Power consumption and area consumption of regular linear BK CSA and Modified square root BK CSA has been designed using 16-bit word size. Comparison of these two adders on basis of area and power is given in the Table. 2. The result shows that modified square root BK CSA has better outcome in power consumption and area consumption at various input voltages. Fig.4 shows the graphical representation of comparison two adders at different input voltages.

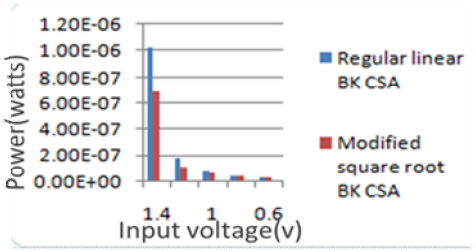

Figure 5. Comparison of power at various input voltages

VII. FUTURE WORK

The proposed work can be extended with high number of bit size like 32 bit, 64 bit and further applied in larger applications and field. In this proposed work there is drawback in speed i.e the delay of the architecture is quiet large, hence in future work can be handled to largely reducing the delay of the Carry select adders. Parallel prefix adders are again can be used in different technique in minimizing the delay in the proposed system.

VIII. CONCLUSION

In order to reduce the area and power consumption of carry select adder. The brent-kung adder for Cin=0 and binary to excess-1 convertor of Cin=1 is used in replacing the ripple carry adder of Cin=1 and brent kung adder Cin=0. Therefore, the architectures of Regular linear Brent-kung adder and

Modified Square root Brent-kung Adder is designed in 16-bit word size. Here, we used brent-kung adder from parallel prefix adder because it derive fast results. With small speed penalty the modified square root BK CSA has reduced power and area consumption comparing with the regular linear BK CSA, So, it can be applied in multipliers, adder circuits, DSP processors such as Finite impulse response.

Table 2. Comparison of existing and proposed system

DESIGN	NO.OF TRANSISTOR	AVERAGE POWER
REGULAR LINEAR BK CSA	192	0.020421mw
MODIFIED SQUARE ROOT BK CSA	174	0.0021791mw

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