A Superregenerative QPSK Receiver

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Abstract-*In this paper we present a description and experimental verification of a superregenerative receiver (SR) for QPSK signals. Exploiting the fact that a conventional SR generates pulses which preserve the input phase information, we take 1-bit samples of each generated pulse. A suitable choice of the sampling frequency gives as a result a bit vector containing a sub-sampled version of each PSK pulse. Extremely simple digital processing of the vectors from two consecutive pulses allows symbol decision, together with information on signal quality and frequency displacements. Although presented for the QPSK case, the principle may be applied to the M - PSK case with obvious changes. Experimental results on a 20 kbit/s proof-of concept receiver in the 27 MHz band, achieving a sensitivity of 103 dBm, with an FPGA-based implementation of the digital part, validate the proposed approach.*

Keywords-Low-power communication receivers, QPSK demodulation, RF receivers, superregenerative receiver.

I. INTRODUCTION

In the last years, superregenerative receivers are getting in-creased attention because they are an attractive alternative for low-power wireless data links. The main reason for this is their reduced complexity, which is easily translated into low cost and low power consumption. Since its introduction in 1922 [1], this receiver has been successively refined with bit - synchronous designs [2], [3], applications to direct-sequence spread-spectrum [4], and several integrated implementations, such as [3], [5]–[9], have been recently reported. Expressed in perhaps the most general terms, receiver operation relies on a superregenerative oscillator (SRO), a feedback system with a second-order bandpass filter where a pulsed, externally injected signal—the so-called quench signal—is able to control the feedback gain and, hence, the stability or instability periods of the whole system. So, in response to the quench pulses, the SRO is able to generate RF pulses. Several parameters of these RF pulses are dependent on the value of certain parameters (amplitude, phase, frequency) of the external RF input signal in a sensitivity window centered around the instants where the system changes from stable to unstable [10], [11].

Traditional receiver operation aimed at detecting amplitude-modulations or, in the digital case, OOK (on-off keying) modulations, makes use of a quench signal of considerably higher frequency than the actual information bandwidth. In this approach, the dependence of the SRO envelope on the input amplitude is used to effectively oversample the envelope of the incoming RF signal. A final low-pass filter is then able to reconstruct the trans-mitted signal. In this approach, the equivalent bandwidth of the receiver turns out to be much larger than the bandwidth of the transmitted signal, which translates into a low performance in terms of the required signal-to-noise ratio (SNR) for proper operation.

This drawback may be overcome making use of a bit-synchronous quench signal, allowing to generate a single RF pulse for each received bit [2], [3]. In this approach, the envelope of the generated RF pulse is also dependent on the amplitude of the incoming RF signal. In this approach, the sensitivity window of the receiver may operate as a matched filter [2], optimizing the noise performance of the receiver. Operation in this mode re-quires paying attention to the synchronization problem between bit and quench phase and frequency Building on the same basic idea, the receiver has also been used to detect direct -sequence spread-spectrum signals, where the quench signal is synchronous to the chip rate [4].

While it is known [10] that the signal generated in the SRO preserves input phase information, only two implementations of SR receivers being able to detect binary phase-modulated (BPSK) signals have been reported. In [12], the SRO was built around a transmission line oscillator where the transmission line supports two modes of oscillation depending on a control signal. In the first mode of oscillation, the generated signal has no dc component and is an exponentially growing oscillation whose phase is coherent with the phase of the received signal. At a given instant, the circuit topology is switched to generate the second oscillation mode which is characterized by producing a waveform consisting in the sum of a) a similar waveform whose frequency is twice the frequency of the first mode and b) an exponentially growing low frequency component whose amplitude is proportional to the cosine of the generated signal phase in the first topology at the moment of switching. Low-pass filtering the generated signals allows retrieving a dc component whose sign is used to decide the received bit in a BPSK modulation. While the operation principle was

demonstrated experimentally, no performance figures of a receiver in actual operation were reported. In contrast, the technique in [13] makes use of a conventional SRO followed by a one-bit sampler acting when the SRO pulses have achieved sufficient amplitude. A conventional flip-flop is used to sample and store the decided bit, which is even less complex than analog envelope detection and ulterior sampling. A receiver prototype demonstrated satisfactory operation.

Experimental multi-level PSK detection has still not been reported, to the authors' knowledge. However [14] reports the design and simulation of an approach for SR QPSK detection: The SRO is used as a simple front-end amplifying and filtering the input signal while preserving phase information. The scheme suggested in [14] includes a conventional IQ demodulation chain. Besides no experimental verification, this approach has two significant drawbacks which cannot be overlooked. First, in a real implementation, the comparatively high-level local oscillator required for conventional IQ demodulation, operating at the frequency of the channel to be received, would completely mask the signal to be received. Second, this approach entails a significant complexity and associated power consumption, spoiling the main point of using the SR principle.

In this paper we present the first description and experimental verification of an SR QPSK receiver. Based on a bit-synchronous receiver, we build on the results in [13] but taking 1-bit samples of each SRO pulse. A suitable choice of the sampling frequency gives as a result a bit vector containing a sub-sampled version of each PSK pulse. By comparing the current vector to the previous one the symbol decision is straightforward. Although presented for the QPSK case, the principle may be applied to the M- PSK case with obvious extensions. This approach is done in the digital domain with minimum complexity. As a by-product, information on re-ceived signal quality and frequency displacement is obtained, allowing for easy synchronization. Experimental results are provided to validate the proposed approach [15].

II. A LOW-COMPLEXITY PSK SUPERREGENERATIVE RECEPTION PRINCIPLE

The ideas to be explained next may be applied to any -array PSK modulation. However, we will use the QPSK case for most explanations. This is done in part because of the inherent interest of the QPSK case and in part to simplify the explanation. The extension to other cases should be straight forward. A basic QPSK modulated signal with a symbol rate around a carrier may be written as

$$x(t) = \sum_{n=-\infty}^{\infty} p_c(t - nT_s)\cos(\omega_c t + \phi_n) \quad (1)$$

with the phase corresponding to the n-th symbol given by $\phi_n = \{0, \pi/2, \pi, 3\pi/2\}$ and $p_c(t) = \Pi(t)$ i.e. a unit pulse. In a SRO operating in the linear mode, the response to an input signal given by (1) may be written as [10]

$$s(t) = K\,|H(\omega_c)| \sum_{n=-\infty}^{\infty} p(t - nT_q) \times \cos\left(\omega_0 t + n(\omega_c - \omega_0)T_q + \phi_n + \angle H(\omega_c)\right) \quad (2)$$

assuming that the changes from stability to instability happen at $t = nT_q$ and that $T_q = T_s$, as we are taking one quench cycle per symbol.

A detailed discussion of the parameters in (2) is available in [10]. Here, we will point out that T_q is the receiver quench pe-riod, ω_0 is the SRO oscillation frequency, $H(\omega_c)$ is a frequency response term, depending on the carrier frequency, and $p(t)$ is a normalized pulse, with $\max(p(t)) = 1$. Upon inspection, we may conclude that the response (2) is a train of RF pulses where the phase information contained in the input signal is preserved [13], [16]. If we consider the phase term of the n-th pulse

$$\varphi_n(t) = \omega_0 t + n(\omega_c - \omega_0)T_q + \phi_n + \angle H(\omega_c) \quad (3)$$

the phase difference between the consecutive n-th and $(n-1)$ -th pulses becomes

$$\Delta\varphi = \varphi_n(t) - \varphi_{n-1}(t - T_q) = \phi_n - \phi_{n-1} + \omega_c T_q. \quad (4)$$

It is usual to choose the symbol duration T_s to be a multiple of $T_c = 1/f_c = 2\pi/\omega_c$, ensuring that a CW signal is generated if a symbol is repeated indefinitely. From this, it follows that $\omega_c T_q$ is a multiple of 2π and the phase difference in (4) becomes

$$\Delta\varphi = \phi_n - \phi_{n-1} \quad (5)$$

meaning that phase changes in the input signal directly translate into phase changes in $s(t)$. Note also that, if T_s is not a multiple of T_c, there would be a fixed phase term in (4) that could be compensated for during symbol decision. For simplicity, in the following, we will assume that (5) holds. On the other hand, we shall mention that having to work with phase differences is no significant drawback, as many PSK systems rely on differential signaling schemes.

At this point it should be noted that the result from (2) is obtained for an SRO operating in the linear mode and making some reasonable assumptions and simplifications. A more de-tailed analysis is given in [16], without underlying assumptions and covering also the SRO in the logarithmic mode of operation, and showing that the main conclusion of (5) is still valid.

Now, from a pure signal processing point of view, the SRO signal $s(t)$ could be demodulated by a conventional PSK detector, using IQ down conversion as suggested in [14]. However, in a practical implementation, the radiation from the oscillator required for down conversion would mask the input signal. On the other hand, this approach requires a significant complexity and power consumption in the conventional signal processing part, spoiling the main advantage of SR detection.

Alternatively, at a fixed time offset T_1 with respect to $t=nT$, (when the SR changes from stable to unstable) the SRO signal $s(t)$ has achieved sufficient amplitude and may be sampled and discretized with two levels with a simple D flip -flop, as in [13]. Now, if the detected bit is fed into a shift register clocked by N pulses of suitable frequency f_{CLK}, for each RF pulse we may obtain digital patterns such as those depicted in Fig. 1. The idealized waveforms in Fig. 1 show the RF signal subsampled and quantized to obtain 20 1-bit samples from 21 RF cycles.

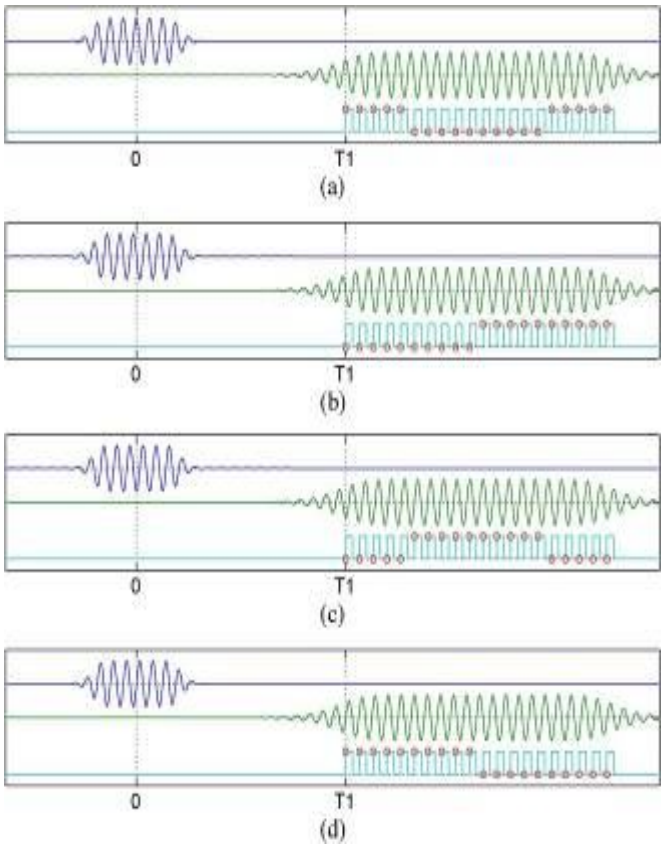


Fig. 1. Idealized representation of the QPSK detection scheme (see text). Fig. 1(a) depicts the qualitative behavior for an RF pulse with relative phase 0. Fig. 1(b) corresponds to an RF pulse with relative phase $\pi/4$ and Figs. 1(c) and 1(d) correspond to phases $2\pi/4$ and $3\pi/4$ respectively.

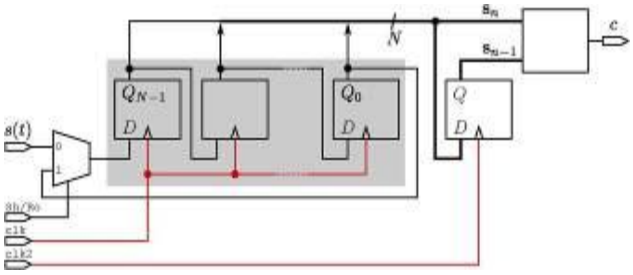


Fig. 2. A schematic representation of the sampling and correlation process.

In practice, there are many more RF cycles than depicted, so that the choice of is not critical. In each of the subfigures the traces qualitatively depict respectively, from top to bottom, the modulated input signal , the SRO output signal and the sampling clock signal, with the obtained samples denoted the response is the same as if the input signal fi lls up the whole symbol period. This might be used to further decrease power consumption in the transmitter side (with lower power spectral density, although with increased bandwidth).

On the other hand, this property is also advantageous if the transmitter phase is not kept constant during the whole symbol, as happens with many PSK -based standards, where the base-band pulses are pre-filtered to reduce the occupied bandwidth while avoiding inter-symbol interference: as long as the instantaneous phase achieves the required value during the sensitive period, the signal $s(t)$ and the corresponding vector $\mathbf{s}$ are the same as those obtained keeping the phase constant during the whole symbol.

III. IMPLEMENTATION DETAILS

The process of subsampling $s(t)$ generates a lower frequency signal which is sampled in a whole period using N samples. This may be achieved with a sampling frequency satisfying

$$f_{CLK} = \frac{N}{kN+1} f_0 \tag{6}$$

with any integer k. The case $k=0$ means taking N samples in one single period of $s(t)$, which results in a frequency that is too high for most purposes. Taking $k=1$ means obtaining N samples in $N+1$ periods of $s(t)$. In this case, for high values of N, and depending on the selectivity of the SRO, this might

translate into a frequency f_{CLK} that is too close to f_c, which could mask the signal to be received. In general we may be interested in low clock frequencies, and there are no restrictions to taking $k \geq 2$ which means sampling during $kN+1$ periods. In this way, the sampling frequency may be set sufficiently far away from the SRO bandwidth so that it does not interfere with the operation of the SRO. Negative values of k are also feasible, but will introduce a sign change in (5).Considering also the results in [16], it follows that the instantaneous frequency of the SRO is sufficiently constant during the interval where the SRO has sufficient amplitude. As a con-sequence, there will be no significant warping in the obtained samples.

Once the vector of current samples s_n is stored, it is compared to the vector of the previous samples s_{n-1} , and the displacement that provides highest correlation is found. This is achieved by circularly rotating s_n by k positions (notated $\mathrm{rot}^k(s_n)$) and counting the number of 1 in the comparison (logical xnor) with the previous vector s_{n-1} . In compact form, this may be written as

$$c(k) = \mathrm{sum}\left(\mathrm{rot}^k(s_n) \,\mathrm{xnor}\, s_{n-1}\right). \tag{7}$$

In practice this computation is carried out very efficiently storing the received samples in a shift register. Then, when all positions are filled, the shift register is successively rotated and the comparison with the previous register is carried out.

Fig. 2 and the associated timing diagram in Fig. 3 depict this schematic data flow in a simplified view. The signal Sh/Ro controls whether the shift register is shifted in or rotated, and a combinational block computes the similarity between vectors $c(k)$as in (7). Note that, in the real implementation, the system is fully synchronous with suitable enable signals at each flip-flop.

The sum of ones in (7) has been done in a combinational process in our proof -of-concept implementation. However, as there are many clock cycles available $(T \gg T_{CLK})$, this could be done in a sequential process where one bit is compared at a time, which could lead to even lower resource usage.The information that may be extracted from this procedure

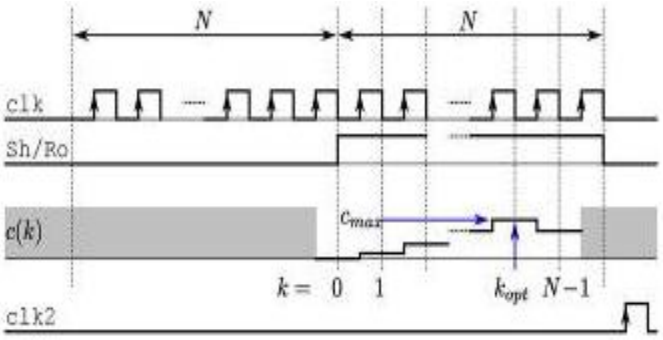


Fig 3: Timing Diagram

The displacement k_{opt} that gives maximum correlation. From this information, the phase difference is directly obretical lower bound, but it is often desirable to have more information available to perform better symbol decisions, reducing the error probability, and to extract information on the quality of the decisions. In general, N should be an odd multiple of 4 to have a symmetric constellation plane. For instance, $N=20$ would give 20 different values for the phase difference between successive pulses (Fig. 4) to choose from. In the ideal case, we would observe only 0, $\pi/4$, $2\pi/4$ and $3\pi/4$ phase differences.

But in the presence of noise and minor errors of frequency for The displacement from the most probable transmitted current symbol was decided with an offset of

$$\left[\frac{N-4}{8}, \cdots, \frac{N-4}{8}\right]\frac{2\pi}{N} \tag{8}$$

following the procedure outlined in Table I. The average of d provides a significant insight into receiver operation, as will be explained in the next sections. Our prototype even uses 5 LEDs driven by to give a visual indication of receiver operation.

IV. EXPERIMENTAL RESULTS

We have built an experimental receiver prototype to validate the proposed approach. The structure of the whole receiver is depicted in Fig. 5.

The digital part has been implemented on a DE0-Nano low-end prototyping board [17]. For convenience, we have chosen a straightforward clock frequency of $f_{CLK}=25$MHz and the SR

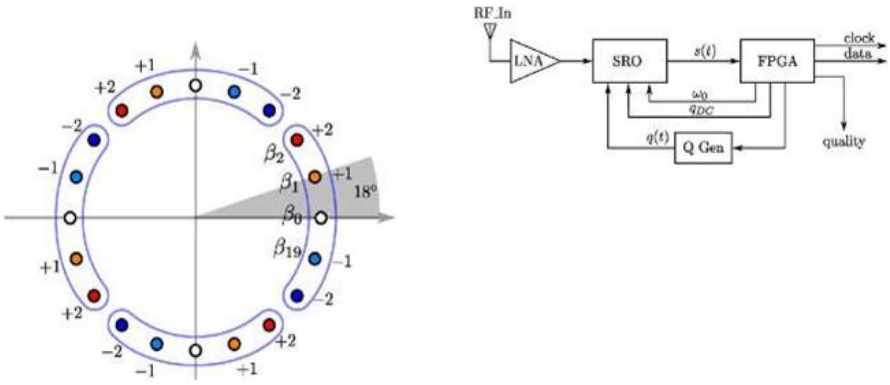
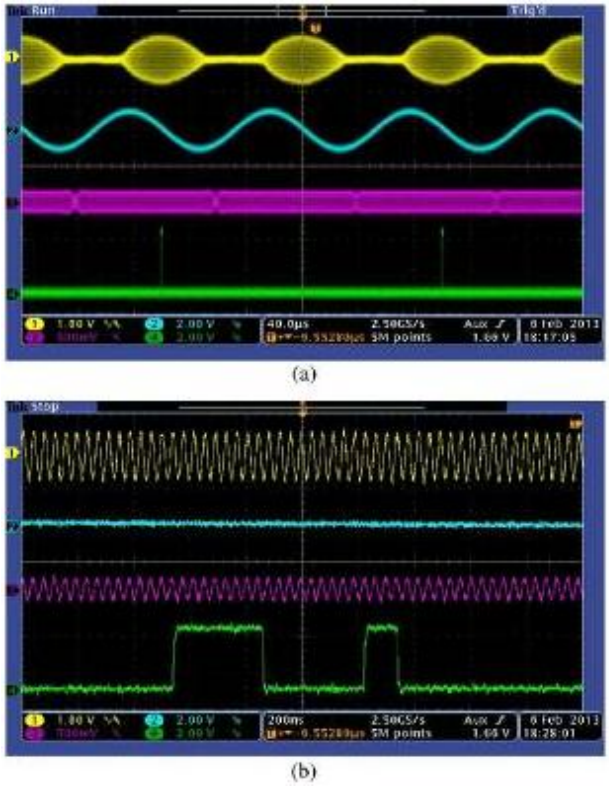


Fig. 4. The set of possibly detected phase differences for N=20 and their corresponding decision regions

core was tuned to $f_c = 25 \times 21/20 = 26.25$ MHz Symbol rate is 10 ks/s corresponding to a bit rate of 20 kbit/s The schematic of the LNA and the SRO core is essentially the same as in [13], with minor enhancements.

The FPGA provides two pulse- width modulated (PWM) sig-nals to the SRO core: The signal labeled ω_0 allows tuning the center frequency of the receiver by means of a varicap diode. The signal q_{DC} is a DC quench component that is added to the ac part of the quench signal $q(t)$. For the sake of flexibility while experimenting different waveforms, $q(t)$ is currently gen-erated by an external generator, triggered



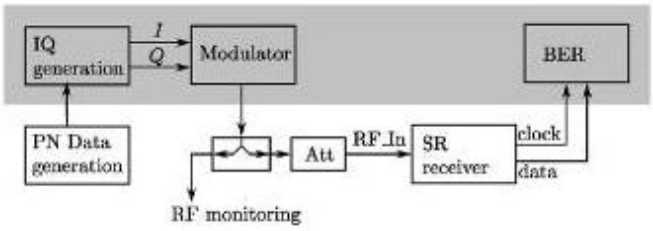


Fig. 6. Fig. 6(a): QPSK SR receiver in operation

by a signal from the FPGA—although in the following it has been kept generating a 2 Vpp sinusoidal signal. In a practical implementation, an analog or FPGA-based approach would be straightforward to implement.

Fig. 6 shows the main receiver signals while in operation. It may be seen from Fig. 6(a) that the receiver is operating in the logarithmic mode, where input phase information is also pre-served [13], [16]. It should be pointed out that operation in the linear mode or in the transition from linear to logarithmic mode, which is often the choice for traditional ASK modulations, re-quires a fine control on the quench amplitude which has to be readjusted for different input signal levels. In the logarithmic mode of operation such a control is not

necessary: the circuit may be adjusted, for instance through V_D $C_{(f)}$, to ensure saturation when no RF input signal is present and no further adjustment is

The top trace (#1) depicts v_o, showing operation in the logarithmic mode. Trace #2 is the ac part of the quench signal, v_q. Trace #3 is a replica of the transmitted signal (QPSK modulated) while the bottom trace (#4) depicts the N samples obtained in each quench period. Fig. 6(b): A zoomed-in single shot depicting the samples obtained for a single pulse For instance, in our prototype we have measured a dynamic range greater than 83 dB without any adjustment.

To test the performance of the whole receiver in operation we have used the test setup depicted in Fig. 7. A PN9 sequence turn, the generator internally constructs the baseband IQ signals according to the desired shape and modulates them onto a carrier. The RF output signal is split in two paths with a power divider: the first path is used for signal monitoring and the second one reaches the SR receiver after a fixed 60 dB at-tenuator. Among other signals, the SR receiver outputs ber_clk and a ber_data signals that are fed to a Bit Error Rate (BER)analyzer, properly adjusted for the PN9 sequence used in this test. Fig. 8 depicts the measured BER vs. RF_In peak input power level in dBm. It follows that the receiver has a sensi-tivity of approximately 103 dBm for the usual specification of $BER = 1 \times 10^{-3}$. The 3 dB bandwidth of the receiver is97 kHz, which is reasonable given the high gain associated with the logarithmic operation mode. The re-radiated power through the antenna connector is less than 95 dBm. This relatively low level is due to the high reverse isolation of the cascode structure of the LNA [13].

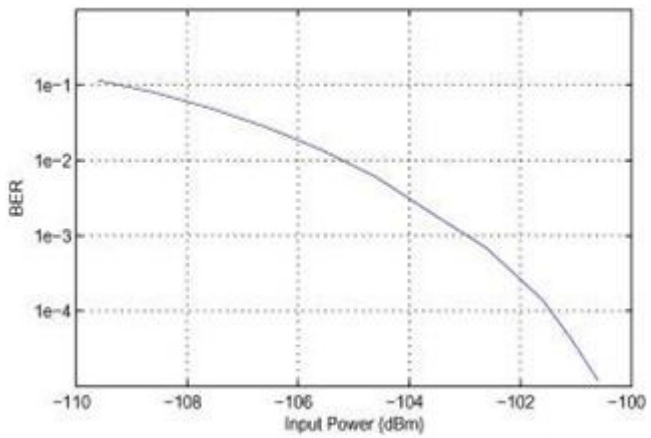


Fig. 7. Experimental Bit Error Rate vs. RF_In peak input power.

V. DISCUSSION

A. Performance With Pulse Shapers and Pulse Modulation

The performance of the receiver has also been tested using a Nyquist pulse filter with $\alpha = 0.35$ at the transmitter side. This means that the phase keeps changing more or less smoothly between symbols and that the exact phases of multiples of $\pi/2$ are only observed at the center of the symbol period (Fig. 9(a)).

As expected, there are no differences in performance when the sensitivity window of the SRO happens at the appropriate time points where the transmitted phase has to be observed.

When this is not the case, i.e. when there is a phase error between the transmitter symbol clock and the receiver quench, we will observe phase transitions between symbols which are not multiples of $\pi/2$. This is easily monitored by the average of vector $\mathbf{d}$.On the other hand, as the transmitted power outside the sen-sitivity window is lost, the same performance may be achieved by pulse-modulating the phase -modulated signal. For instance, in Fig. 9(b), the same BER is achieved with 10 dB less trans-mitted power (pulse duty cycle is 10%), although with higher bandwidth.

B. Effects of Frequency Displacement

The relative displacement of the transmitter carrier frequency f with respect to the transmitted symbol clock frequency may be avoided deriving both signals from the same reference, as is usual in modern transceivers. On the other hand, in many standards relying on packet transmission, the receiver clock reference is often specified tight enough (for instance, ± 40 ppm [18])

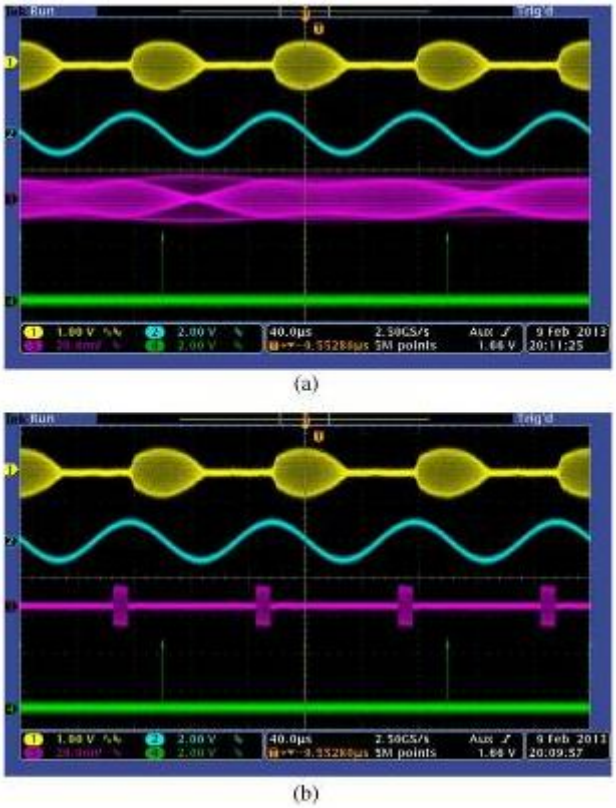


Fig. . Receiver operation is unaffected when transmitter uses Nyquist pulse shaping with $n=0$ (9a) or when the signal is pulse-modulated (9b), as the instantaneous phase at the sensitivity window is the same. The traces are the same as in Fig. 6.

so as to ensure negligible drift over a whole packet after align-ment has been achieved in the preamble, making continuous fre-quency correction unnecessary.

For testing purposes, we have made changes to the input car-rierfrequency f_c, as this is equivalent to changes in the receiver clocks. As expected, changes in f in steps of $\pm f/N$ translate into a shift of ± 1 positions in the vector of averaged displace-ments, as may be obtained from (4).

So, the average of $\mathbf{d}$ provides an indication of the magni-tude and the sign of the frequency displacement. Hence, a very simple control loop allows staying properly tuned. The aver-aging and control signal generation may be easily implemented in an analog way with appropriate weighting resistors, following the scheme outlined in Fig. 10. This figure depicts the case for $N=20$, with the bits of $\mathbf{d}$ signaling ± 2 and ± 1 shifts driving the R and the $2R$ resistors, respectively. Signals c_+ and c_- are directly usable for frequency correction.

C. Noise Performance

The exact analysis of the effects of input noise and SR oscil-lator jitter on the samples s and on the subsequent decisions is

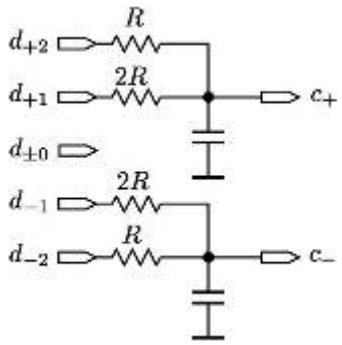


Fig. 9.Analog generation of frequency indication/correction signals for the $N=20$ case.

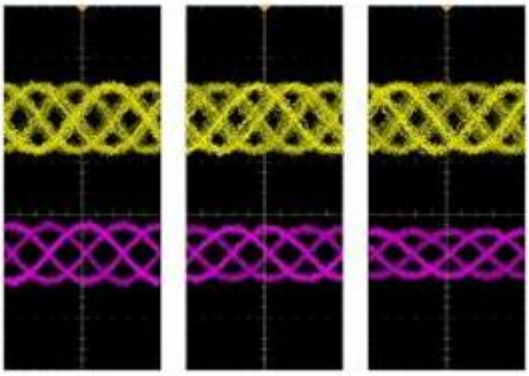


Fig. 10. SRO (top) and transmitted (bottom) signals taken with 10 s screen persistence. The receiver is operating at a BER of 5×10^{-2} (left), 5×10^{-1} (center) and 5×10^{-3}(right).

subject of current work and out of the scope of this paper, de-voted to presenting the core idea. However, some observations and considerations may be done.

First, it should be remarked that the whole SR behavior is determined by the input signal and noise during the sensitivity window. As a consequence any meaningful measure of the signal to noise ratio depends on the filtering performed by the inherent SR operation of the classical receiver, thus being independent of the detection scheme.

On the other hand, some preliminary Matlab simulations show that, in order for the SRO jitter to contribute significantly to the overall error probability, the magnitude of the jitter would have to be significantly higher than what is routinely achievable from conventional designs, unless operating at an extremely good SNR.

To illustrate typical receiver operation for different input signal levels, Fig. 11 depicts the SRO signal (top traces) together with the transmitted signal (bottom traces) all taken with a trace persistence of 10 s.

A measure of the quality of the decisions, directly related to input signal quality and to the resulting BER, is obtained by the information that is qualitatively equivalent to the BER.

D. Frequency Scaling

Several kinds of SR receivers have been demonstrated at fre-quencies exceeding 20 GHz, e.g. [19] and references therein. The scheme suggested herein only relies on the ability of the first flip-flop of the shift-register of being able to sample the SRO signal. The subsequent stages may easily work at a clock frequency down to several orders of magnitude lower. With the current state of the art of CMOS technologies, the design of the first flip-flop is by no means a fundamental challenge. This,combined with FPGAs able to cope with multi-Gigabit serial in-terfaces and the availability of even discrete flip- flops operating at frequencies over 20 GHz make the approach directly exten-sible to higher frequencies, both in CMOS and discrete-compo-nents versions.

E. Complexity and Power Consumption

The SR front-end is a conventional design, with a power con-sumption in the sub -1 mW region, without any particular effort done in optimizing this figure. As the digital part was imple-mented on a Terasic DE0-Nano development board, it is not easy to give figures on power consumption due to the overhead of other elements on the board. On the other hand, these figures could change drastically implemented on other devices aimed specifically at lower power consumption or when integrating the full design in a custom chip.

The whole receiver takes up very few resources, as is easily deduced from its structure. Excluding debugging and monitoring elements, and without any optimization effort the fitter (Altera Quartus II) reports an usage of around 160 logic elements so that it could even fit on one of the smaller CPLDs currently available. Also, the design requires only clock cycles per symbol. In our prototype, this means that the 25 MHz clock is active only 1.6% of the time. Hence, we may conclude that the detection circuitry adds little complexity and very limited power consumption to a naked SRO core, independently of the technology used (discrete or integrated).

From the power consumption point of view, significant saving can be accomplished by choosing the sampling start time T_1 as soon as the amplitude is sufficient for the first flip-flop and quickly extinguishing the oscillator once the samples have been obtained, as in [5]. This would be achieved by a suitable quench waveform. In our experiments, we have used a plain sinusoidal signal to allow focusing on the core of this paper.

VI. CONCLUSION

In this paper we have presented what, to the best of our knowl-edge, is the first experimental verification of an SR receiver able to efficiently demodulate QPSK signals. Based on the well-known but usually unexploited fact that the information con-tained in the RF signal phase is preserved by an SR oscillator, we have proposed a simple post-processing scheme that allows signal demodulation. The post-processing scheme consists in subsampling the RF pulses generated in the SR oscillator. The vector of the 1-bit quantized samples corresponding to the cur-rent symbol is correlated to the vector corresponding to the past symbol. From this information the phase change and, hence, the transmitted data is inferred.

The complexity of the all-digital demodulation scheme is ex-tremely low, taking up very few resources on the low-end FPGA prototyping board used.

With a suitable number of samples for each symbol, the pro-posed approach is also able to provide: *a)* a measure of the re-ceived signal quality in terms of bit error probability and *b)* an indication of sign and magnitude of possible frequency drifts. These features are not directly available in conventional SR re-ceivers intended for ASK-modulated signals.

Operating with a constant amplitude QPSK-modulated signal a 20 kbit/s receiver prototype achieves a sensitivity of 103 dBm for a bit-error-rate of 1×10^{-3}. However, as the SR re-ceiver exhibits a time sensitivity window which is a fraction of the symbol period, it is possible to achieve the same perfor-mance shaping the transmitted signal in pulses better matched to the SR sensitivity window. In this way, the sensitivity may be enhanced by about 10 dB.

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