A 30 Ghz Low Power,Low Phase Noise Mosfet Vco Using 65 Nm Technology

Monika Gupta[1], Vinod Sonkar[2], Deepak Sharma[3]
[1, 2, 3] SDBCT,Indore

Abstract-*A VCO is one of the key building blocks of RF wireless communication because its phase noise performance will make an impact on the sen-sitivity level and blocker characteristic of a receiver. A Voltage Controlled Oscillator (VCO) is used for implementing a frequency synthesizer to provide the Local Oscillator (LO) signal for an up/down converter in a RF transceiver or a data and clock recovery in a high speed data links with a Phase-Locked Loop (PLL). Parameter which are important in context of designing LC VCO are phase noise,tuning range,FOM,supply voltage.*

One of the parameter which is very important to be focused on is phase noise. The inductor and capacitor is connected in parallel at the drain of NMOS transistor to reduce the phase noise as well as to improve the figure of merit which indicate the performance of LCVCO is implemented in this thesis. In this thesis, 30 GHz LC VCO is shown with the help of which better phase noise and FOM is obtained. Whole circuit is implemented on 65nm technology. A 8.4 GHz tuning range is obtained with tuning voltage of 0-1V. The power consume by the whole circuit is 1mW which is better than the other listed papers shown in the references. The supply voltage is 1V.

I. INTRODUCTION

Voltage Controlled Oscillator is tunable oscillator whose output frequency is linear function of control voltage. The relation between output frequency (f0) and control voltage Vcon is given below

$fout = f0 + K \,.\, Vcon$

Where, *f*0 is the oscillation frequency at $Vcon$ = 0 and $KVCO$ represent the gain or sensitivity of the circuit . The achievable range, *f2 – f1,* is called the frequency tuning range.

1.1 Characteristics of VCO

a) Phase Noise: Noise in phase is referred as phase noise which is basically a random deviation in frequency or random variation in zero crossing point of time dependent oscillator waveform.

David B. Lesson in 1966 given a phase noise model commonly known Lesson's model for oscillator the phase noise predicated by this model is can be expressed as

$$L(\Delta\omega) = 10\log\left[\frac{2FK_T}{P_s}\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\left(1+\frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right]$$

By choosing carefully power supplies, power supply noise and tuning voltage supply noise can be minimized. Due to this reason phase noise of the VCO is mainly determined by the overall quality factor Q of the circuit.

b) Tuning Range: Frequency of oscillation for LC tank is given below by manipulating equation

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Tuning of capacitor is achieved by use of voltage dependent capacitor which is varactor. By varying the voltage of these varactor maximum and minimum capacitance can be obtained which help to calculate minimum and maximum oscillation frequency which is given by below equations

$$f_{max} \approx \frac{1}{2\pi\sqrt{LC_{min}}}$$

$$f_{min} \approx \frac{1}{2\pi\sqrt{LC_{max}}}$$

The C_{max}/C_{min} is necessary for designing LC VCO which is given by below equation

$$\frac{C_{max}}{C_{min}} = \frac{f^2{}_{max}}{f^2{}_{min}}$$

Where centre frequency of oscillation f_0 is given by below equation

$$f_0 = \frac{f_{max} + f_{min}}{2}$$

Finally fraction tuning range is given by

$$Fractional\,Tuning\,Range = \frac{f_{max} - f_{min}}{f_0}$$

c) Power Dissipation: Today many wireless devices are required long life of battery which means that have low power consumption. But for VCO designer it's difficult to obtain low power consumption and low phase noise simultaneously. This because of tank voltage amplitude is proportional to current

flowing. It means that there is trade-off exist between phase noise and power consumption.

$$V_{tank} \approx I_{total} \cdot R_{eq}$$

II. LITERATURE SURVEY

Zhou Mingzhu, [3] has proposed a low phase noise wideband LC VCO is realized in the SMIC 65 nm CMOS technology for low power applications. In this paper they used conventional CMOS cross coupled differential topology with a switched capacitor array, two power supply and substrate noise filters. In the proposed VCO they are adopted switched capacitor array to realize the wideband function. They obtain performance indices such phase noise and power consumption are measured to be-125.8 dBc/Hz at 1 MHz offset and 3.4mW respectively. They observed tuning range of 0.75GHz-1.5GHz for frequency .The FOM is found to be -180 dBc/Hz at a offset frequency of 1 MHz.

IjiAyobami B et.al [4] proposed low power, wide tuning range CMOS LC VCO for ultra wide band application in 0.25um CMOS process. They implemented cross coupled differential topology with double switch. They implement this topology using diode varactor and MOS varactor and compared. By this comparison they conclude that MOS varactor VCO has wider tuning range compared to diode varactor VCO. in their design they obtain 3.5GHz frequency of oscillation, power consumption of 2.26mW and phase noise of -108.8 dBc/Hz phase noise at 1 MHz offset frequency.

Mahmoud Moghavvemi and AliyarAttaran[6] demonstrated comparative study of various cross coupled topologies with different configuration for different CMOS processes. In their note they give detail discussion on phase noise reduction for CMOS LC VCO and effect of tail current source on resonator performance. In last they analyze on 1/f flicker noise contributed by active devices.

Albert Jerng, and Charles G. Sodini [11] present a impact of device type and sizing on phase noise mechanism for cross coupled differential topology. In their paper they show conversion of bias noise into phase noise through MOS switching transistor. They show minimization this phase noise through MOS device sizing rather than through filtering. In their paper they compare implementation of two cross coupled differential topology using NMOS and PMOS.

They finally concluded that PMOS based cross coupled differential topology has better phase noise performance in 1/f2 region and by reducing size of MOS switching transistor phase noise can be improve in 1/f3 region.

Lin Jia, et.al [14] presented a novel methodology for reducing phase noise in cross coupled LC tank VCO. In their paper they derive fundamental relation between phase noise and channel length of cross coupled MOS transistors is derived. Using this methodology they design 2GHz LC tank VCO by 0.18um CMOS technology. They obtain phase noise is -103.3 dBc/Hz at 100 kHz offset frequency and -118.9 dBc/Hz at 600 kHz offset with low-power consumption around 3.15 mW.

R. Saeidi, et.al [15] presented an analysis of phase noise differential cross coupled LC oscillator and a single-ended Colpitts oscillator were presented. In their paper they concluded that a single-ended Colpitts oscillator has better phase noise performance but consume more power compare to differential cross coupled LC oscillator.

Ali Fad et.al [17] demonstrated a comparative study of CMOS LC VCO Topologies in standard 0.35um CMOS technology for Wide-Band Multi-Standard Transceivers. In their study, they simulate both cross coupled differential and CMOS cross coupled differential topology and obtain result.The comparison shows that both circuits are applicable for multistandard transceivers. The complementary VCO shows 50% lower power dissipation with lower phase noise levels. Asa disadvantage, the circuit is suffering from larger parasitics and shows 500 MHz lower maximum operating frequency when compared to the NMOS structure. Although the NMOS topology consumes more current but by reducing the supply voltage the power dissipation significantly reduces due to this reason this topology more attractive for realization in digital technologies with lower supply voltages.

Ali Hajimiri and Thomas H. Lee [22] proposed new physical phase noise model which help to make quantative prediction of phase noise and jitter for different type of oscillators.

III. DESIGN

The CMOS LC VCO circuit(Figure.1) is designed by using S-edit from Tanner EDA. The design CMOS LC VCO is simulated using in 65nm CMOS process. This section briefly discusses the simulated transient response and amplitude, tuning range and power consumption of the cross coupled differential LC-VCO designs. The focus is targeted on the measurement of parameters for CMOS LC VCO design.

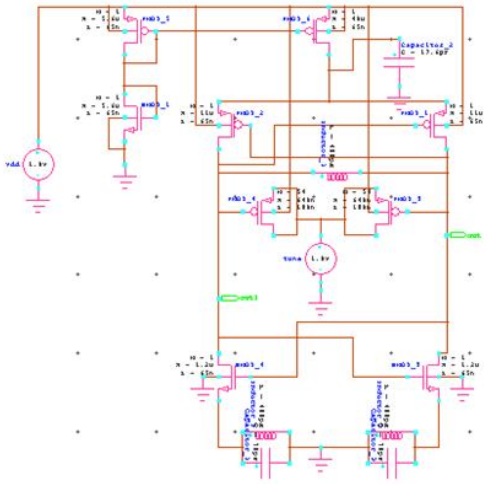

Fig.1 Schematic of LC VCO

Measurement of frequency

The frequency of CMOS LC VCO design can be calculated by transient response as show in Fig.2. For frequency calculation, time period (dx) is directly read by oscillation as show in Fig.2 which is equal to 33 ps at 0.9V. The relation between frequency and time is given below

F=1/T

In the above expression T is time period of oscillation. The time period of oscillation T is equal to dx. Substituting the value of time in above equation frequency comes out to be,

$$F = \frac{1}{33\,ps}$$

$$F = 30.2\,GHz$$

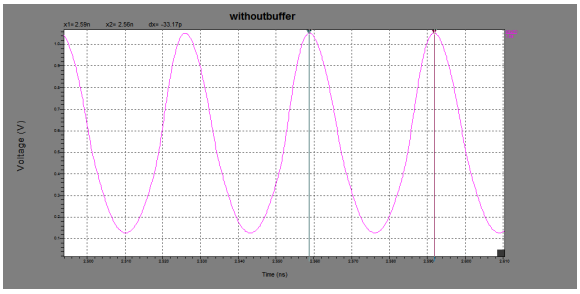

Fig.2 Transient Response of LC VCO

Measurement of tuning range

The fractional tuning range of LC VCO design can be calculated by plotting graph between control voltages and frequencies as show in Fig. 3 by transient analysis.

$$Fractional\ Tuning\ Range = \frac{f_{max} - f_{min}}{f_0} \times 100$$

By the graph is clear that $f_{max}$and f_{min} is 37.2GHz and 28.8 GHz where f_0 is 30 GHz so fractional tuning range can be given by

$$Fractional\ Tuning\ Range = \frac{(37.2 - 28.8)GHz}{30\,GHz} \times 100$$

$$Fractional\ Tuning\ Range = 19\,\%$$

$$K_{VCO} = 2\pi \frac{(37.2 - 28.8)}{(1.0 - 0.0)}$$

$$K_{VCO} = 52.75 \frac{rad}{s} / voltage$$

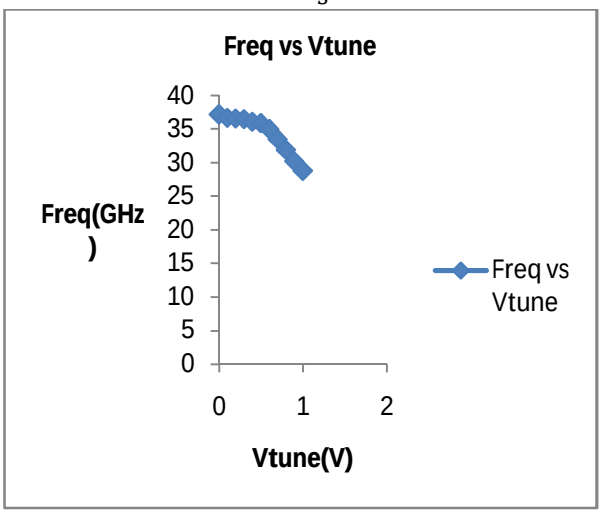

Fig.3 Relationship between voltage & frequency in VCO.

Power Consumption

The power consumption of VCO can be calculated by formula given below

$$\text{max d. c. power dissipation} = V_{supply} I_{bias}$$

It gives total power consumed by the integrated parts in the circuit. The power consumed by this VCO is 1 mW according to formula.

IV. DESIGN

Tabulation of Parameters extracted

CMOS LC VCO design has very low power consumption. The low value of power is obtained due to implementation of cross coupled pair of PMOS transistor in design of LC VCO. This design of CMOS LC VCO has very optimized tuning range. The two PMOS are connected back to back and biased in inversion mode in design. In last area is

computed using L-edit of tanner EDA. The results are summarized in Table 1.

Table 1: Results of CMOS LC VCO.

S.No.	Parameter	Simulation result	
1.	Technology	65nm	
2.	Power Consumption(mW)	1	
3.	Frequency(GHz)	28.8-37.2	
4.	Tuning Voltage(V)	0.0-1.0	
5.	Tuning Range (%)	28	
6.	Phase Noise(dBc/Hz)	@10KHz	-105
		@100KHz	-111
		@1MHz	-112
7.	FOM(dBc/Hz)	-209 @100KHz	

Phase Noise & FOM

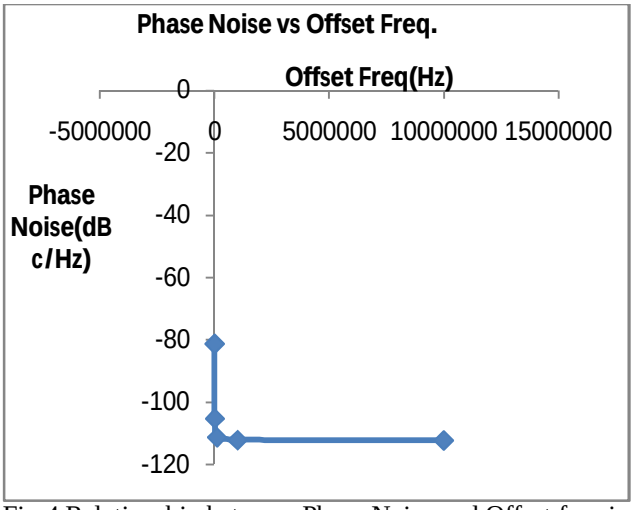

Fig.4 Relationship between Phase Noise and Offset freq in VCO.

Fig. 4 shows that the phase noise at an offset of 10 kHz, 100 kHz, and 1MHz is -105,-111,-112 dBc/Hz, respectively.

FOM of the proposed VCO is -209 dBc/Hz/ at 1 MHz offset from 30 GHz operating frequency that is better than other reported work.

Comparative study of results

Table 2:Comparison of CMOS LC VCO**.**

S.No.	Parameter	Ref. [6]	Ref. [1]	Ref. [13]	Ref. [14]	Ref. [15]	Ref. [16]	Ref. [17]	Ref. [18]	This work
1.	Technology (nm)	350	90	90	90	90	65	180	130	**65**
2.	Supply Voltage (V)	2.5	1.5	1.2	1.8	1.2	1.0	1.5	1.2	**1.0**
3.	Power Consumption (mW)	12.5	3.1	9	0.38	2.9	-	11.31	11	**1**
4.	Frequency (GHz)	1.86	27-32.5	28.7-32.4	25.5 - 35.4	33-40.4	-	15/20/30/40	30.5-39.6	**28.8-37.2**
5.	Tuning Voltage(V)	-	0.0-1.6	0.6	-	0.0-1.3	-	0.0-1.8	0.4-0.9	**1.0-0.0**
6.	Tuning Range(GHz)	-	5.5	3.7	9.9	7.4	-	1.6	9.1	**8.4**
7.	Phase Noise(dBc/Hz)	-	-101.38 @1MHz	-104, @MHz	-105 dBc/Hz@MHz	-103.4 @MHz	-106 dBc/Hz@MHz	-103.8 @MHz	-100.1 @MHz	**-112@1MHz**
8.	FOM(dBc/Hz)	-	-185	-	-	-189	-	-183.1	-189	**-209**

V.CONCLUSION

A CMOS LC VCO is designed in 65nm CMOS process for high frequency application. This design is simulated on S-edit of Tanner EDA tool. In this design inductor with capacitor in parallel is connected to source of NMOS transistors to reduce the phase noise and figure of merit. In this design two P-type MOS varactor implemented to obtain good tuning range at low supply voltage. These two PMOS varactor provide a strong capacitance variation within few hundred of millivolts. This VCO works above 30GHz frequency with control voltage from 0.0 to 1.0V. This design has a very low power consumption of 1 mW.

REFERENCES

[1] Li Zhu, Wang Zhigong, Li Zhiqun, Li Qin and Liu Faen, “IC design of low power, wide tuning range VCO in 90 nm CMOS technology” , Journal of Semiconductors, Vol. 35, No. 12, December 2014.

[2] Neha K. Mendhe1, Prof. M. N. Thakare2, Prof. G .D. Korde3 “ High Frequency Power Optimized Ring

[3] VoltageControlled Oscillator for 65nm CMOSTechnology-Review", International Journal of Engineering Trends and Technology (IJETT) – Volume 8 Number 3-Feb 2014.

[4] Zhou Mingzhu, "A low phase noise wideband VCO in 65nm RF CMOS for low power applications,"in International Conference Microwave and Millimeter Wave Technology (ICMMT), pp. 1 - 4, May 2012.

[5] IjiAyobami B, Forest Zhu, and Michael Heimlich,"Design of Low Power, Wider Tuning Range CMOS Voltage Control Oscillator for Ultra Wideband Applications", IEEE International Conference on IC Design & Technology (ICICDT),pp. 1-4, June 2012.

[6] MrunaliniNandanwar and Deepak Dandekar, "High Performance VCO for Low Power RF Transmitter-A Review", the National Conference on Innovative Paradigms in Engineering & Technology (NCIPET-2012), pp. 22-25, 2012.

[7] M. Moghavvemi and AliyarAttaran"Performance Review of High-Quality-Factor, Low-Noise, and Wideband Radio-Frequency LC-VCO for Wireless Communication [Application Notes]",Microwave Magazine, vol. 12, pp. 130-146, June 2011.

[8] Albert Jerng and Charles G. Sodini, "The Impact of Device Type and Sizing on Phase Noise Mechanisms",IEEE journal Of Solid State Circuits, Vol. 40, February 2005.

[9] Lin Jia, KiatSeng Yeo and ManhAnh Do, "A Novel Methodology for the Design of LC Tank VCO with Low Phase Noise", in IEEE International Symposium on Circuits and Systems (ISCAS), vol. 1, pp 376-379, 23-26 May 2005.

[10] R. Saeidi, N. Masoumi, F. Kalantari and M. S. Oskooei,"Analyzing of Phase Noise in CMOS LC Oscillators" in the 17th International Conference on Microelectronics (ICM), pp. 330-337, Dec. 2005.

[11] Ali Fad, Tord Johnson, Martin Linder and Denny Biberg "A Comparative Study of CMOS LC VCO Topologies for Wide-Band Multi-Standard Transceivers",The47th IEEE International Midwest Symposium on Circuits and Systems, pp. 17-20 July 2004.

[12] A. Hajimiri and T. H. Lee, "Jitter and Phase noise in ring oscillators", IEEE J. Solid State Circuits, 34(6):790-804, June 1999.

[13] Junyi Sun, Chirn Chye Boon, Xi Zhu, Xiang Yi, Khanna Devrishi, and Fanyi Meng,"A Low-Power Low-Phase-Noise VCO With Self-Adjusted Active Resistor" , IEEE Microwave and Wireless Components Letters, 2016.

[14] Junliang Wang, Zhigong Wang, Jian Xu, and Yan Wen, "A 30-GHz Low Phase Noise LC VCO and Frequency Divider in 90-nm CMOS Technology" , PIERS Proceedings, July 6-9, 2015.

[15] Anshuman, Dr. V.V.Shete, "Tuning Range Optimization of a Voltage ControlledOscillator", IEEE,2016.

[16] Zhu Li, Zhigong Wang, Zhiqun Li, Qin Li, "Design of 33-40GHz Low Power VCO in 90-nm CMOS Technology", WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS, Volume 14, 2015.

[17] Dong-Soo Lee, "A low phase noise 30-GHz frequency synthesizer with lineartransconductance VCO and dual-injection-locked frequency divider", Analog Integr Circ Sig Process(2016).

[18] Ro-Min Weng, Yao-Chang Chiang, Hung-Chi Chen, and Ren-Yuan Huang, "A 15/20/30/40 GHz Multi-band Push–Push VCO Using Dual-Resonant LC Resonator", IEEE 4th Global Conference on Consumer Electronics,2015.

[19] Qiyang Wu, "A −189 dBc/Hz FOMT Wide Tuning Range Ka-band VCO UsingTunable Negative Capacitance and Inductance Redistribution", 2013 IEEE Radio Frequency Integrated Circuits Symposium.

[20] Meng-Ting Hsu, Jie-An Hung, and An-Cheng Ou, "Design of 5-GHz CMOS LC VCO with Dual Tuning Circuit", Microwave and Optical Technology Letters, Vol. 56, No. 6, June 2014.