Hardware Co-Simulation of Low Power QPSK Modulator

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Abstract- *QPSK is an extensively used digital modulation method in Wi-Fi communication along with TDMA mobile cell phone, OFDM, Bluetooth, satellite TV for pc communication and many others. Due to its higher noise immunity, bandwidth efficiency and easier circuitry, Speed, electricity and region are the three major elements considered even as designing any digital machine. Low strength devices are continually traumatic for electronic gadgets due to the fact that electricity intake is one of the major elements; the focus is given on reducing the energy consumption of the device. To reduce the energy intake the scale of real block diagram is decreased by using disposing of a few blocks so as to provide the same output signal. In this paper a QPSK modulator is proposed and discussed to enforce on Xilinx ISE 9.2i web version software program tools with the usage of lively HDL coding.*

Keywords- QPSK, VHDL, FPGA, Xilinx

I. INTRODUCTION

Modulation is the technique of sending statistics signal over service signal to reduce the noise or fading impact. They're specifically divided into two classes i.e. analog and virtual. In analog modulation service sign is modulated with the help of analog statistics signal and in digital it modulates with virtual sign. Virtual modulation is known as shift keying because on this, the carrier signal is shifted in amplitude, frequency or phase by virtual enter sign. One of a kind PSKs may be received through M-ary PSK, where M is the number of states or number of phase shifts that is depend upon the number of indicators are blended for modulation.

In QPSK signals are combined for modulation. BER of QPSK is higher than better order PSK signals consisting of eight-PSK, sixteen-QAM, 32-QAM and many others. This can be easily suffering from noise. At higher order PSK, larger bandwidth is require for higher facts switch rate and devour more strength, whereas QPSK is extra bandwidth as well as strength green. There are lots of packages which are used in QPSK modulator, out of which few are of battery operated devices consisting of Bluetooth, TDMA mobile conversation, medical Implant verbal exchange services (MICS) etc. consequently it's miles important to limit the electricity intake of these gadgets so that the battery will remaining for longer time. It can be reduce by decreasing length of circuit or decreasing the rate of operation. The QPSK modulator can modulate two signals in same frequency band as proven in figure 1. Every signal is to be transformed from analog to virtual then modulate one signal with sine and some other with cosine which offers four extraordinary segment shifts with alerts through including those two phase shifted indicators we get QPSK output signal. QPSK signal mathematically expressed as

$$S_{QPSK} = \sqrt{\frac{2E_s}{T_s}} \cos\left(2\pi f_c t + (i-1)\frac{\pi}{2}\right) \quad \ldots(1)$$

For $i = 1, 2, 3, 4$

Where,

$\sqrt{\frac{2E_s}{T_s}}$ = Constant amplitude with E_s energy and T_s time period of the signal, fc= Frequency of carrier signal, i = phase no. of signal as per the symbols of the data signal from the trigonometric equation given below,

$$\cos(A+B) = \cos(A)\cos(B) - \sin(A)\sin(B) \quad \ldots(2)$$

In figure 1 Blocks of QPSK indicates that separate sine and cosine waves are generated which require ROM's. That is then modulated via the entire binary signal. Ones signals are modulated then introduced to generate the QPSK signal. A majority of these method is communicate in with format glide diagram from equation (2) we are able to write

$$S_{QPSK} = \sqrt{\frac{2E_s}{T_s}}\cos(2\pi f_c t)\cos[(i-1)\tfrac{\pi}{2}] - \sqrt{\frac{2E_s}{T_s}}\sin(2\pi f_c t)\sin[(i-1)\tfrac{\pi}{2}] \quad (3)$$

There are two signals in QPSK signal i.e. in phase I(t) and Quadrature phase Q(t). Which is given in equation 3 final signal can be written as

$$S_{QPSK} = \sqrt{\frac{2}{Ts}} \cos(2\pi f_c t)\, I(t) - \sqrt{\frac{2}{Ts}} \sin(2\pi f_c t)\, Q(t)$$

for $i = 1, 2, 3, 4$. Where,

$$I(t) = \sqrt{Es} \cos[(i-1)\frac{\pi}{2}] \text{ and } Q(t) = \sqrt{Es} \sin[(i-1)\frac{\pi}{2}]$$

Output QPSK waveform with 4 unlike phase shifts is as exposed in Table 1. In this, we can see that in support of each symbol phase angle of unique signal is different.

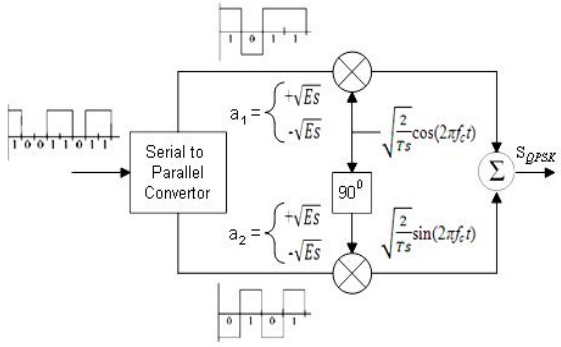

Figure 1: Conventional Block Diagram of QPSK Modulator.

Table 1: Phase shifted signal for different input symbols

Symbol	Bits	S(t)	Phase (Deg.)	Mod. Signal
S1	00	$\sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t + \frac{\pi}{4})$	45⁰	
S2	01	$\sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t + \frac{3\pi}{4})$	135⁰	
S3	11	$\sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t + \frac{5\pi}{4})$	225⁰	
S4	10	$\sqrt{\frac{2Es}{Ts}} \cos(2\pi f_c t + \frac{7\pi}{4})$	315⁰	

II. PROPOSED WORK

we will see, day by day the digital devices are getting smaller, many studies is going on to minimize the dimensions of the design which reduce the power consumption of the device, subsequently price of the device gets reduce. If we observe the QPSK output waveform, we found that there may be a sinusoidal wave transferring with the trade in symbol and the section angle is equal for one of a kind symbol as proven in fig. 4, method we are able to say that, for specific image there can be precise phase shift output sign [1]. So, as opposed to producing the section shift by means of multiplying information signal with carrier one, we will simply shop the sign in ROM and get in touch with it for precise symbol from specific segment. It means the output waveform can be the equal sinusoidal sign with beginning from precise phase perspective.

In this example we don't require multiple ROM to keep our signal considering that it's far most effective the sinusoidal sign [2]. We just have to begin the output signal from one-of-a-kind segment attitude according to enter symbol (00, 01, 11, 10). The phase shift perspective can be 0°, 90°, 180° and 270° degree or it is able to be 45°, 135°, 225° and 315°. In proposed block diagram as shown figure 2, we're transferring signal from 45°. The constellation diagram in figure 3 shows the phase attitude and amplitude of signal for different symbols. In above diagram the section angles are 45, 135, 225 and 315 degree for "0 0", "01", "11" and "10" respectively. The symbols are taken as gray codes i.e. one bit trade in step with image or 90° section shift consistent with image Above table shows the phase trade of the sign is depend upon the change in symbols, each symbol is having particular section perspective or sign sample. The dimensions of the layout is reduced up to a whole lot quantity, number of blocks are few in comparison to standard block diagram [3]. In proposed block diagram simplest one ROM is used for provider sign rather than ROMs for sine and cosine sign generator.

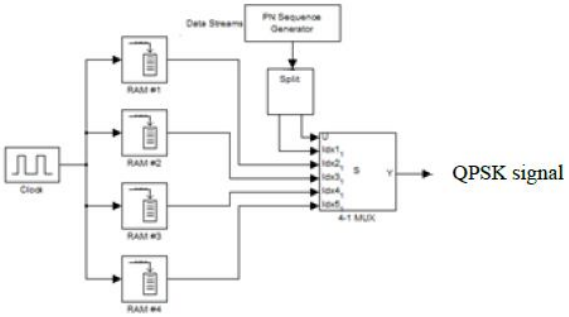

Figure 2: Proposed Block Diagram of QPSK Modulator.

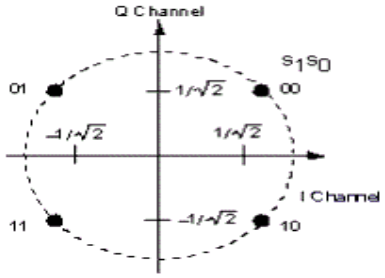

Figure 3: Constellation Diagram of QPSK Signal.

a) **Carrier Source:** It affords a sinusoidal carrier sign of specific frequency that's modulated with the aid of the data sign. A ROM is used to save the amplitude values of the sign which may be study by using VHDL coding for FPGA to provide sine sign. On board frequency is in MHz that is high to have a look at the output signal on DSO, a shift sign up may be growing to provide various frequency alerts.

b) **Phase shifter:** It shifts the sine sign into 4 one-of-a-kind angles as proven in fig. five. it's far not anything but the ROM which saved the sinusoidal signal and we are sending the signal on the output with different starting point of signal or special phase attitude that's precise for exclusive symbols. Truly it is a DMUX which takes one input as service signal i.e. sinusoidal sign and giving output as special segment shifted sinusoidal signal. Those output are decided on by means of select strains that are input signals I and Q.

c) **Shift register:** almost we take enter records alerts to modulate them with identical provider signal, however on board we need to generate two indicators from a random signal. Here we are taking one facts signal and keeping apart it into two sign i.e. Serial in parallel out (SIPO).

d) **Multiplexer:** It selects best one sign at a day trip of 4 shifted signals and gives as output QPSK signal. The sign is chosen through two choose lines I and Q, method output might be the phase shifted sign according to the input symbol.

e) **Digital to Analog Converter (DAC):** To put all the designed blocks into Field Programmable Gate Array (FPGA) packages which gives output digital QPSK signal, so we need to convert it into analog form using DAC. The waveform can be determined on DSO. The ROM incorporates values of sinusoidal signal, it calls for a clock to examine the values i.e. one value in line with clock pulse, similarly shift sign in require a clock sign to take enter statistics signal then

$$T = \frac{1}{f_c} * x = T_d$$

Where,

T = Time period of sine signal.

x = No. of values stored in the ROM.

f_c = clock frequency applied to carrier signal.

T_d = Time period of data signal.

To divide the frequency a divider block with issue x is required to design, it'll take the enter clock frequency f_d that is to be divided through x to get the frequency identical to frequency of sine signal. In this paper, active HDL tool is located to generate the blocks with VHDL coding. The FPGA kit might be use to implement these blocks on hardware to have a look at the output waveform [5]. But the FPGA is a digital circuit which offer virtual output sign subsequently we need a DAC to covert this sign to analog one and block diagram and check its output waveforms observe on Xilinx ISE Starter 9.2I version software [4].

III. IMPLEMENTATION AND RESULTS

Proposed design and conventional QPSK modulator modeled with HDL and simulated on Xilinx ISE platform. The crucial for simulate the conventional QPSK modulator is for comparison with the proposed architecture in term of power and area utilization in FPGA. Each of the design HDL code synthesizes and tested with a test bench code to simulate it functionality [6]. The synthesizable code translated into RTL (Register Transfer level) schematic diagrams while the Xilinx simulator used to run the test bench code to obtain timing diagram. The simulator also used to produce the decimal data which later used in Microsoft office Excel to plot the waveforms.

Figure 4 shows the RTL obtain from synthesize HDL code for Proposed QSPK modulator while figure 5 shows a portion of timing diagram where the data (even and odd) change from 00 to 01. The QPSK wave is represented as sum (concatenation of Cout and S) of I and Q phase in the timing diagram. Decimal data collected for QPSK wave, I and Q phases from the timing simulation used to plot the waveform [7].

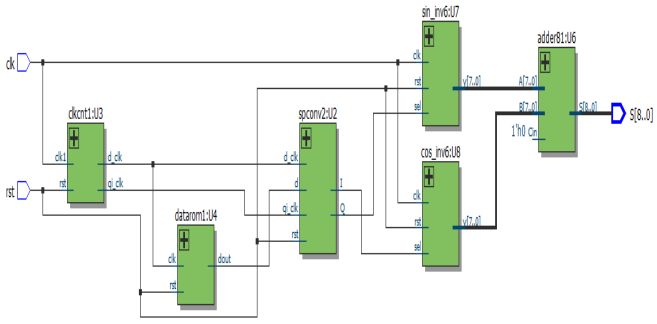

Figure 4: RTL obtain from synthesize HDL code

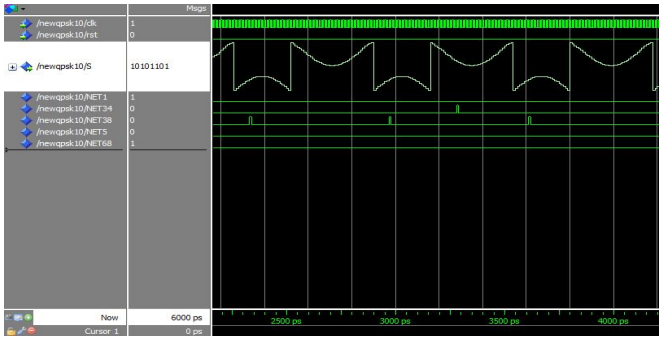

Figure 5: Timing analysis demonstrates a portion of even and odd data transition.

IV. RESULT COMPARISONS

Power consumption and area utilization is 2 main criteria studied in this project. Both criteria play major roles when the FPGA design translated into ASIC.

1) **Power:** Power estimator tool usually used in the predesigned and implementation phases of this project. While the Power Analyzer (XPA) tool performs power estimation at post implementation stages [10]. It is the most accurate tool since it can read from the implemented design database the exact logic and routing resources used for a design. The last power analyzer tools provided by xilinx are PlanAhead RTL power estimator. This software provided earlier stages of power and area utilization of a design at RTL level. PlanAhead reads the HDL code from a design to estimate the resources needed, and reports the estimated power from a statistical analysis of the activity of each resource [12]. Since the PlanAhead provide an earlier power consumption and area utilization analysis at same time, the software used instead of the other two power tools analyzer. Figure 6 shows the power comparison between the proposed and conventional QPSK modulator. Its Cleary shows that the power consumption for proposed. The power analysis mainly carried out on device static power or leakage power where the transistor in FPGA uses to hold the device configuration. However it is also known that the FPGA consumed more power compare to ASIC [13]. The power consumption is high in FPGA due to it flexibity in configuration and rerouting. So when the proposed design implemented in ASIC where only dedicated number of transistor used for that design, more power consumption can be reduced.

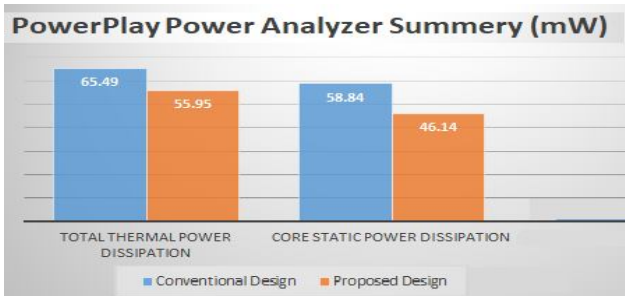

Figure 6: Power dissipation of 64 values ROM proposed design and Conventional Design

2) **Area:** Area employment by number of gates in FPGA can directly influence the power consumption, reliability and the cost of a design. A simple design can cut or reduce the number of gates occupied in FPGA and at the same time increase the performance indirectly. The proposed architecture dramatically consumed more less gates compare to the conventional. Power consumption is still less when compared. This is mainly because the architecture proposed does not employ DDFS, DSP48 and arithmetic logic blocks as in the conventional design [13] [14]. Figure 7 shows the number of LUT and I/O used for the proposed and conventional architecture.

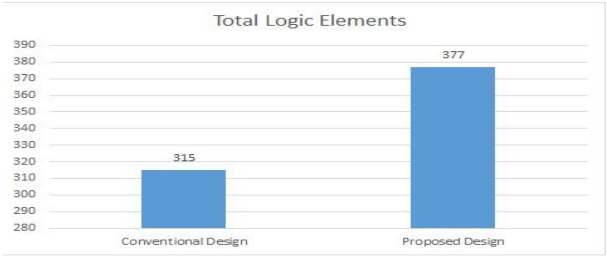

Figure 7: Device utilization of 64 values ROM proposed design

V. CONCLUSION

The proposed QPSK modulators successfully simulated on Xilinx ISE 9.2i software platform and the results obtain shows that the output waveform is same as conventional QPSK modulator. The power analysis tools used on analyze the power consumption and area utilization on the proposed modulator also gives positive feedback. proposed architecture consume less power when compared with conventional architecture. As for future plan, both designs will be implemented on virtex 6 FPGA board and RF front end module will be used to transmit the baseband data. A functional demodulator also will be constructed to retrieve the wirelessly transmitted baseband data. As per Results Proposed Design is having Higher size as compared to others, It consume lowest power, It is having highest speed of operation

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