Simulation of Low Power QPSK Modulator By Using Xilinx ISE: A Review

Kiran M. Chaudhari[1], Komal Kanojia[2], Dr. Manish Jain[3]
[1]Dept of ECE
[2]Assistant Professor, Dept of ECE
[3]Head Of Department, Dept of ECE
[1, 2, 3] RKDF Inst.of Sci.and Tech.,Bhopal,MP (India)

Abstract- *The modulators are the basic requirement of the communication systems they are designed to reduce the channel distortion and to use in RF communication, hence many types of carrier modulation techniques has been already proposed according to channel properties and data rate of the system. This paper presents a study of different concepts of FPGA implementation of QPSK modulator based on simulation with Xilinx system generator. The different way of designing QPSK modulator are discussed in details along with its respective concerts such as low power, reduced hardware and many application oriented approaches.*

Keywords- QPSK, VHDL, FPGA, Xilinx

I. INTRODUCTION

The modulators are the basic requirement of the communication systems they are designed to reduce the channel distortion & to use in RF communication hence many types of carrier modulation techniques has been already proposed according to channel properties & data rate of the system. QPSK (Quadrature Phase Shift Keying) is one of the modulation schemes used in wireless communication system due to its ability to transmit twice the data rate for a given bandwidth. The QPSK is the most often used scheme since it does not suffer from BER (Bit Error rate) degradation while the bandwidth efficiency is increased. It is very popular in Satellite communication. As the design of complex mathematical models such as QPSK modulator in „pure HDL" is very difficult and costly; it requires from designer many additional skills and is time-consuming. Even though QPSK modulator consumes less power in a present devices but for system such as satellite and mobile devices where their operations are power limited, this can be an issue at high power. Many implementations have been reported in the literature for implementation of QPSK modulator on FPGA at low power in which QPSK modulator is simulated with Xilinx System Generator Simulink software and later on it is converted in Very high speed integrated circuit Hardware Descriptive Language to implement it on FPGA. After successful implementation, the parameters are analyzed on Xilinx ISE software.

For implementation of QPSK modulator on FPGA several techniques have been developed to improve performance but all requirements were not satisfied. For example the QPSK modulator is implemented using VHDL codes in Xilinx and analog filter simulation in Matlab which gives less complexity of design but at high power. In order to overcome these types of difficulties, the QPSK modulator is designed by using Hardware co-simulation at less operational power.

II. LITERATURE REVIEW

From the review of related work and published literature, it is observed that many researchers have performed implementation of QPSK modulator on FPGA by applying different techniques like using analog filters, elimination of DSS (Direct Digital Synthesizer). Researchers have undertaken different systems, processes or phenomena with regard to design of QPSK Modulator and attempted to find better outcome. Since in the real world today Digital communication systems are very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing Low Power.

Implementation QPSK modulator is a process of Complex Mathematical Models Simulation on Mixed HDL-Simulink Platform, which can be one of the best solutions on problems occurring in simulations of models in pure HDL, which is very difficult, costly and time-consuming. So, for these types of problems, alternative approach has been developed based on mixed HDL-Simulink platform where the basic properties of the simulation process in Simulink are addressed and problems of data and signal transfers, driving samples, synchronization and entire communication between HDL and Simulink are described in details. The simple inter-process communication makes use of mechanisms implemented in the operating system. Optimizations have been introduced to overcome the performance limitation of the

inter-process communication protocol. The implemented conversion functions, responsible for data representation, are flexible, accept all Simulink types and cover a wide range of HDL types [Adam Milik, and Andrzej Pulka, 2008].

A simple model is designed for a Quadrature Phase shift Keying (QPSK) modulator applied for implantable telemetry applications in which VHDL programming code is used to generate QPSK digital signal. The input test signals data and carrier are interfaced to the CPLD and FPGAs board from Agilent function generator (E8408A) and the local clock oscillator is used for test, which is operating at 25.175 MHz and used 12.5MHz for the carrier and 2Mbps reduced for data source. The advantages of this modulator are it can be reconfigured and upgraded to improve the data rate [Gihad Elamary 2009].

The architecture has been developed by Teena Sakla and Divya Jain which presents a FPGA based QPSK modulator with Analog filters; which has many advantages over traditional QPSK modulators such as reduced cost, better stability, less complexity. The simulation of the system proves all the features mention above. The System is designed using VHDL codes in Xilinx & analog filter simulation in Matlab. The implementation of digital QPSK Modulator is done on XILINX 11.1i.The results are verified by test bench generated by the FPGA. Then the Analog filter is simulated by using MATLAB 7.5It can be concluded that the designed RTL model for QPSK Modulator is accurate and can work for real time application [Teena Sakla, 2010].

Wenmiao Song and Qiongqiong Yao have designed the QPSK system for Spread spectrum communication which uses field programmable device. The whole system is divided into several small models based on top-down design method, and using VHDL hardware description language for designing each model. The direct digital synthesis (DDS) is used to design orthogonal cosine signal module. In demodulator, the low pass FIR filtering is used to filter high frequency component. The whole system has been simulated in the Quartus II7.2 simulation environment and successfully downloaded to the chip of the Cyclone II EP2C5F256C6.This method is used for improving the efficiency, to reduce developing period and cost but use of DSS is responsible for consuming more power.[Wenmiao Song, 2010].

The digitally implemented QPSK modulator is developed for satellite communication for future satellite missions. This design in new approach minimizes the component count and hence reduces the PCB size, power and bandwidth which is mainly useful for space application. Realization of hardware blocks like CCITT V.35 Scrambler, Differential Encoder, ½ rate convolution Encoder, Sine and Cosine subcarrier generation, assignment of symbols with respect to I and Q data, their additions to obtain QPSK streams are digitally implemented inside an FPGA using suitable high frequency sampler. At the last end, the digital QPSK stream is converted to analog and the modulated signal obtained from it, is suitably translated to required carrier frequency [K. Monpara, S. Parmar, 2010].

Another important way for designing QPSK modulator on FPGA is by using algorithm implemented on FPGA with the VHDL language on Xilinx ISE 12.3. The local clock oscillator of the board is 50 MHz which corresponds with a period of 20ns. The frequency of the QPSK carrier is 31,250 kHz and because the QPSK symbol is made of two bits, the output frequency is 62,50kbps. The QPSK Modulator is then simulated using Matlab/Simulink environment and System Generator, a tool from Xilinx used for FPGA design as well as implemented on a Spartan 3E Starter Kit board. But this architecture does not forbid the effect of AWGN causing distortion in result. [S. O. Popescu, 2011].

Later on, researchers have presented a design on QPSK digital communication system and its implementation on FPGAs. Simulation of the system was made in MATLAB/Simulink environment and system generator is used as FPGA design tool. The system is designed by using two Spartan 3E Starter Kit boards, where first is implemented to comport as a modulator and the second as a demodulator and modulator and the second as a demodulator and VHDL hardware descriptive language was used for designing [A. S. Gontean and D. Ianchis, 2011].

The model has been designed on a modulator-demodulator circuit which can execute different modulation schemes like- AM, ASK, BPSK, FSK & QPSK. Both the LUT based implementation and complete VHDL based implementation has done by using digital high frequency carriers. In the first step, realization of whole modulation and demodulation schemes using MATLAB Simulink is done and later on the format of a VHDL program is built around the concept of blocks which are the basic building units of a VHDL design. The carrier used is also digital high frequency square wave signal. As a result the total realization is much faster than other technique which uses Analog signals and Analog circuits. [Swapan K Samaddar, 2012].

Another important application of QPSK modulator is for designing the Software defined radio (SDR) based modulator because SDR technology enables implementation of wireless devices that support multiple air interfaces and modulation formats, which is very important if consider

proliferation of wireless standards. This modulator is designed and implemented with the help of Altera Cyclone IV FPGA and Altera DSP Builder Tool combined with Matlab/Simulink, Model sim and Quartus II design tools. This makes the use of SDR based modulators simpler and faster. [Tarik Kazaz, 2013].

The architecture has been designed on BPSK and QPSK digital Modulation scheme and it is implemented on FPGA.MATLAB is used for simulation of the system and System generator is used as a tool for FPGA design. This system gives the hardware realization of such digital modulation scheme with minimum area strategy which is beneficial for mainly universal mobile telecommunication system (UMTS), CDMA2000 and SDR applications. Hardware co-simulation is designed using VHDL and is verified using MATLAB simulink [G. Purohit, D. Vyas 2013]. The researchers have given the model on simulation of QPSK Modulator to generate real and imaginary channel which is done using Xilinx ISE and VHDL language is used for simulation. The modulated signal obtained in the form of I and Q channel. Different data streams are applied at the input and both real and imaginary parts are observed. The use of work is to develop a system to modulate the data using FPGA so that security can be provided to the data as well as to improve the data rate of the communication and by using FPGA implementation, power requirement can be minimized and operation can be speed up [T. Kafare, V. Joshi, 2013].

Low power consumption might be the first demand of advanced communication techniques. Based upon this requirement architecture is developed on FPGA implementation of low power digital QPSK modulator using Verilog HDL. This modulator successfully modeled with verilog Hardware Descriptive Language (HDL), simulated with Xilinx ISE v.12.4 software and implementation on Spartan 3E board. The measured performances of modulator show the proposed architecture consumes significantly 32 mw less power than conventional architecture. The power reduction can be achieved due to less usage of input/output logic block in FPGA conjunction with the elimination of DDS (Direct Digital Synthesizer) in new design. [Asaraf Mohamed Moubark, 2013].

From the careful study of reported work, it is observed that researchers have proposed different techniques to design the QPSK Modulator on FPGA to improve its characteristics and various parameters. But up to the result of this survey regarding such type of Modulators design, no one had suggested use of Hardware Co-simulation technique which provides compactness of system at less operational power.

It can be seen that many advanced changes are taking place in Digital Communication techniques in order to increase its use in the real time applications. By scaling down the technology, we can optimize the parameters like power consumption. The current technology up to 2013 has given the design of QPSK modulator having power 32mw less than that of conventional architecture. Hence considering the advancement of future technology and the advantage of Hardware Co-simulation technique the architecture has been decided to operate with less power to make QPSK modulator more efficient. Considering all this constraint regarding the demand of today's fast communication world, the research has been taken to design low power QPSK Modulator on FPGA by using Hardware Co-simulation.

III. CONCLUSION

The main purpose of this paper was to study a complete model of one of the most commonly used modulation schemes in satellite communication systems, QPSK Modulator and Demodulator. It has been designed, simulated, and tested using MATLAB Simulink. The key indicator of our model performance, such as Bit Error Rate (BER), constellation diagram, and eye Pattern, have been generated and analyzed. BER curve closed to the theoretical one, the constellation diagram had four points in one cycle which mean it has a constant envelope and this leads the system not to suffer from attenuation. Moreover, these points satisfy Gray code which provides minimum BER. On the other hand, the model was not affected by Intersymbol Interference. This was observed by the opening eye in eye pattern.

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