Performance of CNTFET Based Inverter in Nanometer Regime

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Abstract- *The review of the CNTFET inverter on rise time and fall time can be perform. Also we analyze PVT variation of CNTFET technology. In that we analyze performance of CNTFET inverter under the variation of temperature and oxide thickness. The power consumption of circuit can also be analyze. The influence of variation of parameters on the characteristics of CNTFET inverter is simulated and analyzed using H-SPICE tool and Stanford nano model-39 of CNTFET*

Keywords- Carbon nano-tube CNT; CNTFETs; temperature; oxide thickness.

I. INTRODUCTION

The scaling of devices has shrunk the device size considerably over the time and integration of number of transistors into the chip has increased drastically. As a consequence there is tremendous increase in leakage currents, high power consumption and reduced reliability of the devices. Silicon technology continues to scale down and is a dominant choice for high-performance digital circuits. These challenging aspects leads the researcher to investigate the performance of nano scaled devices. Carbon nanotubes (CNTs) have been explored as a promising candidate for the same. As CNTFETS whose diameter is ranging from 1 to 3 nm and the length can be up to several micrometers, CNTFETS can also be used as interconnections because of their higher carbon- carbon bond strength and scalable feature. The idea of implementing logic circuits with CNTFETS is to overcome the limitations of traditional silicon MOSFETS with modification in channel material by introducing a single CNT into the channel. As the MOSFET suffers with short channel effects due to scaling, the replacement of the channel with a CNT, not only facilitate the device to scale down to nano regime but also offers efficient performance due to its better electrical properties.

The effect of change in temperature and oxide thickness has little effect on rise and fall time of the inverter. The leakage power consumption of the CNTFET inverter is very small [1]. It is found that with decreasing in diameter power reduces but with a delay penalty [2-4]. CNTFET has some unique property of decreasing quantum capacitance, while reducing the thickness of oxide which is not possible in MOSFET [3]. and effect of variation of chiral vector on threshold voltage in CNTFET devices its found that at low value of chiral pair the threshold voltage is higher, whereas at high value of chiral vector the threshold voltage comes lower and the effect of temperature on threshold voltage is very less or negligibly small[3-5]. CNTFET inverter has ideal response with Vst=Vdd/2=0.6V whereas CMOS technology inverters switch at slightly higher values and has slower switching compared to CNTFET [6].The I-V characteristics of CNTFET are identical to that of MOSFET and the heavily doped CNTs are placed between gate and source/drain regions to have a low series resistance in ON state [7]. [8] Has analyzed using nanoHUB tools and justified the advantage of CNTFET device over MOSFET device in nanometer regime and concluded that the CNTFET has the potential to lead the post-CMOS device domain. The geometry-dependent threshold voltage of CNFETs has been effectively used to design a ternary logic family [10].

II. STRUCTURE OF CARBON NANO TUBE TRANSISTOR

Fig.1 depicts the structure of a CNTFET device [3] the channel region under the gate dielectric of a conventional MOSFET has been replaced by a CNT. The length and diameter of the CNT will decide the feature size.

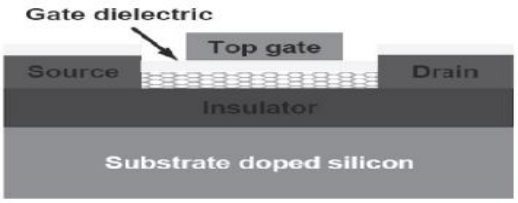

Fig. 1 Structure of CNTFET Device

For determining the diameter of a SWCNT, we can draw a carbon molecule as a regular hexagon in a circle as shown in Fig.2 [11].

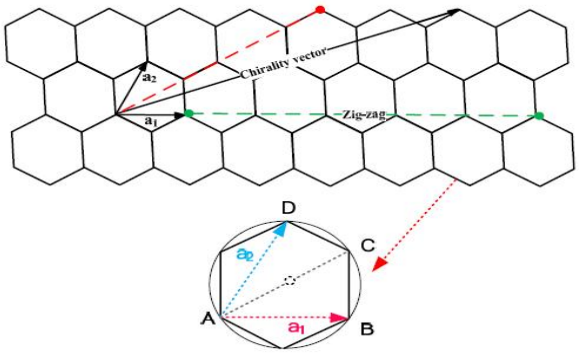

Fig.2 Unrolled graphite sheet.

In this figure triangular ABD is isosceles, so a1= a2. By considering the rectangular triangle ABC and by means of triangular relationship |a1| and |a2| is determined as:

$$a_1 = a_2 = 2a_0 \sin(60^\circ) = \sqrt{3}a_0$$

The chiral vector is calculated as:

$$Ch^2 = a_1^2 n_1^2 + a_2^2 n_2^2 + 2a_1 a_2 n_1 n_2 \cos(60^\circ)$$

$$Ch = \sqrt{3}a_0 \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad \ldots.1$$

Where, a0 shows the carbon to carbon atom distance. The diameter of a CNT can be calculated according to the following relation

$$D_{CNT} = \frac{\sqrt{3}a_0 \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \quad \ldots.2$$

Structure and operation of the carbon nanotube field effect transistors are more similar to traditional silicon transistors but the conduction channel in CNTFETs is consists of semiconducting SWCNTs. Threshold voltage of a CNTFET is approximately calculated as:

$$Vth \approx \frac{E_g}{2e} = \frac{\sqrt{3}\, a_0 V_\pi}{3\, eD_{CNT}} \approx \frac{0.43}{D_{CNT}(nm)} \quad \ldots.3$$

The energy bandgap (E_G) in eV of CNT is given as [4]

$$E_G = 0.84/D_{CNT} \quad \ldots.4$$

For conduction to start, the barrier at source channel junction has to be overcome energy EG/2 (=Δ1, say). As barrier height determines the threshold voltage of an FET. Transconductance gm of a CNTFET is given by equation [12]

$$g_m = \frac{\mu \left(\frac{C_{gg}}{L}\right)}{\left(\frac{V_{ds}}{L}\right)} \quad \ldots.5$$

III. CNTFET INVERTER

The digital inverter is the basic building block of logic circuits and it has been simulated in HSPICE with 32nm technology using Stanford models. The CNTFET inverter is depicted in Fig-3 is structurally identical to that of CMOS inverter except that the channel region is replaced by a SWCNT or MWCNT [6].p-CNTFET forms the pull up device and n-CNTFET forms the pull down device as depicted in fig.3.A pulsed signal with an initial value 0 volt and final value of 1 volt is provided at the gate terminal to observe the output and transfer characteristics of the circuit.

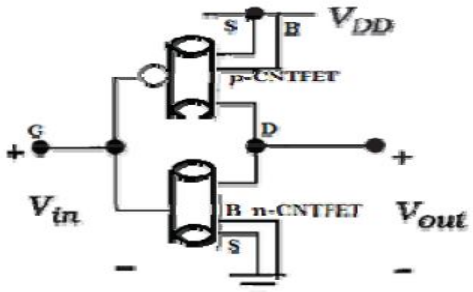

Fig. 3 CNTFET Inverter

IV. H-SPICE SIMULATION ANALYSIS AND RESULT

A. Effect of temperature on power and rise time and fall time of CNFET inveter

In this analysis we have considered the model parameters as depicted in table1.Stanford model files were used and the standard model parameters considered for the design are depicted in table-1.

Table-1 Standard model parameters considered for the performance analysis of CNTFET inverter

Sr. No.	**Parameter description**	value
1	Vdd	1volts
2	Pitch	20nm
3	Oxide thickness	4nm and 3nm
4	Ccsd-coupling capacitance between channel and substrate	20Pf/m
5	Ccsd- Coupling capacitance between source and drain	0
6	Kgate-dielectric constant of Gate	16
7	Ffi- fermi level of doped S/D	0.6eV
8	Lch= Physical channel length	Considered 32nm and 22nm
9	Temperature	Varied between -100°C to +100°C

To analyze the inverter performance at different temperatures, 32nm and 22nm CNTFET inverter are designed and the temperature is varied as depicted in table-1 for the oxide thickness of 3nm and 4nm.

Fig-4 describes the variation of power with respect to variation of temperature for 32nm

CNTFET with oxide thickness= 4nm

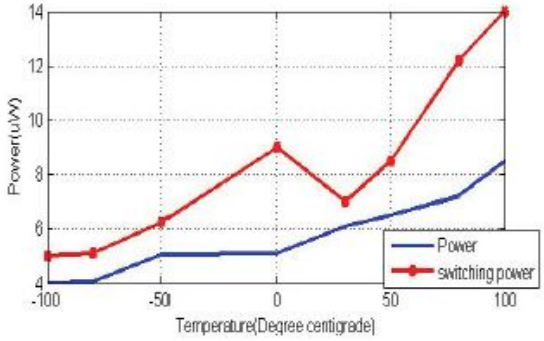

Fig. 4 Variation of CNTFET power with respect to temperature.

Fig-5 describes the variation of Rise time and fall time of inverter with respect to variation of temperature for 32nm

CNTFET with oxide thickness= 4nm

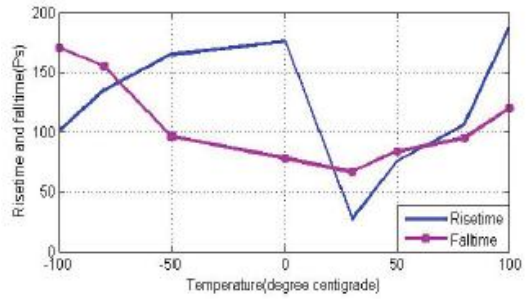

Fig. 5Variation of rise time and fall time with respect to temperature.

Fig.6 describes the variation of power with respect to variation of temperature for 32nm CNTFET with oxide thickness= 4nm.

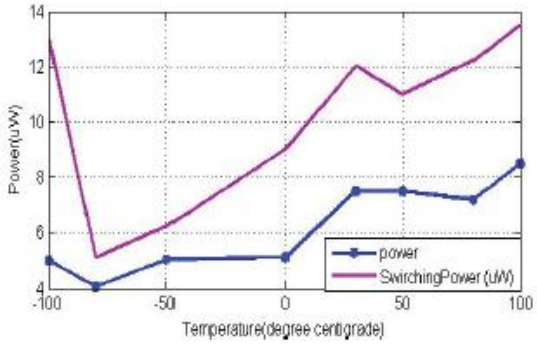

Fig. 6 Variation of CNTFET power with respect to temperature.

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Fig-7 describes the variation of Rise time and fall time ofinverter with respect to variation of temperature for 32nm CNTFET with oxide thickness= 3nm

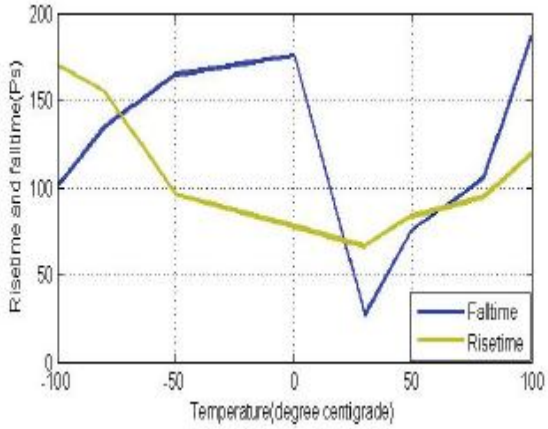

Fig. 7Variation of rise time and fall time with respect to temperature.

The performance analysis of the CNTFET inverter reveals that it has very low power consumption and faster rise and fall time for its characteristics and assures it to be a promising candidate for the nano circuit design.

IV. CONCLUSION

This paper compares the performance parameters of 32 nm CNFET inverter under temperature and oxide thickness variation.

From fig.4 the power consumption of the inverter varies from 4μW to 8.5μW under temperature variation.it reveals that the circuit consumes very low power. fig.5 infer that rise time logic transition varies from 100ps to 185ps at minimum and maximum value of temperature. The fall time of logic transition varies from 170ps to 120ps at minimum and maximum values of temperature. CNFET has near reliable performance and stable operation under temperature variation. Entire analysis is carried out by reducing oxide thickness to 3nm. fig.6,7 depict the performance analysis for 3nm oxide thickness.

V. REFERENCES

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