Efficient Coding Scheme For Low Power Shift Registers

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Abstract- *A master-slave flip-flop using two latches can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem*

This technique proposes a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register using pulsed latches was fabricated using CMOS process. The proposed shift register saves area and power compared to the conventional shift register with flip-flops.

I. INTRODUCTION

A SHIFT register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receiver, and image processing IC. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

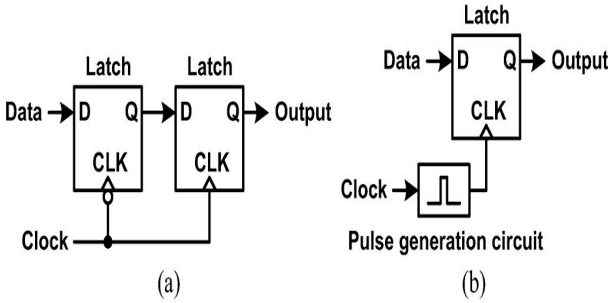


Figure 1. a master-slaveflip-flop. b pulsed latch.

This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

II. PROPOSED SHIFT REGISTER

A master-slave flip-flop using two latches in Fig.1.1 can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig.1.2 All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 4. The shift register in Fig. 4.1.(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 4.2.(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant

during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width. One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 4.2.(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 4.2.(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock.

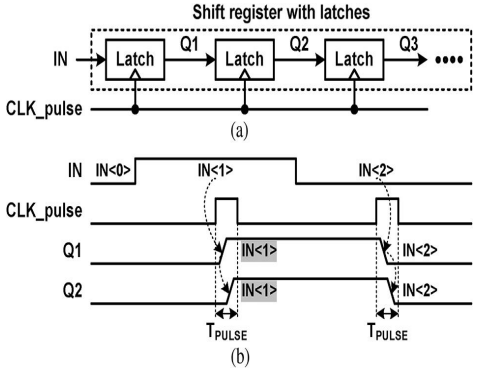


Figure 2. Shift register with latches and a pulsed clock signal. (a) schematic. (b) waveforms

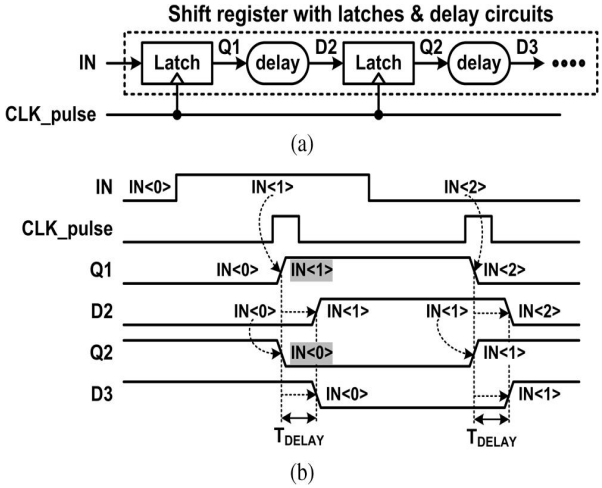


Figure 3. Shift registers with latches, delay circuits, and a pulsed clock signal (a) schematic. (b) Waveforms

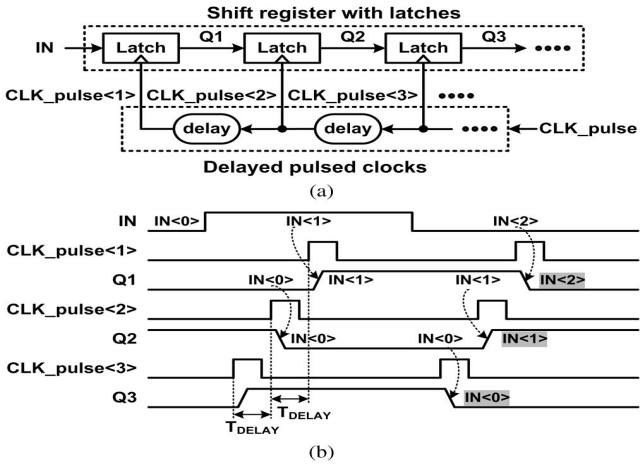


Figure 5. Shift Register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.

`Pulse and no timing problem occur between the latches. However, the delay circuits cause large area and power overheads. Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 4(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. Fig. 5(a) shows an example the proposed shift register. The proposed shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse□1:4□ and CLK_pulse□T□). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2.

Fig.4.3.shows the operation waveforms in the proposed shift register. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator in fig. 4.4. The sequence of the pulsed clock signals is in the opposite order of the five latches. Initially, the pulsed clock signal CLK_pulse□T□ updates the latch data T1 from Q4. And then, the pulsed clock signals CLK_pulse□1:4□ update the four latch data from Q4 to Q1 sequentially. The latches Q2–Q4 receive data from their previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register. The proposed shift register reduces

the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. As shown in fig. 4.3each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. When an shift register is divided into sub shift registers, the number of clock-pulse circuits is and the number of latches a sub shift register consisting of latches requires pulsed clock signals. The number of sub shift registers becomes, each sub shift register has a temporary storage latch.

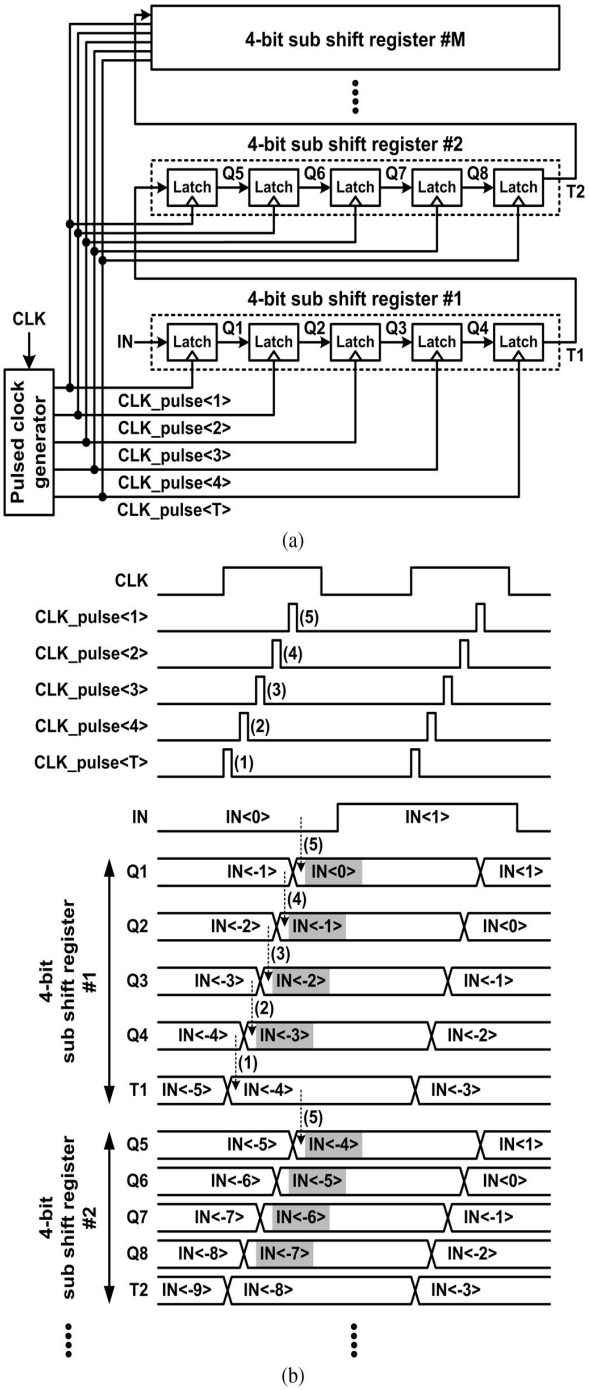


Figure 6. Shift register with delayed pulsed clock generator (a)Schematic (b)waveforms

Therefore, latches are added for the temporary storage latches. The conventional delayed pulsed clock circuits can be used to save the AND gates in the delay. However, in the delayed pulsed clock generator in fig.4.5 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals. The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register .is selected by considering the area, power consumption, speed. The area optimization can be performed as follows. Whenthe circuit areas are normalized with a latch, the areas of a latch and a clock-pulse circuit are 1 and T, respectively. The total area becomesoptimal for the minimum area is obtained from the first-order differential equation of the total area.

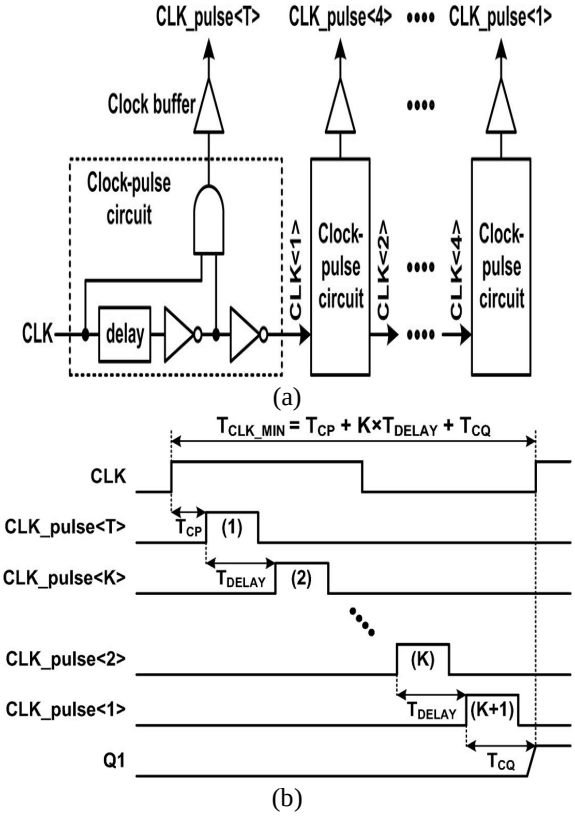


Figure 7. (a) Delayed pulsed clock generator (b) Waveforms

Minimum clock cycle time of the proposed shift register. The power optimization is similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit are 1 and , respectively. The total power consumption is also an integer for the minimum power is

selected as a divisor of , which is nearest to . In selection, the clock buffers in Fig. 6 are not considered. The total size of the clock buffers is determined by the total clock loading of latches. Although the number of latches increases from to, the increment ratio of the clock buffers is small. The number of clock buffers is. As increases, the size of a clock buffer decreases in proportion to because the number of latches connected to a clock buffer is proportional. Therefore, the total size of the clock buffers increases slightly with increasing and the effect of the clock buffers can be neglected for choosing. The maximum number of is limited to the target clock frequency. As shown in fig.5.2 the minimum clock cycle time is where is the delay from the rising edge of the main clock signal (CLK) to the rising edge of the first pulsed clock signal (CLK_pulseT), is the delay of two neighbor pulsed clock signals, is the delay from the rising edge of the last pulsed clock signal (CLK_pulse) to the output signal of the latch Q1. is proportional to . As increases, the maximum clock frequency decreases in proportion to. Therefore, must be selected under the maximum number which is determined by the maximum clock frequency of the target applications. The pulsed clock signals are supplied to all sub shift registers. Each pulsed clock signal arrives at the sub shift registers at different time due to the pulse skew in the wire. The pulse skew increases proportional to the wire distance from the delayed pulsed clock generator. All pulsed clock signals have almost the same pulse skews when they arrive at the same sub shift register. Therefore, in the same sub shift register, the pulse skew differences between the pulsed clock signals are very small. The clock pulse intervals larger than the pulse skew differences cancel out the effects of the pulse skew differences. Also, the pulse skew differences between the different sub shift registers do not cause any timing problem, because two latches connecting two sub shift registers use the first and last pulsed clocks (CLK_pulse T and CLK_pulse) which have a long clock pulse interval.

In a long shift register, a short clock pulse cannot through a long wire due to parasitic capacitance and resistance. At the end of the wire, the clock pulse shape is degraded because the rising and falling times of the clock pulse increase due to the wire delay. A simple solution is to increase the clock pulse width for keeping the clock pulse shape. But this decreases the maximum clock frequency. Another solution is to insert clock buffers and clock trees.

The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flip flops to reduce the area and power consumption. In chip implementation, the SSASPL (static differential sense amp shared pulse latch) in Fig. 5.3, which is the smallest latch, is selected. The original SSASPL with 9 transistors [6] is modified to the SSASPL with 7 transistors in Fig.5.3 by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal. The SSASPL updates the data with three NMOS transistors and it holds the data with four transistors in two cross-coupled inverters. It requires two differential data input (D and Db) and a pulsed clock signal. When the pulsed clock signal is high, its data is updated. The node Q or Qb is pulled down to ground according to the input data (D and Db). The pull-down current of the NMOS transistors must be larger than the pull-up current of the PMOS transistors in theinverters. The SSASPL was implemented and simulated with a 0.18 CMOS process at .The minimum clock pulse width of the SSASPL to update the data is 62 ps.

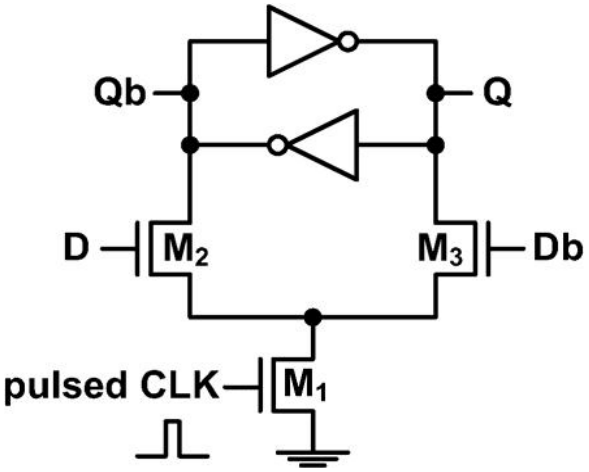


Figure 8. Schematic of the SSASPL

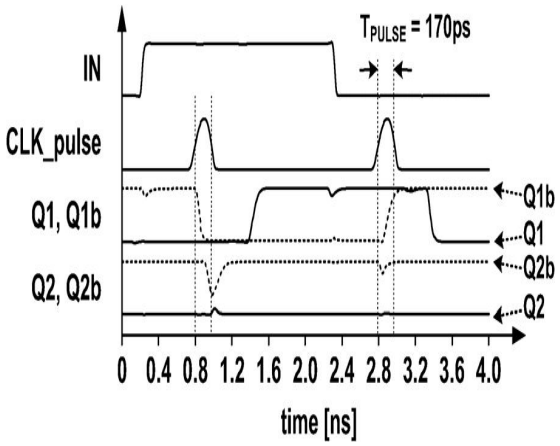


Figure 9. Waveforms of PPCFF

The rising and falling times of the clock pulse are approximately 100 ps. The clock pulse shape can be degraded due to the wire delay, signal coupling, supply noise. The clock pulse width of 170 ps was selected by adding the timing Simulation waveforms of a shift register with the SSASPLs driven by a pulsed clock signal.

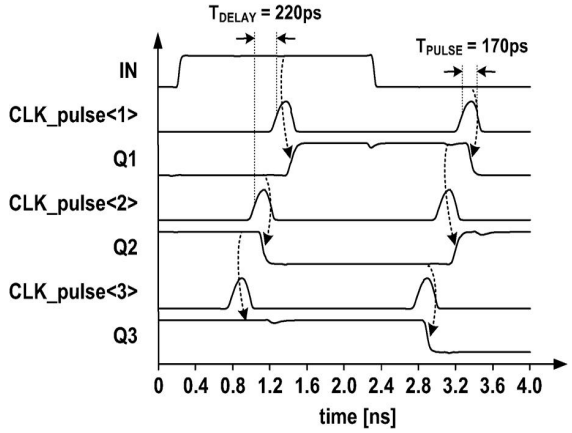
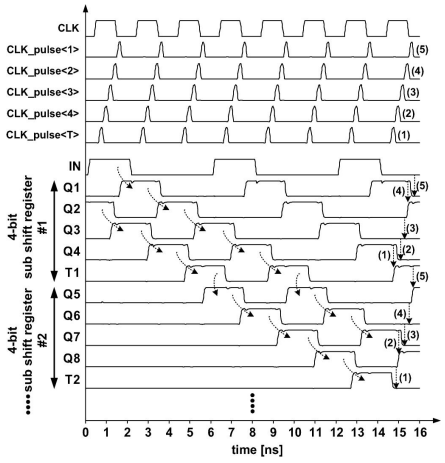
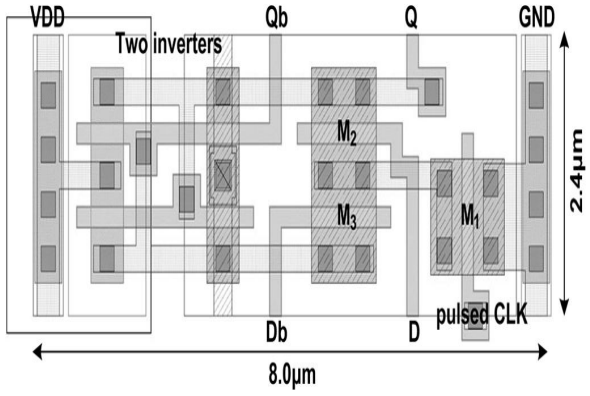


Figure 10. Simulation waveforms of a shift register with the SSASPLs driven by delayed pulsed clock signals

The output signals of the first latch (Q1 and Q1b) change correctly, because the input signal of the first latch (IN) is constant during the clock pulse width. On the other hand, the output signals of the second latch (Q2 and Q2b) do not change, because the input signals of the second latch, which are connected to the output signals of the second latch (Q2 and Q2b), change during the clock pulse width. The SSASPL flips the states of the cross-coupled inverters (Q and Qb) by pulling current down through either or during the clock pulse width. The clock pulse width is selected as the minimum time to flip the output signals of the latch (Q and Qb) when its input signals (D and Db) are constant. If the input signals change during the clock pulse width, the time pulling current down through either or becomes shorter than the clock pulse width, so that the latch has not enough clock pulse time to flip the output signals after the input signals change. Fig. 5.shows the simulation waveforms of a shift registerwith the SSASPLs driven by the delayed pulsed clock signals. This example has three shift registers (Q1–Q3) and three delayed pulsed clock signals (CLK_pulse□1:3□). The pulsed clock delay is 220 ps by adding the pulse interval of 50 ps between clock pulses to the clock pulse width of 170 ps. The sequence of the pulsed clock signals is in the opposite order of the latches. Each latch has a constant input during its clock pulse so there is no timing problem. Fig. 11 shows the simulated waveforms of the proposed 256-bit shift register with at the first 4-bit sub shifter register consisting of five latches (Q1–Q4 and T1) performs the shift operations correctly with five pulsed clock signals (CLK_pulse 1:4 and CLK_pulse T)(Q5–Q8 and T2) receives data from the latch T1 in the first sub shift register and performs the shift operations correctly mean the data transition sequence of the latches driven by the sequential pulsed clock signals.



(a)



(b)

Figure 11. (a) Layout of the SSASPL (b) Waveforms

III. RESULTS

Simulation Results

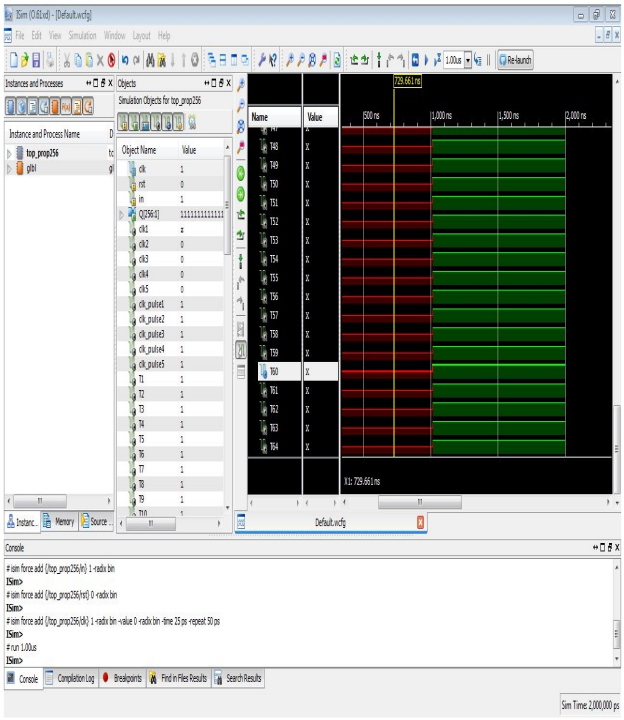


Figure 12. Technology Schematic

Synthesis Results

Final Results

RTL Top Level Output File Name : top_prop256.ngr
Top Level Output File Name : top_prop256
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : No

Design Statistics
IOs : 259

Cell Usage :

FlipFlops/Latches : 320
FDR : 320
Clock Buffers : 1
BUFGP : 1
IO Buffers : 258
IBUF : 2
OBUF : 256

RTL Schematic

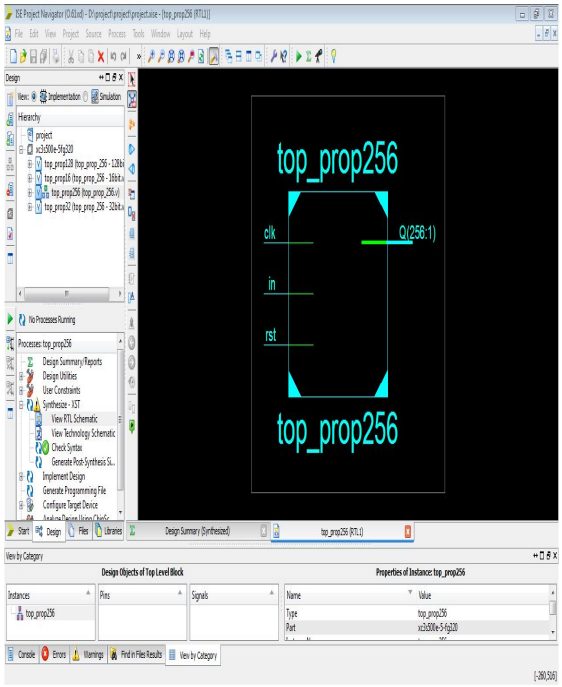


Figure 13.Technology Schematic

Technology Schematic

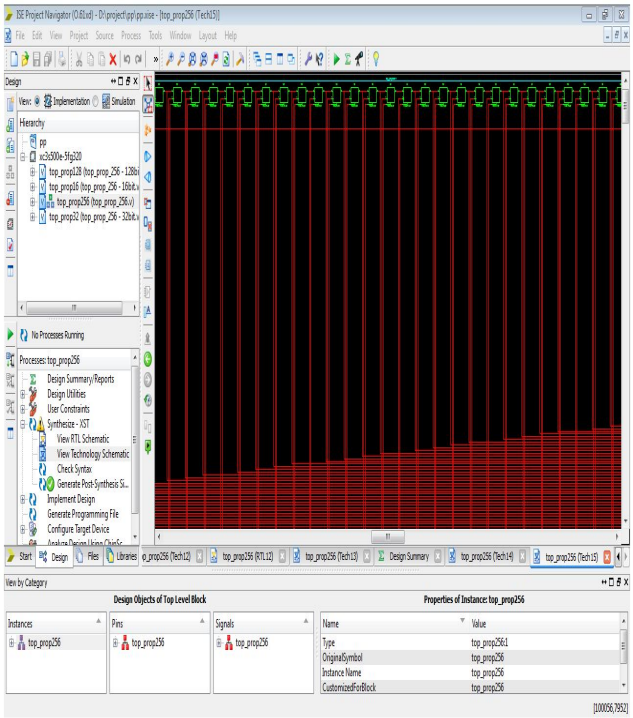


Figure 14. Technology Schematic

This technique proposes a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. A 256-bit shift register using pulsed latches

was fabricated using CMOS process. The proposed shift register saves area and power compared to the conventional shift register with flip-flops.

This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

IV. PERFORMANCE COMPARISON

Table I shows the transistor comparison of pulsed latches and flip-flops. The transmission gate pulsed latch (TGPL) , hybrid latch flip-flop (HLFF), conditional push-pull pulsed latch (CP3L) , Power-PC-style flip-flop (PPCFF) , Strong-ARM flip-flop (SAFF) , data mapping flip-flop (DMFF) , conditional precharge sense-amplifier flip-flop (CPSAFF) , conditional capture flip-flop (CCFF) , adaptive-coupling flip-flop (ACFF) are compared with the SSASPL used in the proposed shift-register. When counting the total number of transistors in pulsed latches and flip-flops, the transistors for generating the differential clock signals and pulsed clock signals are not included because they are shared in all latches and flip-flops. The SSASPL uses 7 transistors, which is the smallest number of transistors among the pulsed latches . The PPCFF uses 16 transistors, which is the smallest number of transistors among the flip-flops . Two 256-bit area-efficient shift registers using the SSASPL and PPCFF were implemented to show the effectiveness of the proposed shift register. Fig. 14 shows the schematic of the PPCFF, which is a typical master-slave flip-flop composed of two latches. The PPCFF consists of 16 transistors and has 8 transistors driven by clock signals. For a fair comparison, it uses the minimum size of transistors. The sizes of NMOS and PMOS transistors are and , respectively. Its layout was drawn compactly by sharing all possible sources and drains of transistors. All circuits were implemented with a 0.18 CMOS process.

The power savers measured and Table II shows the performance comparisons of the PPCFF and SSASPL. The SSASPL is 48.8% smaller and consumes 60.2% less power than the PPCFF. Table III shows the performance comparisons of the 256-bit shift registers. The conventional shift register using flip-flops was implemented with the PPCFFs. Two types of the proposed shift register using pulsed latches were implemented with the SSASPLs. The proposed shift register achieves a small area and low power.

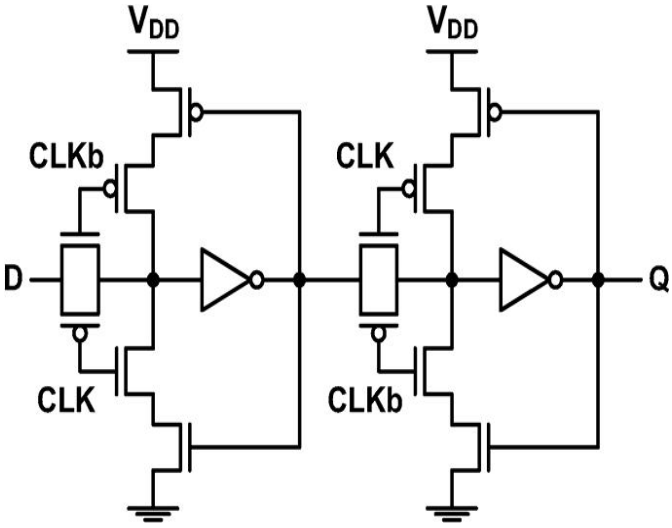


Figure 15. Schematic of the PPCFF

Table 1. Transistor comparison of pulsed latches and flip-flops

Type		Total number of transistors	Number of transistors connected to clock
Pulsed Latch	**SSASPL**	7	1
	TGPL	10	4
	HLFF	14	2
	CP3L	26	6
Flip-flop	**PPCFF**	16	8
	SAFF	18	3
	DMFF	22	5
	CPSA	28	5
	CCFF	28	5
	ACFF	22	4

Table 2. Performance comparisons of the PPCFF and SSASPL

		PPCFF	SSASPL
Type		Flip-flop	Pulsed Latch
Number of transistors	Total	16	7
	Clock	8	1
Area		37.5µm² (6.7 µm×5.6 µm)	19.2 µm² (8.0 µm×2.4 µm) (51.2%)
	Tota	8.29	3.30(39.8%)

Power[µW] @f_{clk}=100MHz	l		
	Data Path	3.87	2.57(66.5%)
	Clock load	4.42	0.73(16.5%)
Min.clock pulse width[ps]		-	62@TT 54-76@FF-SS
Clock pulse width(T_{PULSE})[ps]		-	170
Clock pulse interval[ps]		-	50
Pulsed clock delay(T_{DELAY})[ps]		-	220
Sizes of Transistors(W/L) [µm/µm]		NMOS=0.5/0.18 PMOS=1/0.18	M1-M3=1/0.18 NMOS=0.5/1.8 PMOS=1/0.18 In inverters

	Clock Buffer	818	192	173
	Clock-Pulse	-	248	446
Power[mw] @f_{CLK}=100 MHz	Total	2.123	1.194 (56.3 %)	1.199 (56.5 %)
	Data Path	0.991	0.824	0.741
	Clock Load	1.132	0.232	0.210
	Clock-Pulse	-	0.138	0.248
Max.Clock frequency		2.8 GHz	840MHz	483MHz

Table 3. Performance comparisons of shift registers

		Conventional shift register	**Proposed shift register**	
Type		**PPCFF** (Flip-flop)	**SSASPL** (Pulsed Latch)	
Word Length of shift registers(N)		256		
Word Length of sub shift registers(k)		-	4	8
Total number of Flip-flops or pulsed latches		256	320	288
Area[μm^2]	Total	10,418	6,583	6,148
	Flip-flop or pulsed latch	9,600	6,144	5,530

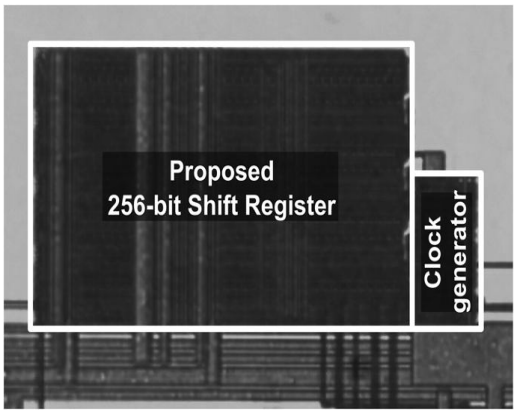


Figure 16. Chip microphotograph

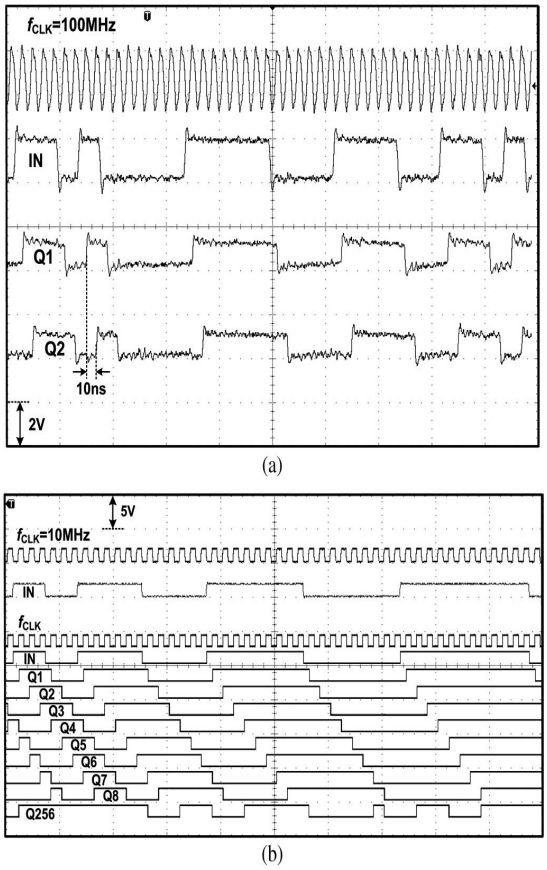


Figure 17. Measured waveforms of the proposed shift-register at (a)fclk=100 MHz (b) fclk=10 MHz

V. CONCLUSION& FUTURESCOPE

This proposed shift register design reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register was fabricated using a 0.18 micro m CMOS process with vdd=1.8 v. Its core area is 6600 micro m2 . It consumes 1.2 mW at a 100 MHz clock frequency. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flip-flops.

For the future analysis, the implementation of further more bits with still efficient shift register can be designed. Here the efficient shift register with pulsed latches can be designed. The future scope for this project is designed such as the speed of the circuit is half of its speed, and the area is half of the proposed system area and the power consumption is also less compared proposed system. For that we are using trigger generator in place of clock pulse generator. Hence the performance of the circuits also more efficient.

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