Design of 6T SRAM Cell And Result Analysis

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Abstract- *Static Random Access memory (SRAM) is a matrix of static volatile memory cell. SRAM has become a major component in many VLSI chips due to their large storage density and small access time. SRAM has become topic of substantial research due to the rapid development for low power, low voltage memory design during recent years due to increase demand for notebooks, laptops, IC memory card and hand held communication devices. SRAMs are widely used for mobile applications as both on chip and off-chip memories, because of their ease of use and low standby leakage.*

Keywords- 6T SRAM cell, Power dissipation, Read delay, Write delay.

I. INTRODUCTION

SRAM or Static random access memory is a form of semiconductor memory widely used in electronics, microprocessor and general computer applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion and does not need to be dynamically updated as in the case of DRAM memory. While the data in the SRAM memory does not need to be refreshed dynamically, it is still volatile meaning that when the power is removed from the memory device, the data is not held and will disappear.

There are two key features of SRAM memory:

1. The data is held statically: This means that the data is held in semiconductor memory without the need to be refreshed as long as power is applied to the memory.
2. SRAM is a form of random access memory: A random access memory is one in which the locations in the semiconductor memory can be written to or read from in any order, regardless of the last memory location that was accessed.

The circuit for an individual SRAM memory cell comprises typically four transistors configured as two cross coupled inverters. This circuit has two stable states and these equate to the logical "0" and "1" states. In addition to the four transistors in the basic memory cell, additional two transistors are required to control the access to the memory cell during the read and write operations. This makes a total of six transistors, making what is termed a 6T memory cell. 6T static random access memory is a type of semiconductor memory that uses bistable latching circuitry to store each bit SRAM memory basics

II. OVERVIEW OF CMOS INVERTER

The gate of an MOS transistor controls the flow of current between the source and drain. When the gate of an NMOS transistor is 1, the transistor is ON and there is a conducting path from source to drain. A PMOS transistor is just the opposite, being ON when the gate is low and OFF when the gate is high.The bar at the top indicates VDD and the triangle at the bottom indicates GND. The output Y is pulled up to 1 because it is connected to VDD but not to GND [2].

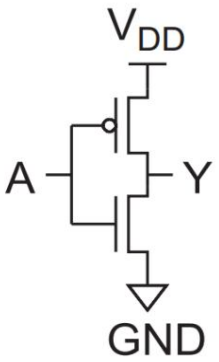

Fig.1. Basic ST inverter [1]

III. 6T SRAM CELL OPERATION

1. 6T sram cell operation

The standard cell comprises six transistors, as shown in fig.3.The nMOS access transistors (A1 and A2) located at the ends of circuit and a pair of cross-coupled inverters constitute memory cell. The nMOS elements (D1 and D2) of the latch are the driver transistors, while pMOS (P1 and P2) are the pull-up transistors. The access transistors operate when the word line is raised, for read or write operation, connecting the cell to the bit lines (Bit line, ~Bit line). The cell has three different operation modes. In the standby state, word line is not asserted, so access transistors are turned off. Therefore, cell cannot be accessed and two cross-coupled inverters continue to feedback each other as long as they are connected to the supply, data will hold in the latch. The read operation

starts by pre-charging the bit lines high then allowing them to float. Then word line is asserted turning on all access transistors. The data stored in the nodes are driven onto bit lines. A voltage difference is developed between bit lines and a sense amplifier detects the value of the cell.

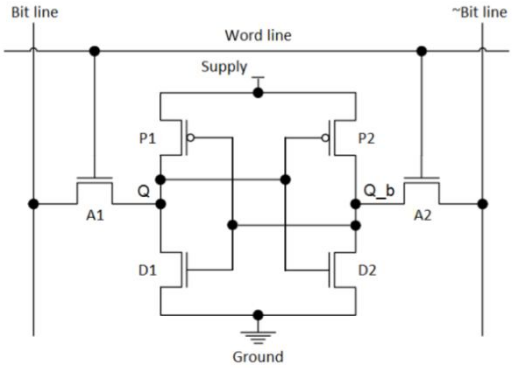

Fig.2. 6T SRAM cell

During the write operation the bit lines are driven to complementary voltage level sand then word line is raised. The data to be written into the cell are driven onto the bit lines and one of the storage nodes is discharged through the access transistor [2]. 6T SRAM cell suffers from read-current disturbance-induced SNM degradation with Vdd scaling. Also, the read stability and the write stability of 6T SRAM cell degrade to unacceptable level at low supply voltages due to process variations [1].

IV. PERFORMANCE PARAMETERS

Write delay: It is the delay between the applications of the word line WL signal and the time at which the data is actually written.

Read delay: Read delay is the delay involved in allowing the bit lines to discharge by about 10% of the peak value or the delay between the application of the WL signal and the response time of the sense amplifier.

Supply Voltage: Variations in switching activity and diversity in the type of logic result in uneven power dissipation across the die. This variation results in uneven supply voltage distribution and temperature hot spots, causing transistor sub-threshold leakage variation. The supply voltage (Vcc) will continue to scale modestly by 15% not by the historic 30% per generation, due to

1) Difficulties in scaling threshold voltage (Vth)
2) To meet the transistor performance goals. Maximum Vcc is specified as a process reliability limit and minimum Vcc is required for the target performance.

Temperature: Within-die temperature fluctuations have existed as a major performance and packaging challenge for many years. Both the device and interconnect performance have temperature dependence, with higher temperature causing performance degradation. Additionally, temperature variation across communicating blocks on the same chip may cause performance mismatches, which may lead to logic or functional failures [4]. The delay and the power suffer from an increase in the circuit temperature mainly due to the adverse impact of temperature on the drain current and interconnect resistance. Temperature also affects certain variables such as the mobility and Threshold voltage which determine Id drain current, Idsat drain current insaturation and Req equivalent resistance of the transistors [5].

V. RESULTS AND ANALYSIS

Write mode

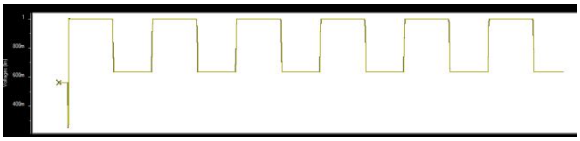

Fig.3. V(1) : Write one program

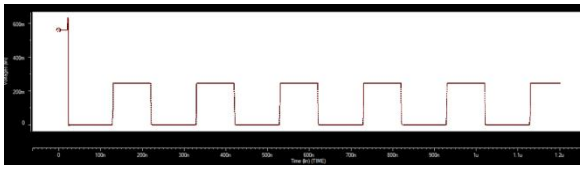

Fig.4. V(2) : Write one program

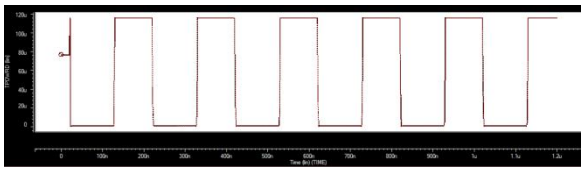

Fig.5. Power

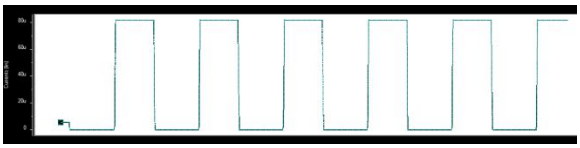

Fig.6. i(Vbl)

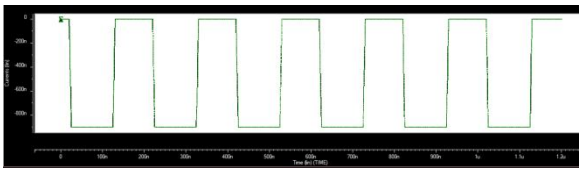

Fig.7. i(Vwl)

Power Dissipation	76.72u
Total Power	5.34E-05
Tpdrise	1.24E-12
Tpdfall	2.45E-09
Tpd	1.23E-09
Tpdwrite	1.24E-12

Read mode

Fig.8.V(1)

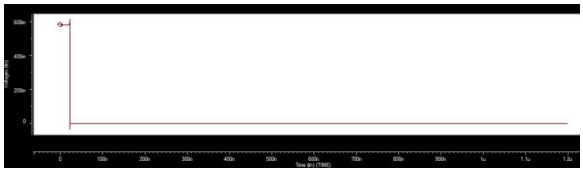

Fig.9.V(2)

Fig.10.VBL

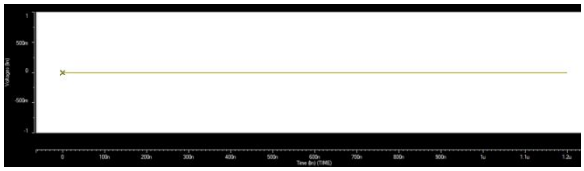

Fig.11.VBLB

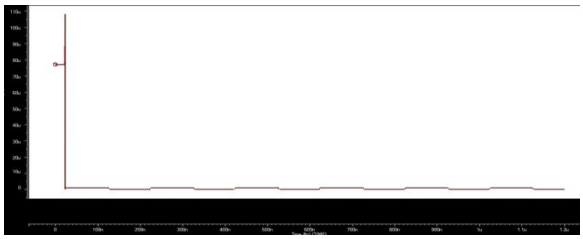

Fig.12. Power

Power Dissipation	76.9943u
Total Power	2.04E-06
Tpdrise	1.29E-12
Tpdfall	9.00E-10
Tpd	4.51E-10
Tpdread	1.29E-12

Standby mode

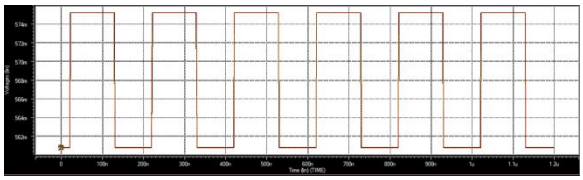

Fig.13. V(1) & v(2)

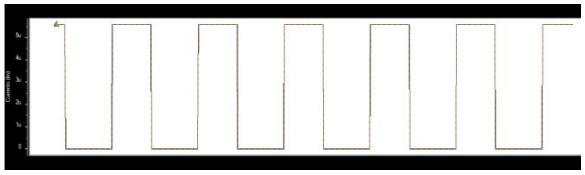

Fig.14. VBL

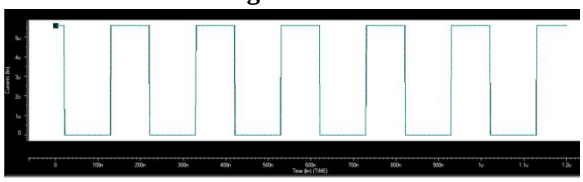

Fig.15. VBLB

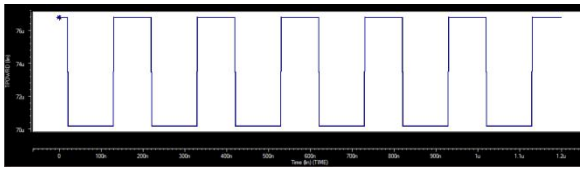

Fig.16. Power

VI. CONCLUSION

Simulation results for rise time, fall time, read access delay, write access delay, power and total power dissipation has been carried out successfully in 32nm Technology.

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