Design and Implementation of Thermal Aware Multichannel UART Using Verilog HDL

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Abstract- *UART is the serial communication protocol that send and receive data with stop and start signal such as USB exchanging data with PC. For proper communication between them, baud rate is set such as 4800,9600 and so on. Transmitter can send one byte at a time to the sender and it can communicate with one sender only.*

There many application that contain many slave and one master such as PC has to send multiple data to various equipment but when one slave is getting attention from the transmitter , other equipment has to wait for transmitter to get free. After completing communication with first equipment, transmitter start communication with second equipment while other equipment will wait for their chance. In this way, transmitter take long time to send multiple data to all the equipment.

So to solve this problem, concept of multichannel UART have been introduced. Transmitter can send multiple data to multiple receiver at a time by setting different baud rate.

Rather than designing UART, there is another motive of this thesis i.e. green communication. The main contribution to the green communication is energy efficiency, thermal awareness and power analysis. These points are needed to be obtained to design UART for green computing and network communication.

So, Xilinx 14.5 software is used to simulate and synthesize Verilog hdl language and this language is used to design UART. SPARTAN 6 45nm technology FPGA kit is used to test UART design since it low power consuming, submicron based FPGA. This design is taking less time to run i.e. 3.9 ns. In context of green communication, leakage power is 0.028W at 16GHz and 0.012W at 1GHz. So the power consumption is 0.433 W for 500 LFM ,0.420W for 250 LFM at 16GHz and 0.019W for 250 & 500 LFM at 1GHz. This results indicate that its good candidate for green computing and network communication in context of the previous work .

Keywords-FPGA,UART,Xilinx,Verilog,Green Communication.

I. INTRODUCTION

In some complex systems, communications between the master controller and slaver controllers are implemented by serial or parallel port. Parallel communication needs a lot ofmulti-bit address bus and data bus and it is only convenient for short distance transmission. Serial communication is another way of communication used extensively because of its simple structure and long transmission distance. But sometimes a common serial port could not meet requirements of complex systems with different Baud Rates equipments even some special Baud Rate equipments. As showing in figure 1, in a system, the PC's Baud Rate is 115200bps and the Ep1 i.e. equipment 1's

Baud Rate is 57600bps, equipment 2's Baud Rate is 19200bps, and other equipments are set at 9600bps or other Baud Rates. It is impossible to implement this multi-Baud Rate communication system without a special Baud Rate converter.

Now-a-days, Micro controllers and digital signal processors (DSPs), in complex control algorithms can be easily implemented to attain the desired system performance. But in proposed control systems, it is difficult to attain the exact result for various factors such as which affect the control of the system, it means control algorithms are capable of controlling and implementing equipment and states of control circumstance. Except those factors, communication parameters of control systems include Bit Error Rate, Baud Rate and synchronization between sub-systems also causing great effect. In order to improve precision of control system and make better use of modern control algorithms, we should pay much more attention on communication methods in control systems[12].

In a 6-DOF robot, there are 6 sub-controllers which are all the same structure to be designed. The PC is used to implement the control algorithm of the robot and send control parameters to sub-controllers and sub-controllers are used to collect feedback signals and send them to the PC. The PC and sub-controllers communicate with each other on a RS485 BUS NET. Each sub-controller has a unique address number and the PC uses this number to identify each sub-controller. When the PC wants to send data to node 6, it has to access front 5 nodes, this engenders time delay and makes performance of the robot's each DOF not synchronization. So it reduces the control algorithm's

precision and brings difficulties in researching of the control algorithm.

To solve these problems described as above, we design a multi-channel UART controller based FPGAs. It can receive data with a UART block at a certain Baud Rate and transmit data to sub-equipment with a UART block at the same Baud Rate or at other kind of Baud Rate which is different from the receiving Baud Rate. And it also can be used to reduce time delay between subcontrollers. Xilinx 14.5 software is used to design UART using Verilog language and implemented on SPARTAN 6 45nm FPGA kit.

II. LITERATURE REVIEW

Mohammed Azeemuddin[1] designed UART using Verilog which consumes less power of 2 mW. This UART communicate at 115200 baud rate. They showed that 89% power consumption is reduced as compare to the presented previous works.

Iti Aggarwal, Shweta Gaba[2] shown the UART implementation on Virtex 4 and Spartan 3 FPGA kit. The frequency obtained for reception and transmission of 8-bit on Virtex 4 is 284 MHz and on Spartan 3 is 147 MHz. Finally they concluded that Virtex 4 kit is better device family to implement UART because it consumes less number of resources of this FPGA.

Umakanta Nanda, Sushant Kumar Pattnaik[3] implement UART on Virtex II because of low cost,reprogram ability and high speed. Verilog programming was done on Xilinx ISE 8.2 software.They use shift register,data register,control register and status register.

Ashwini D. Dhanadravye , Samrat S. Thorat[4] surveyed on various architecture's of UART such as Mutlti channel UART,UART embedded with BIST technique,Auto tuning baud rate and asynchronous FIFO,AES implementation with UART module and 9-bit UART module. All the architecture designed using VHDL.

Ms.Neha R. Laddha,Prof.A.P.Thakare[5] perform transmission and reception operation of data on Altera DE1 board and UART had been designed using Quartus and Modelsim software. This UART uses the multi baud rate so that it can be communicate at different baud rate.

C.K.Hemantha Lakshmi, C.K.Hemantha Rama and C.K.Mahesh Babu[6] designed multi channel UART with asynchronous FIFO which meet the complex control system communication demand. With the help of this, UART can send number of data.

HU Zhe, ZHANG Jun, LUO Xi-ling[7] presented noval architecture of multi channel UART which contains interrupt controller design. Several data can be send at a time in no time.All the results are compared with PowerPC 860 and ST 16C554.

G. Sowmya Bala, A.Rama Krishna[8] perform master serial communication at different baud rate with different slave which solve the problem of sending less data. Xilinx Spartan 3E FPGA is used for hardware implementation.

Tloy Scoft[9] has done power analysis functional and timing verification. He mention the number factor which helps to reduce power such as reducing operating voltage,using optimum operating frequency,use optimum encoding,reduce voltage swing of I/O's. He also focused on the environment model of FPGA device include heat sink,airflow,ambient temperature,PC board layer.

Randive Poonam Umakant, Pimpodkar Shweta Dattatray, Gupta Sonali Jeetlal,Prof. Rakibe Rupali S.[10] perform UART communication with laptop and program have been written on Xilinx 14.5 ISE design suite using Verilog. They have shown communication at 4800 and 9600 baud rate.

Shouqian Yu, Lili Yi, Weihai Chen, Zhaojin Wen[11] design UART controller whose baud can reconfigurable with help of which time delay is reduced between sub-controllers complex system to improve the synchronization of sub-controllers. The program is written using Verilog language and tested on ALTERA FPGA kit.

Sunny Singh, Abhishek Jain, Amanpreet Kaur, Bishwajeet Pandey[14] focused on green computing and network communication. They proved on the basis of varying airflow ,temperature variation and linear feet per minute(LFM). One parameter is fixed , one is varied and on the basis of these two, third is obtained. They obtained these results by design Verilog based UART on Virtex 6 FPGA.

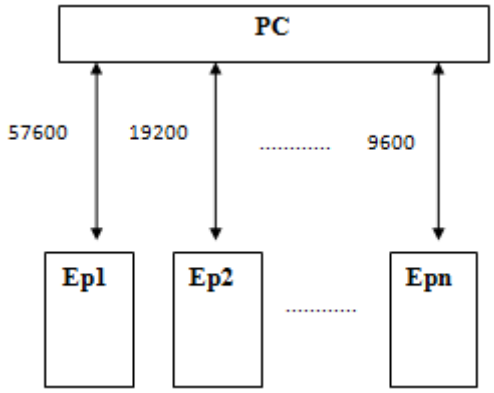

Fig.1 Multi-equipments communication diagram

III. THEORY

In the multi-channel controller, there are different blocks including UART block, Status Detectors, asynchronous FIFOs block and Baud Rate Generator block. Each block has different function in the controller.

The first part is UART circuit block and its structure is shown in figure 2. It consists of three parts Receive Circuit,Transmit Circuit and Control/Status Registers. The Transmit Circuit consists of a Transmit Buffer and a Shift Register. Transmit Buffer loads data being transmitted from local CPU. And Shift Register accepts data from the Transmit Buffer and send it to the TXD pin one by one bit. The Receive Circuit consists of a Receive Shift Register and a Receive Buffer. The Receive Shift Register receives data from RXD one by one bit. The Receive Buffer loads data from long-distance MCU and gets it ready for the local PC to read. The Control Register a special function register is used to control the UART and indicate status of it. According to each bit's value the UART will choose different kind of communication method and the UART knows what to do to receive or transmit data. FIFOs are used to store data received from the PC and get ready for sub MCUs. When writing data into FIFOs and reading data out of FIFOs we could set different clock domains according to the PC's and MCUs' Baud Rate. So it can be used to implement communications between MCUs at different Baud Rate .

The controller also has a block of Baud Rate Generator to engender different Baud Rates to content requirements for different kind of systems. This block is constituted by timers (32/16 bits timers), frequency dividers and a Baud Rate setting register.

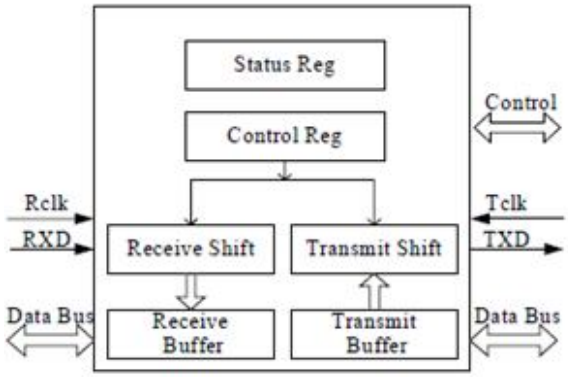

Fig.2.Structure of UART block

Structure of the controller is showing in figure 3. The structure consist of PC, COM port ,buses,four UART and baud rate generator. Verification and testing of multichannel UART is done by sending data to the PC with the help of COM port. Before communication start, different baud rate are set for communication with different UART. Transferring of data is done through databus.

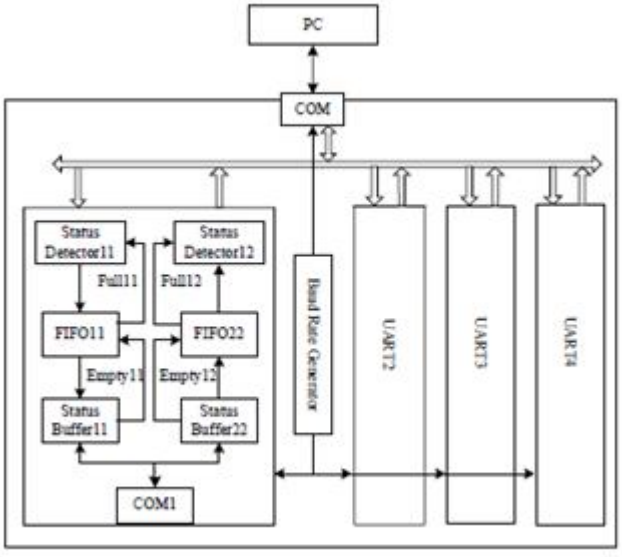

Fig.3 Structure of the controller

The following terminology are for power estimation:

Quiescent Current

The current drawn by a blank configured device with no output current loads, no active

input pull-up resistors, and all I/O pins 3-state and floating.

Device Static Power

The power from transistor leakage on all connected voltage rails and the circuits required for the FPGA to operate normally, post configuration. Device static power is a function of process,

voltage and temperature. This represents the steady state, intrinsic leakage in the device.

Design Power

The power of the user design, due to the input data pattern and the design internal activity.This power is instantaneous and varies at each clock cycle. It depends on voltage levels and logic and routing resources used. This also includes static current from I/O terminations,clock managers, and other circuits which need power when used. It does not include power supplied to off-chip devices.

Ambient Temp (°C)

Specify the maximum possible temperature expected inside the enclosure that will house the FPGA design. This, along with airflow and other thermal dissipation paths (for example, the heatsink), will allow an accurate calculation of Junction Temperature which in turn will allow a more accurate calculation of device static power.

Airflow (LFM)

The airflow across the chip is measured in Linear Feet per Minute (LFM).LFM can be calculated from the fan output in CFM (Cubic Feet per Minute) divided by the cross sectional area through which the air passes. Specific placement of the FPGA and/or fan may have an effect on the effective air movement across the FPGA and thus the thermal dissipation. Note that the default for this parameter is 250 LFM. If you plan to operate the FPGA without active air flow (still air operation) then the 250 LFM default has to be changed to 0 LFM.

IV. ALGORITHM

4.1 Transmitter

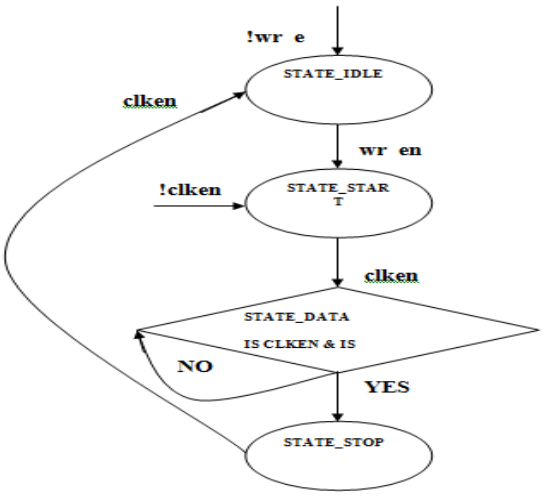

Fig.4.1 Flow chart of transmitter

This transmitter(figure 4.1) consist of four state's:STATE_IDLE,STATE_START,STATE_DATA and STATE_STOP. When wr_en is low and tx signal is high that indicates transmitter is not ready to send the data and transmitter is in STATE_IDLE state. In this state, input data,din, enters into data register and bitpos is zero. When wr_en is high, then transmitter enters in the STATE_START state. This state check clken signal. If it is high, then tx goes into low that indicate transmitter is ready to send the data and transmitter enter into the next state,STATE_DATA. This state perform the transfer operation of data serially. This state continuously check bitpos. If bitpos is equals to 7,then STATE_IDLE state. Except in the STATE_IDLE, transmitter enter into next state,STATE_STOP. If bitpos is less than 7, transmitter remain in the same state. In this last state, clken signal again check and tx goes high which indicate's transfer process has been done. If clken is high, then transmitter goes back to thetx_busy signal is low.

4.2 Receiver

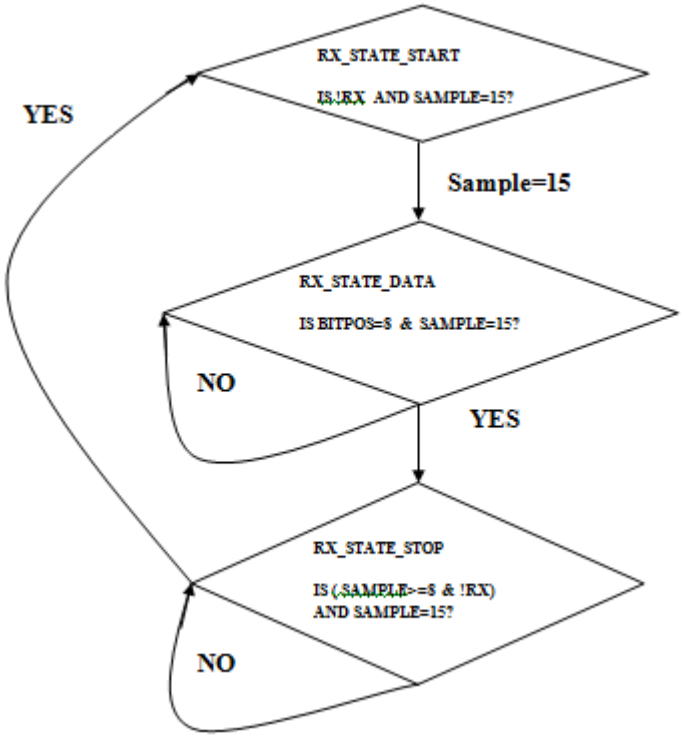

Fig.4.2 flow chart of receiver

This receiver consist of three states:RX_STATE_START,RX_STATE_DATA and RX_STATE_STOP. Initially rdy signal is zero when rdy_clr signal is high. When clken is high, then receiver enters in the RX_STATE_START. In this state, two condition are checked: first if rx is low or sample is not equal to zero and second if sample is equals to fifteen. First condition is start incrementing sample by one and second condition is initialising

bitpos,scratch,sample signals to zero and move to next state,RX_STATE_DATA. This state again checking two conditions: if sample equals to eight and if sample equals to fifteen and bitpos is equals to eight. First condition is incrementing bitpos by one and moving rx into first three bit of scratch. Second condition is moving into next state,RX_STATE_STOP. This state is checking if sample is greater than eight and rx is not high or sample is equal to fifteen, then scratch is move to the data,sample is zero and rdy signal is high. If condition is not satisfy, then sample will increment itself by one. Finally move receiver to the RX_STATE_START state.

V. SYNTHESIS & HARDWARE TESTING

Synthesis and simulation has been done on Xilinx 14.5. Initially baud rate of UART set to 9600 so that it can communicate with the PC. Verilog code is burn on 45nm SPARTAN 6 kit. Figure 5.1 showing testing of UART using Verilog. Initially clk,data,enable and rdy_clr signals are kept zero. Then clk and enable starts toggling. On positive edge of rdy signal, rdy_clr also start toggling. In simultaneously to this, if rxdata is not equal to data which was set initially, then transmitter continuously sending data and increments data as well. If rxdata is equals to 256, then transmitter stop sending data. Loopback is the signal through which transmitter send data and receiver receives.

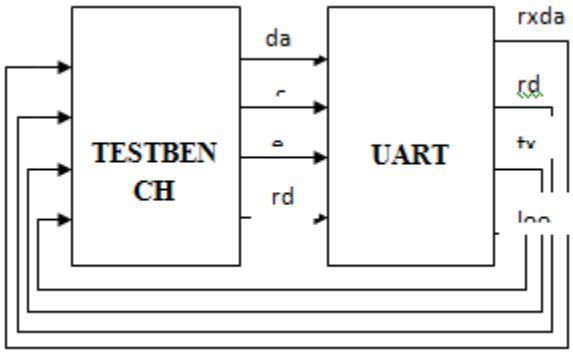

Fig.5.1testbench of UART

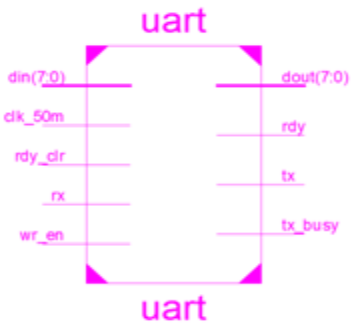

Fig.5.2 RTL schematic of UART

After synthesis of UART design, register transfer level(RTL) view have been obtained(figure 5.2). It consists of din[7:0],clk_50m,rdy_clr,rx and wr-en inputs and dout[7:0],rdy,tx and tx_busy outputs. Figure 5.3 shows the starting procedure of UART. Rxdata is the receiving input and data is the transmitter data. Txclk_en is the signal which signify the baudrate for transmitter and rxclk_en signify the receiver's baudrate. During this time, tx_busy signal is high indicating transmitter is busy in transmission of data. Both communicate at 9600 baudrate indicating by two vertical cursor: one in orange and one in blue. In this case,Loopback signal is the signal through which receiver and transmitter is communicating. Figure 5.4 showing the completion of UART process i.e. transmission and reception os data have been done. Whole data send by transmitter is received by receiver. Transmitter signal tx_busy signal is low indicating transmitter is ready to send more data.

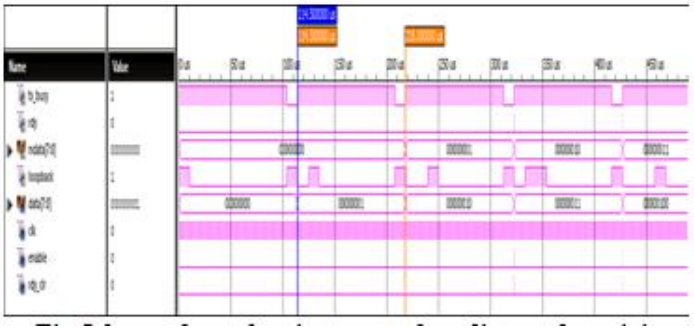

Fig.5.3 waveform showing start of sending and receiving of data

VI. RESULTS

6.1 Power Analysis

Following are results and analysis for green communication:

A. When Ambient Temperature is 15 ˚C

From table1, it can be observe that as soon as we scale down the frequency from 16 GHz to 1 Ghz, the reduction in clock power is 93.7%, in IOS is 94.44 %, in leakage is 20 %, in junction temperature is 43.5% and in total power is 90.7%.

From table2, it can be observe that as soon as we scale down the frequency from 16 GHz to 1 Ghz, the reduction in clock power is 93.7%, in IOS is 94.44 %, in leakage is 14.2 %, in junction temperature is 42.55% and in total power is 90.7%.

Fig.5.4 waveform showing transmission and reception of data have been done

Table 1: When Airflow is 250 Linear Feet per Minute

Frequency	Clock	IOS	Leakage	Junction Temperature(JT)	Total
1 GHz	0.019	0.002	0.012	16.3	0.039
6 GHz	0.114	0.013	0.013	20.6	0.170
11 GHz	0.209	0.025	0.014	24.8	0.296
16 GHz	0.303	0.036	0.015	28.9	0.420

Table 2: When Airflow is 500 Linear Feet per Minute

Frequency	Clock	IOS	Leakage	Junction Temperature(JT)	Total
1 GHz	0.019	0.002	0.012	16.2	0.039
6 GHz	0.114	0.013	0.012	20.4	0.170
11 GHz	0.209	0.025	0.013	24.2	0.296
16 GHz	0.303	0.036	0.014	28.2	0.420

B. When Ambient Temperature is 30 ˚C

Table 3: When Airflow is 250 Linear Feet per Minute

Frequency	Clock	IOS	Leakage	Junction Temperature(JT)	Total
1 GHz	0.019	0.002	0.015	31.4	0.043
6 GHz	0.114	0.013	0.017	35.8	0.174
11 GHz	0.209	0.025	0.018	39.9	0.300
16 GHz	0.303	0.036	0.020	44.1	0.425

From table3, it can be observe that as soon as we scale down the frequency from 16 GHz to 1 Ghz, the reduction in clock power is 93.7%, in IOS is 94.44 %, in leakage is 25 %, in junction temperature is 28.8% and in total power is 89.9%.

Table 4: When Airflow is 500 Linear Feet per Minute

Frequency	Clock	IOS	Leakage	Junction Temperature(JT)	Total
1 GHz	0.019	0.002	0.015	31.4	0.043
6 GHz	0.114	0.013	0.017	35.5	0.174
11 GHz	0.209	0.025	0.018	39.5	0.300
16 GHz	0.303	0.036	0.019	43.4	0.425

From table4, it can be observe that as soon as we scale down the frequency from 16 GHz to 1 Ghz, the reduction in clock power is 93.7%, in IOS is 94.44 %, in leakage is 21 %, in junction temperature is 27.6% and in total power is 89.9%.

C. When Ambient Temperature is 45 ˚C

Table 5: When Airflow is 250 Linear Feet per Minute

Frequency	Clock	IOS	Leakage	Junction Temperature(JT)	Total
1 GHz	0.019	0.002	0.021	46.6	0.049
6 GHz	0.114	0.013	0.023	51	0.181
11 GHz	0.209	0.025	0.025	55.2	0.307
16 GHz	0.303	0.036	0.028	59.3	0.433

From table5, it can be observe that as soon as we scale down the frequency from 16 GHz to 1 Ghz, the reduction in clock power is 93.7%, in IOS is 94.44 %, in leakage is 25 %, in junction temperature is 21.4% and in total power is 88.6%.

From table6, it can be observe that as soon as we scale down the frequency from 16 GHz to 1 Ghz, the reduction in clock power is 93.7%, in IOS is 94.44 %, in leakage is 25 %, in junction temperature is 20.6% and in total power is 88.6%.

6.2 Timing Summary

Speed Grade: -3
Minimum period: 3.889ns (Maximum Frequency: 257.142MHz)
Minimum input arrival time before clock: 4.058ns
Maximum output required time after clock: 4.932ns

Table 6: When Airflow is 500 Linear Feet per Minute

Frequency	Clock	IOS	Leakage	Junction Temperature(JT)	Total
1 GHz	0.019	0.002	0.021	46.5	0.049
6 GHz	0.114	0.013	0.023	50.7	0.180
11 GHz	0.209	0.025	0.025	54.7	0.307
16 GHz	0.303	0.036	0.027	58.6	0.433

6.3 Device Summary

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	66	54576	0%
Number of Slice LUTs	153	27288	0%
Number of fully used LUT-FF pairs	60	159	37%
Number of bonded IOBs	23	316	7%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

The implementation of the UART was completed. All of the pieces for the UART have been written and simulated. Testing of UART(figure 6.1) is shown below.

VII. CONCLUSION

UART design is tested and verified using 45nm SPARTAN 6 FPGA kit and Verilog HDL language. This design solves the complex systems where sub controllers have to wait for the main system to get free and send them another eight bit of data. This design also solves the problem of synchronization with sub-controllers. It is reconfigurable i.e. baud rate can be change. This design is fast as it require only 3.9ns to run. In context of green communication, leakage power is 0.028W at 16GHz and 0.012W at 1GHz. So the power consumption is 0.433 W for 500 LFM ,0.420W for 250 LFM at 16GHz and 0.019W for 250 & 500 LFM at 1GHz. This results indicate that its good candidate for green computing and network communication in context of the previous work. This design requires zero number of register and LUT of FPGA .

Fig.6.1 implementation of UART

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