Modeling and Analysis of Sinusoidal PWM Technique for CHB Multilevel Inverter for Photovoltaic System

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Abstract-*This paper presents the simulation and analysis of sinusoidal PWM technique for CHB multilevel inverter for photovoltaic system. The ultimate aim of the paper is, the gate pulses generated by Sinusoidal Pulse Width Modulation (SPWM) technique with a Fuzzy logic controller. A buck-boost converter is used to maintain the constant PV voltage level integrated by an MPPT technique followed by Perturb and Observer algorithm is also implemented. The MPPT is used to harness the maximum power of solar radiations under its various climatic conditions. The lower number of semiconductor switches leads to minimizing overall di/dt ratings and voltage stress on each switches and switching losses The effectiveness of the proposed system is proved with the help of simulation. The simulation is performed in MATLAB/Simulink. From the simulation results, it shows that the proposed multilevel inverter works properly to generate the multilevel output waveform with minimum number of semiconductor devices and to achieve high dynamic performance with low THD with transient conditions and also balance the capacitor voltages.*

Keywords: Photovoltaic system, Cascaded H-Bridge Multilevel Inverter, Sinusoidal Pulse Width Modulation (SPWM), MPPT Technique

I. INTRODUCTION

Today, the energy demand is moving on increasing toward generating power with renewable energy source that may be dispersed in a wide area, and most of them are renewable, as they have greater advantages due to their environmentally friendly nature. Photovoltaic (PV) energy has augmented interest in wide range of electrical power applications, since it is considered as a basically limitless and generally on hand energy resource with the focus on greener sources of power particularly for distant locations where utility power is engaged [1-4]. The solar can be used by all in universe which doesn't need more investigations of producing electricity [5-7]. This leads to research in multilevel inverters.

The fast increasing use of power-electronics equipment in recent years has increased the number of nonlinear loads that draw harmonic currents from the power system [8]. The undesired current components cause stress to the power system, generating disturbed fundamental and harmonic voltage drops in the network impedances. They may add additional losses and even excite resonances [9-14]. The active power filter is a common approach to eliminate the undesired current components by injecting equal but opposite harmonic currents [15-18]. Active filtering can be based on various control strategies for obtaining the compensator current reference values, working either in the frequency domain or in the time domain.

Multilevel inverters [19-22] are becoming an established means for developing new high-power applications that require substantial increase of both current and voltage magnitudes. The advantages of multilevel inverters have been well known since the first NPC inverter was proposed in [23-25]. This particular topology increases the power rating because the blocking voltage of each switch is one-half of the dc-bus voltage. Moreover, their output-voltage harmonic content is much smaller than that of two-level inverters with the same switching frequency owing to the output-voltage waveform improvements [26].

The multilevel inverters are classified into three types namely: (i) Diode clamped multilevel inverters; (ii) Flying capacitor multilevel inverter; and (iii) Cascaded H bridge multilevel inverter. Of these the cascaded H bridge multilevel inverter topologies give better results. The research goes on increasing to propose a new structure of inverter with reduced semiconductor devices with increased multilevel at the output waveform [27-33]. The study of the multi sampled multilevel inverters and their control techniques to improve the performance of the multilevel inverters. This also deals with the different control techniques to be implemented in multilevel inverters in order to reduce the total harmonic distortion (THD). But they don't concentrate on the structure of the multilevel inverters [34-38].

A way to balance the capacitor voltage to produce voltage levels of equal width. Therefore the THD is reduced. There is no change in the structure of the inverter. Only the technique has been implemented with conventional structure but they achieved better THD [39-45]. The new algorithm for producing the switching signals. Here new optimization algorithm to produce the modulation signals; the algorithm works better than the other techniques but the structure of cascaded multilevel inverter remains same. Hence the switching loss is more and the number of switches used is same as that of the conventional one. Therefore it is necessary to find the new structural way of producing multilevel with reduced semiconductor devices [46-52].

The cascaded H bridge topology to be used, to reduce THD and the multilevel inverter fed multiphase induction motor; here they use diode clamped inverter to produce multiple levels at the output and they are used to drive the five phase motor. The performance analysis is done using this. Since they use diode clamped multilevel inverter the number of semiconductor devices is high and hence the losses are heavy. On replacing it with a new structure and by increasing the number of levels can improve the performance of the system [53-63]. The closed loop control strategy implemented in multilevel inverter is explained and the control circuit is also big which again increases the circuit complexity thus reducing the effectiveness of the proposed system [64-68]. In this paper, a proposed model of single-phase asymmetrical cascaded H-bridge multilevel inverter for a PV system is implemented with an MPPT array and a fuzzy logic controller.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

A cascaded multilevel inverter is broadly considered for the PV power conversion system. A general structure of an H-bridge module with a separate dc source is shown in Fig 1.

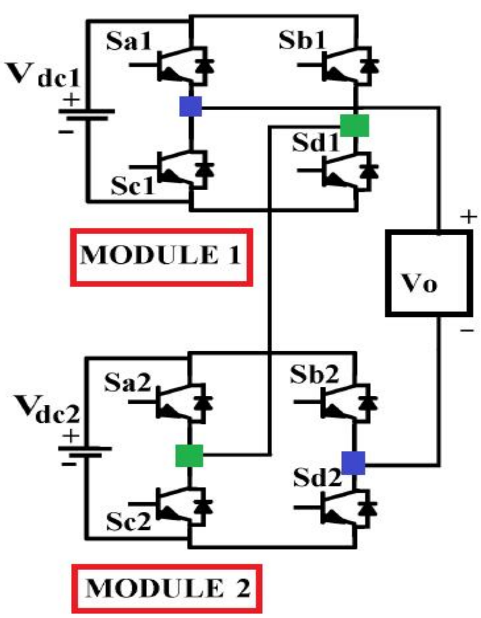

Fig 1. Circuit diagram of H-bridge inverter

It is the combination many H-bridge modules with its each output voltage are connected in series. It consists of four semiconductor switches such as Sw1, Sw2, Sw3 and Sw4, four diodes with a single dc source. Any number of H-bridge modules can be connected to obtain a desired output voltage level of the cascaded inverter. The voltage sources connected with each H-bridge module can be replaced by any dc voltage source such as a battery, PV cells, fuel cells etc., Each H-bridge module can generate three different output voltage levels of +Vdc, 0 and −Vdc. In order to obtain three levels of output voltages, the switches can be operated in three different sequences.

- Mode 1: +Vdc is produced with the switches Sa_1 and Sd_1 are turned on
- Mode 2: −Vdc is obtained with the switches Sb_1, Sc_1 are turned on
- Mode 3: Sa_1, Sd_1 and Sb_1, Sc_1 are turned on to produce zero voltage at the output.

The voltage at the output is defined by M = 2s + 1 and “s” is denoted by number of dc sources. In this structure, a faulty module can be replaced without affecting the rest of the structure. The output waveform generated 11-level cascaded multilevel inverter by summing up of H-bridge is shown in Fig 2.

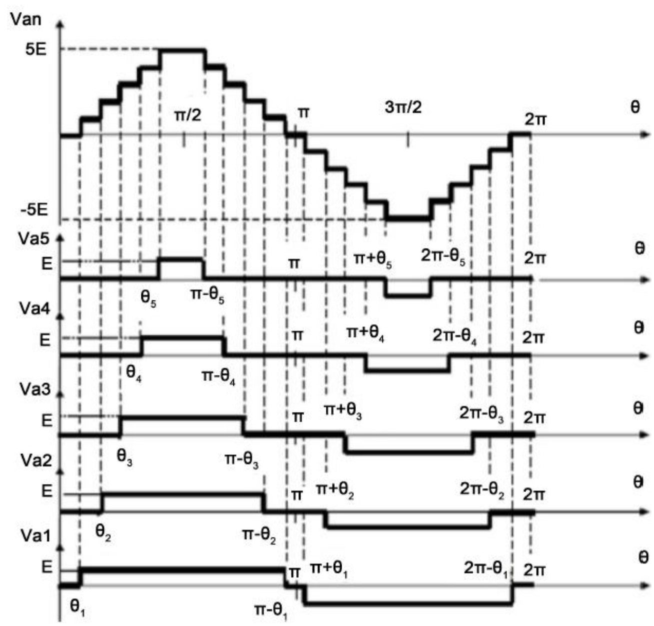

Fig 2. Output waveform of 11-level cascaded multilevel inverter.

The each output of the module is connected in series to get the desired voltage level of the multilevel inverter. Series connection provides the resultant output of the inverter. So, the number of switches used for this structure is lowest while comparing with the conventional multilevel inverter. It can generate the waveform almost closer to sinusoidal. The complexity in control circuit, switching losses, size of the module by the least count of the switching components, requirement of gating circuits are also reduced while comparing with the conventional multilevel inverters.

Thus, asymmetric cascaded multilevel inverter topology significantly increases the number of levels in output voltage for the same number of control switches. Each H-bridge topology produces a quasi-square waveform by phase shifting their positive and negative phase legs with a determined switching timing. The output voltage Vo (Vp) is generated by the summing up of output voltage in each inverter module for various duty cycles. Hence, the voltage of the inverter output is practically sinusoidal. If the number of H-bridge in a single-phase module is greater; then the output voltage Vo would be almost closer to the ac sinusoidal waveform. Thus, the output voltage for an 11-level cascaded H-bridge multilevel inverter is obtained.

III. MODULATION STRATEGIES OF CHMLI

A several types of modulation techniques have been implemented for multilevel inverters to synthesize a desired output voltage levels. They are generally classified in to three categories.

- Space vector modulation (SVPWM) technique
- Carrier based PWM (sine-triangle PWM or SPWM)
- Selective harmonic elimination (SHE)

But above the all, only the SVPWM and SPWM are often used. The SVPWM has more complexity in control when the number of level increased is more than five. Fig 3 shows the phase opposition and disposition of PWM.

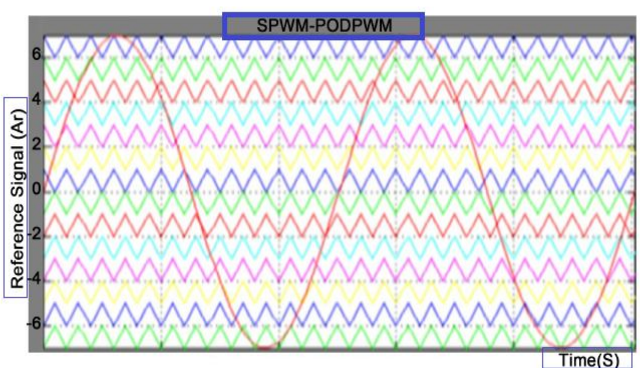

Fig 3. Waveform of Phase opposition disposition PWM.

So the SPWM scheme is almost preferred. Multilevel Carrier based PWM has more than one triangular wave or saw tooth wave form and so on. The modulating or reference signal in carrier based PWM can be sinusoidal or trapezoidal. So, the SPWM scheme is most convenient and is easy to implement. The principle of SPWM is to provide several triangular carrier signals by keeping only one modulating sinusoidal signal. Following Equation (2) is given for an n-level inverter; the (n−1) triangular carriers are required to set the amplitude value and frequency. The carrier frequency fc has the same peak-to-peak amplitude AC. The modulating signals are sinusoidal frequency fm and amplitude Am. At each instant; each carrier signal is compared with the modulating signal. For all comparisons, the switches are switched "on" if the modulating signal is greater than the triangular carrier designated to that switch.

The main factors of the modulation process are the frequency ratio k = fc/fm, where, fm is the frequency of the modulating signal and fc is the carrier frequency. The term Modulation Index (δ) can be realized from the Equation (1) and is given by

$\delta = Ams\ (n * Acs)$(1)

where, "*Ams*" denotes the amplitude of the modulating signal and *Ac* is the peak-to-peak value of carrier signal.

$n = (n - 1)\ 2$(2)

"*k*" refers the number of levels (odd).

3.1. Fuzzy Logic Controller

The Fuzzy logic controller is developed for the proposed model by using nonmathematical solution based algorithms that can be used operator experience. This method is most appropriate for a non-linear system. Fig 4 shows the block diagram for FLC of the proposed inverter.

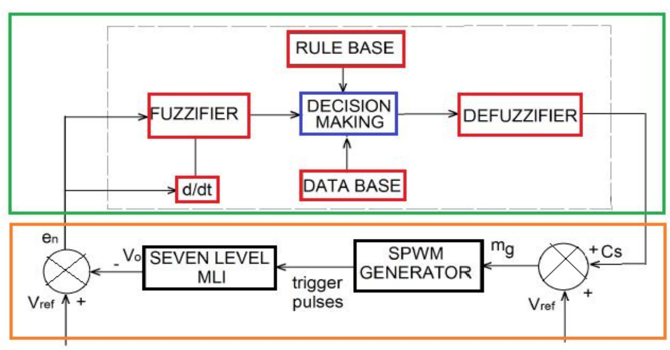

Fig 4. Block diagram of MLI with FLC

The gate signals are generated by SPWM technique. The seven level cascaded inverter output is fed to the load through LC filter in order to produce sinusoidal voltage (Vo) which is compared with the reference voltage (desired voltage-Vref) to generate error signal (en) and so the input to the FL controller is en. The subscript n refers sampling instances.

The output of the FL controller i.e., the compensating signal (Cs) is included with the reference signal to produce the required modulating signal (mg) which is used to generate the gate pulses. As a result, a voltage feedback loop is established to obtain the required sinusoidal voltage at the output. Here a number of steps are followed to obtain fuzzy control surface for non-linear, complex dynamic and time varying systems.

The inputs to the FLC are the error en = Vref −Vo and the change in error ce = en−(en−1). The actual output voltage of the inverter is Vo, the desired output voltage Vref and en−1 is the previous error. The compensating signal Cs is inferred by the FLC. The updated modulating signal mg is obtained by using Cs and fed to SPWM generator which provides a suitable PWM signals.

Buck-Boost Converter and MPPT Method

The Buck-Boost converter consists of two different states (i) on state, the switch S is closed, the inductor current increases and (ii) off state, the switch is open the inductor current flows through the fly back diode D, the capacitor C and load R. This can lead to transfer the energy to the capacitor during the on-state. The current through the inductor (IL) never falls to zero when the converter operates in continuous mode. In a few cases, the sum of energy needed for the load is sufficient to be transferred at a time is lesser than the total switching time.

Here, the current flow through the inductor falls to zero during a part of the period and the converter is assumed to be operated in discontinuous mode. At the end of commutation cycle the inductor is entirely discharged. The MPPT method can be suitably implemented with the help of an algorithm by means of the voltage-power characteristics of the PV modules. The power is reduced or increased by knowing the right and left of the maximum power point by increasing or decreasing the duty cycle. A change in duty cycle of the converter depends on, a most recent change in power. To perform the Perturb and Observer method, U is the power wanted to be read at a time when the voltage is obtained, then the term (U + I) is the power in time. The MPPT algorithm executed for this scheme is used to arrange the necessary adjustment in the buck boost converter's duty cycle to obtain the optimum voltage. Hence, it allows the maximum power supplied to the load.

IV. SEVEN LEVEL MULTILEVEL TOPOLOGY

A new topology of a seven level asymmetric cascaded H-bridge multilevel inverter (ACHMLI) with six switches is proposed here. The low and medium power industrial and domestic gadgets are experiencing many serious power quality issues. The harmonic level of many inverter output are not able to meet the IEEE harmonics standard. By increasing the number of levels in the output of multilevel inverters, the output is also more step levels of staircase waveform, which has a reduced harmonic distortion. If the number of level of output voltage increases, then the number of switches also increased. This phenomenon leads to the complexity in control circuits. The multilevel inverter is able to produce an output voltage with reduced harmonic distortion and lower electromagnetic interference. Therefore by considering these facts which are affecting the harmonic standards, a new topology of a seven level asymmetric cascaded H-bridge multilevel inverter (ACHMLI) with six switches is proposed here. The output voltage presents, less harmonic content and produced a sinusoidal voltage. It is realized that the number of power semiconductors required for an inverter is increased then the inverter circuit size is also increased and hence the complexity of control circuit is also increased. The power consumption is also more and thereby increased in overall system cost. The proposed model is designed by means of one H-bridge and two switches were connected with two flywheel diodes. Given that the number of switches is minimized for a seven level output of the proposed PV inverter, the gate driver circuit and space required is also reduced.

V. SIMULATION RESULTS AND DISCUSSION

The proposed 7 level ACHBMLI was simulated by using MATLAB/Simulink tool box. The simulation of the proposed system is shown in Fig 5 and Fig 6.

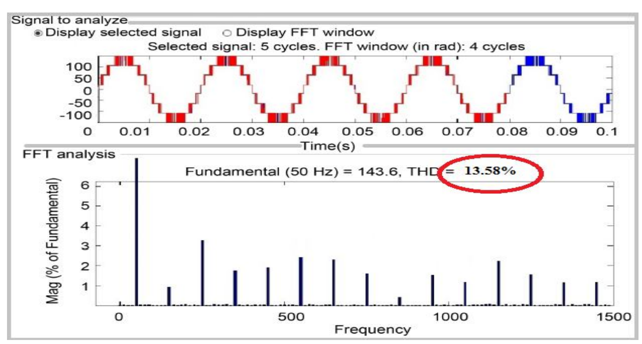

Fig 5. Seven level output voltage waveform

The proposed asymmetric inverter topology consists of three different voltage ratings of PV modules, buck-boost converter with an MPPT controller, cascaded H-bridge module and an IGBT driver circuit with a FLC controller.

Also, it provides a better output power quality, which is most suitable for the application of PV fed inverter. The various intensity of sunlight provides uneven input voltage to the buck-boost converter and the dc/dc converter regulates a constant output voltage from the different voltage ratings (1:2:4) of PV modules. The proposed multilevel inverter further converted to AC, which can be used to feed the nonlinear loads.In this setup, there are six IGBT switches used instead of nine and seven switches in the existing topology for producing the same output voltage level. Pulses are generated by the driver circuit according to the voltage analyzed from the output voltage reference block.

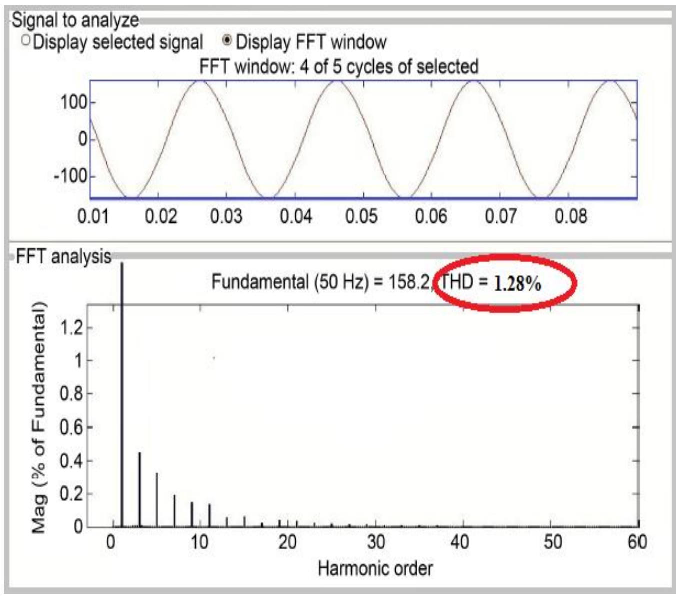

Fig 6. FFT analysis of the proposed system

The voltage is generated due to the light intensities on the surface of the PV panel. Simulations have been conducted using SPWM method by comparing a reference signal as sine wave and carrier signal as triangular wave with fuzzy logic control. Harmonic analysis also done using FFT window in MATLAB/SIMULINK. The uniform step output voltage waveforms of seven level inverter obtained by simulation is shown in Fig 5. From the results, it shows that the THD of current and voltage harmonics thus obtained by six switches produce 14.38% with R load and 1.66% with RL load which is shown in Fig 6. Hence, the harmonics produced at the output have the lowest THD and it offers good performance of the system. The odd harmonics are found appropriately less and it is almost reduced and satisfies the IEEE 1952-519 standard of harmonics.

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