An improve SAR ADC using Reversible Gates

Farhat Siddique[1], Asst. Prof Shubhangini Ugale[2]
[1, 2] Department of Electronics and communication
[1, 2] G.H.R.A.C.E.T

Abstract- *The analog to digital converters ADCs are the vital branch of communication system and signal processing. Among many ADCs successive approximation register (SAR) ADCs are suitable because of low power and small area. The design and implementation details of SAR ADC using reversible gate is implemented in this paper. The proposed 8bit SAR ADC is implemented at high frequency in 90nM technology with tanner tool .As compare to previous implementation we are reducing the power using reversible gates. Reversible gates have attracted more attention because it is usually used to optimize the power of the system. In SAR block of SAR ADC, in place of CMOS gate we are using reversible gates which are built by using buffered CMOS logic than complimentary transistors so that we can achieve low power dissipation.*

Keywords- Reversible gates, successive approximation analog to digital converter, CMOS gate.

I. INTRODUCTION

Signal processing is very important in many of the system on-a-chip applications. As the technology is going so advance, digital signal processing has gained significant importance in the field of control systems telecommunication, biomedical and so on. Analog to digital converters (ADCs) is a mixed signal device that converts analog signals this analog signals are real world signals to digital signals for processing the information. . In the real world most we sensed a signal which is analog signals like light sound, conversion of audio signals like mobile, micro, digital music records etc,conversion of video signals like cameras,frame, grabber etc , measurement system ex- speed, data acquisition system ex.-voltage, current , temperature sensor etc. and data communication system like line communication system ex landline telephone and radio broadcasting communication ex internet, radio etc . ADC used in modem to convert the incoming audio from a twisted-pair line in to signals so the computer understand it, these are the various examples. In the recent years, the need to design a low voltage, low power, high speed and wide bandwidth analog-to-digital converter has increased tremendously. Therefore the focus of this research is to design efficient low power ADCs that operate at high frequency. There are several different types of ADCs available like Direct-conversion ADC or flash ADC, Successive-Approximation ADC, .Pipeline ADC, Cyclic ADC.

1.1 Successive Approximation ADC

Successive-approximation ADC has been the main stay of signal conditioning for many years. A successive approximation ADC convert analog to digital signal i.e a continuous analog waveform into a digital signal and perform a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.SAR ADCS have attracted more attention because of excellent power efficiency, scalability and characteristic of digital nature .The energy limited applications such as wireless sensing devices for wearable products or portable, require high efficient ADCs for extending the battery life of these devices. SAR ADCs are also used in other applications such as high speed wire line and wireless communication systems where low power and low area require.

Block Diagram of SAR ADC

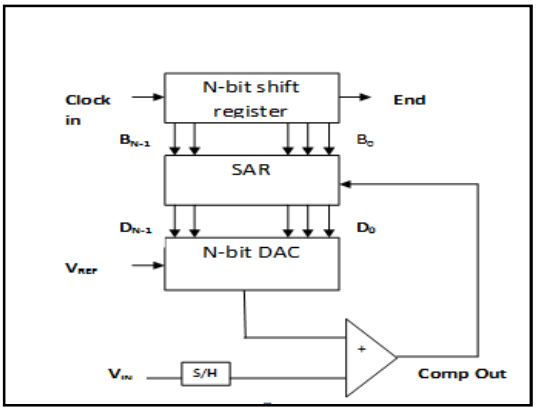


Fig.1 Block diagram of SAR ADC

SAR ADC converter includes-bit Shift register , SAR register, N-bit digital to analog converter and comparator.

In this circuit, V_{IN} voltage is given to sample and hold circuit, it hold the value till the end of conversion. The output of DAC compare with V_{IN} in the comparator, here comparator controls the direction of binary search which perform by successive approximation converter. The output of comparator goes to the SAR register then the output of SAR register is the final digital conversion. Now we will see how it works first , the output of DAC is compare with V_{IN} , if output of DAC is greater than VI_N then the output of comparator is 1 it means there is right shifting in shift register. If V_{IN} is greater than output of DAC then the output of comparator is 0 it means there is left shifting in shift register ,whatever operation will performed the value goes to DAC block to convert that digital value in to analog value . Again the output of DAC compare with V_{IN}, this process is continue till the output of

DAC converges to the value of V_{IN} within the resolution converter.

1.2 Reversible gates

Power dissipation is the most important issue in digital circuit design. A part of power dissipation, energy loss occurs due to switches and materials. Reversible logic has emerged as a promising technology in recent years because it has the ability to reduce the power dissipation which is the actual requirement in low power CMOS design. Reversible logic has many applications in quantum computing, optical computing, cellular automata, nanotechnology, low power CMOS etc. The advantage of reversible logic is that its operations do not erase information it means there is no loss of any information while in irreversible logic gates which is the traditional gates for example AND,OR,XOR these are irreversible gates in which each bit of information loss generate. A reversible logic gate is n-input n-output logic device with one to one mapping. This helps us to determine the output from input and also the inputs can be uniquely recovered from the outputs. If we use reversible gate in our design we can solve the problem of power dissipation. The important reversible gates used for reversible for reversible logic synthesis are Feynman, Fred kin , Peres, Toffoli etc. In our design we used Feynman and Peres gate.

Feynman gate

The Feynman gate which is 2*2 gate and is also called as Controlled Not gate and it is widely used for fan-out purposes. The inputs (A, B) and outputs P=A, Q=A XOR B.

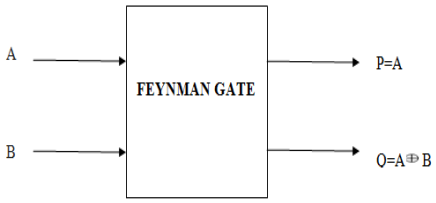


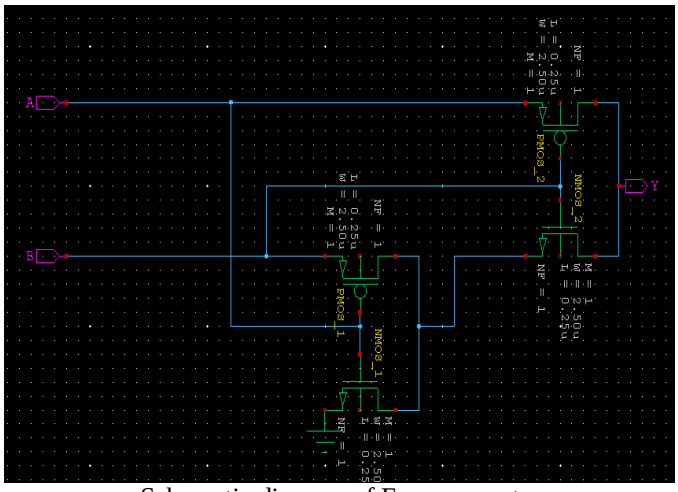
Fig.2 Block Diagram of Feynman gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

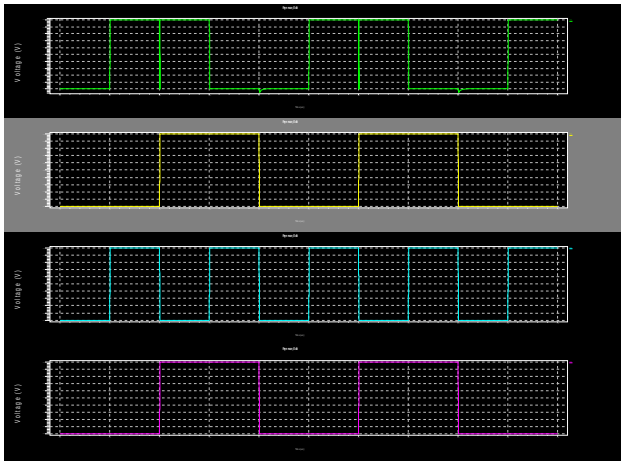
Table.1 Truth Table of Feynman gate

Schematic diagram of Feynman gate

As we know that in transistor when gate value is 0 and source value is 1 P_{MOS} gets ON and when gate value is 1 and source value is 0 then N_{MOS} gets ON. Here in the schematic suppose we take the example if A=0 and B=0 we get the output 0, in this when A=0 ,P_{MOS-2} will get OFF ,P_{MOS-1} will also get OFF at B=0 ,N_{MOS-1} and N_{MOS-2} will also get OFF so we get the output 0.Now we will take the another example from truth table, if A=0 and B=1 the output we get 1,in the schematic , when A=0 P_{MOS-2} will off and P_{MOS-1} will ON and for B=1 N_{MOS-2} will get ON and N_{MOS-1} will off so we get the output 1. Similar process for another value. From this schematic we get the waveform based on the value of truth table.



Schematic diagram of Feynman gate



Waveform of Feynman gate

A) Peres Gate

Peres gate which is a 3*3 gate having inputs(A, B, C) and outputs P=A; Q=A XOR B; R= AB XOR C.

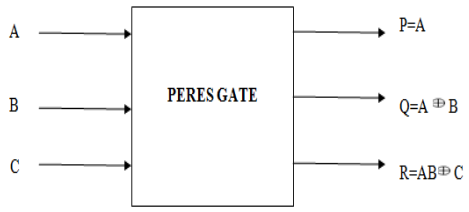


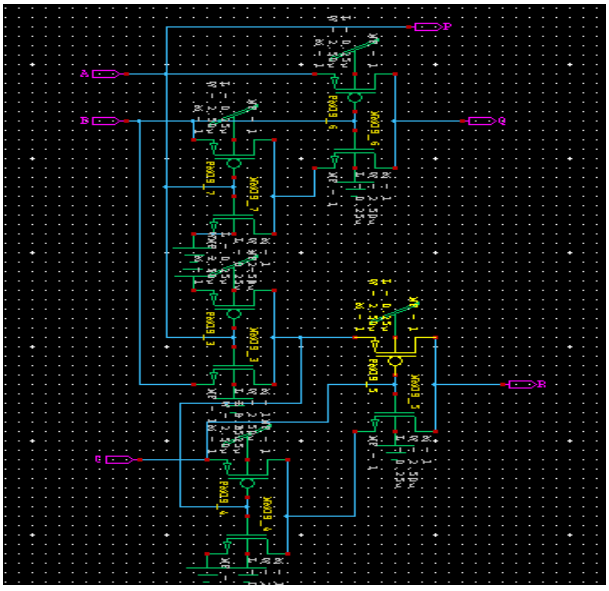
FIGURE-2: 3×3 PERES GATE

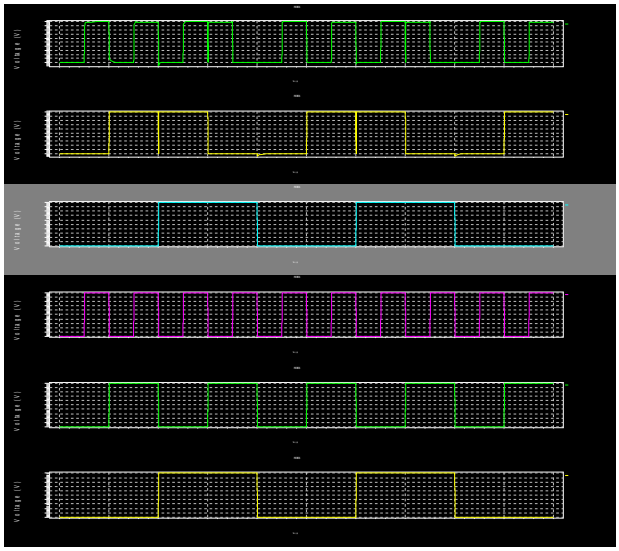
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table.2 Truth Table of Peres gate

Schematic diagram of Peres gate

In this circuit suppose we take the example, A=0, B=1 ,C=0, P_{MOS-6} will get off N_{MOS-6} will get ON therefore we get output Q=1 and from these values P_{MOS-5} and N_{MOS-5} both will get off so we get R=0. We get the waveform from below schematic diagram which is based on the value of truth table of Peres gate.

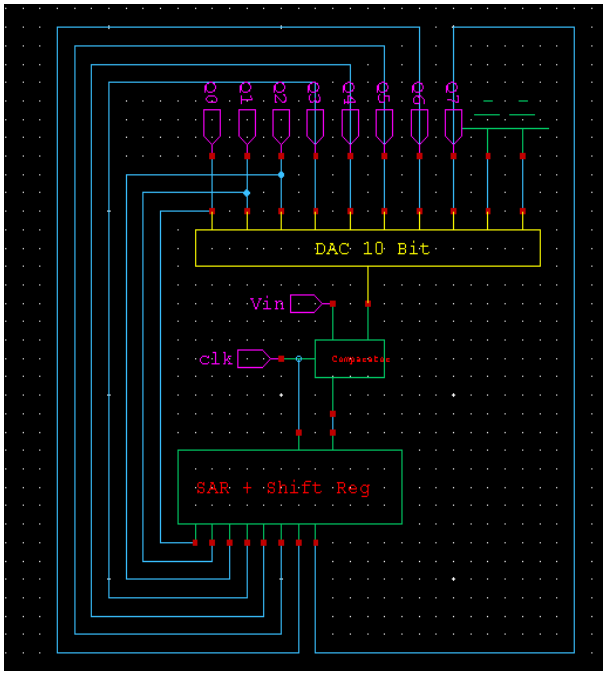




Waveform of Peres gate

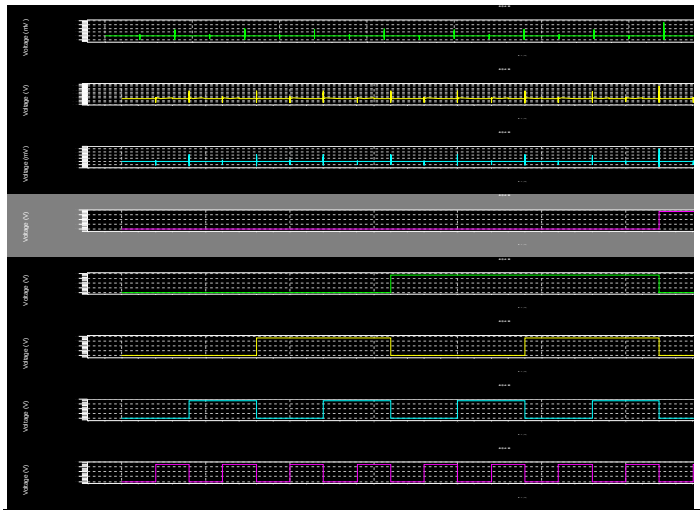
1.3 Proposed architecture diagram of SAR ADC

Here we took the initial value of output of DAC is 0V and V_{IN} is 0.1V, then we compared output of DAC with V_{IN}. We saw that V_{IN} is greater the ouput of DAC so the compactor output 0 or can say it count down from these the digital value shifted to the left side then went to the DAC which convert that digital value on to analog value again it compared with V_{IN}, That process we continued till the output of DAC converges to the value of V_{IN} and we got the result in to digital form.



Simulation result of above schematic diagram

In above schematic diagram of 8bit SAR ADC we used the supply voltage VDD=1.8v , V_{IN}= 0.1V and the output we get in the digital form of 8bit from the result we get the average power which is 7.9nW as compare to existing implementation we reduced the power which our a actual objective here.



II. CONCLUSION

Power consumption is very imp issue in the modern devices and growing in demand to extend the battery life and it is very important in low area devices like watches etc. Reversible logic gate is known for zero power dissipation from it the no of transistors reduced which leads to reduce area automatically and we used it in our design to reduce the power. In this paper, the power optimization architecture is demonstrated by the design of SAR ADC using reversible gates which is the best method than other methods.

REFERENCES

[1] Kai-Hsiang Chiang. Soon-Jyh Chang, Guan-Ying huanh and Ying-zu lin, “A 10b100KS/s SAR ADC with Charge Recycling Switching Method.”IEEE 2014 conference.

[2] Hooman Farkhani and Mohammad Meymandi-Nejad,Manoj Sachdev ,“A Fully Digital ADC Using A New Delay Element With Enhanced Linearity”, IEEE 2008 conference..

[3] Baiying Yu, William C . Black, Jr ,“A 900MS/s 6b Interleaved CMOS FLASH ADC”, IEEE 2001 conference

[4] Young-Kyun Cho,Young-Deuk Jeon ,Jae-Won Nam,Jong-Kee Kwon, “A 9-bit 80 MS/s SAR ADC Converter With a Capacitor Reduction Technique” , IEEE 2010 conference..

[5] Mahesh Kumar Adimulam, Sreehari Veeramachaneni,N Moorthy Muthukrishnan, M.b Srinivas, “A Novel, Variable Resolution Flash ADC with Sub Flash Architecture”, IEEE 2010 conference.