Area Efficient Cordic based Integer DCT Architectures for HEVC

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Abstract- *Now a days the signal processing domain is bottleneck parameter performance like area, latency. In this work looking to provide area efficient Integer DCT designs for HEVC. So that invoked Cordic architecture to produce on fly trigonometric output instead of traditional method. In Integer DCT have its own style of operation and to calculate twiddle factor of integer DCT Cordic architecture actively introduced and make sustainable result in area. The computational complexity is has been reduced considerably fully as compare to traditional operations. The experimental results show that the proposed DCT algorithm only reduces the computational complexity significantly, but also keeps the good transformation quality of the Integer DCT.*

Keywords- Discrete Cosine Transform (DCT) High Efficiency Video Coding (HEVC) Integer Discrete Cosine Transform (IDCT).

I. INTRODUCTION

One of critical normal for HEVC is that it chains DCT of distinctive sizes, for example, 4, 8, 16, and 32. In this way, the equipment building design throught to be sufficiently adaptable for the processing of DCT of any of these diverse lengths. The current outlines for customary DCT based on constant matrix multiplication (CMM) and MCM can give ideal answers for the processing of any of these distinctive lengths, however they are not reusable for any length to backing the same throughput transforming of Integer DCT of diverse change lengths. Considering this subject, this have broke down the conceivable usage of whole number DCT for HEVC in the situation of asset prerequisite and reusability and taking into account that, the proposed calculation has been inferred for equipment execution. This work has composed versatile and reusable architectures for 1-D and 2-D whole number DCTs for HEVC that could be reused for any of the endorsed lengths with the same throughput of handling regardless of change size. In way of analyzing design with multiplication and its corresponding area results are not good to compare with current architectures. The current design invoking CORDIC based Integer DCT can be good to produce on fly computation of cosine terms instead of predefined stored values in LUT tables. In the earlier period, this research has been completed on low power DCT designs.

II.PROPOSED ARCHITECTURES FOR CORDIC DCT COMPUTATION

This has analyzed the possible implementation of integer DCT for HEVC in the circumstance of resource requirement and reusability and based on that, the proposed algorithm has been derived for hardware implementation. This work have designed scalable & reusable architectures for one-Direction and two-Direction integer DCTs for HEVC that could be reused for any one of the prescribed lengths with the same throughput of processing irrespective of transform size.

2.1. PROPOSED BLOCK DIAGRAM FOR CORDIC DCT

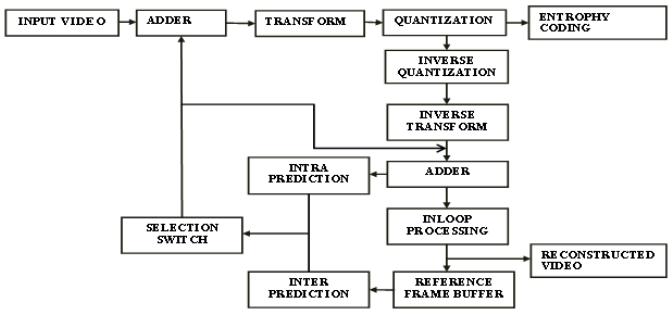


Fig.1 block diagram of Cordic DCT

2.1.1Traditional Architecture for eight-Point Integer DCT

The Traditioanl architecture for eight-point integer DCT is shown in Fig. 1(a). It consists of three adder units. They are input adder unit (IAU) a shift-add unit (SAU), and an output adder unit (OAU). The calculation of t0, 64 and t1,64 does not devour any rationale since the movement operations could be rewired in equipment. The structure of SAU is indicated in Fig. 1(b). output of the SAU are at last added by the OAU as indicated by STAGE-3 of the calculation.

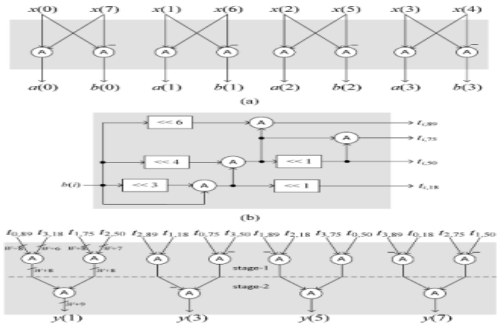


Fig.2 (a) 8 –point traditional Integer DCT IAU (b) Structure of SAU(c) Structure of OAU unit

The proposed outline has been summoning Cordic based plan in an Integer DCT. This usage requires just 38 include and 16 movement operations. I have taken the first Integer DCT as the beginning stage for our improvement, on the grounds that the hypothetical lower bound of the quantity of increases needed for the 1-D 8-point DCT. Keeping in mind the end goal to infer the proposed calculation, I first consider the butterfly toward the start of diagram as demonstrated in Figure 2.

The degree butterflies with scaling variables 3pi/8, 1pi/16 and 3pi/16 can likewise be supplanted by Cordic utilizing q = 3pi/8, 1pi/16 and 3pi/16 separately. Henceforth, this can supplant all butterflies in the Integer DCT to determine the unadulterated Cordic based Integer DCT.

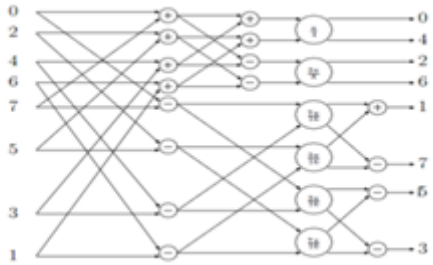


Fig. 3 Proposed 8-point Integer DCT with CORDIC

2.2 CORDIC

CORDIC (COordinate Rotation DIgital Computer), also known as the digit-by-digit method and Volder's algorithm, is a simple and efficient algorithm to calculate hyperbolic and trigonometric functions. It is commonly used when no hardware multiplier is available (e.g. in simple microcontrollers and FPGAs) as the only operations it requires are addition, subtraction, bit shift and table lookup.

2.3 INVERSE TRANSFORMS

Using the normalization conventions above, the inverse of DCT-I is DCT-I multiplied by 2/(N-1). The inverse of DCT-IV is DCT-IV multiplied by 2/N. The inverse of DCT-II is DCT-III multiplied by 2/N and vice versa. Like for the DFT, the normalization factor in front of these transform definitions is merely a convention and differs between treatments. For example, some authors multiply the transforms by $\sqrt{2/N}$ so that the inverse does not require any additional multiplicative factor. Combined with appropriate factors of √2 (see above), this can be used to make the transform matrix orthogonal.

2.3.1MULTIDIMENSIONAL DCTS

Multidimensional variants of the various DCT types follow straightforwardly from the one-dimensional definitions they are simply a separable product (equivalently, a composition) of DCTs along each dimension.For example, a two-dimensional DCT-II of an image or a matrix is simply the one-dimensional DCT-II, from above, performed along the rows and then along the columns (or vice versa). That is, the 2D DCT-II is given by the formula

$$X_{k_1,k_2} = \sum_{n_1=0}^{N_1-1}\left(\sum_{n_2=0}^{N_2-1} x_{n_1,n_2}\cos\left[\frac{\pi}{N_2}\left(n_2+\frac{1}{2}\right)k_2\right]\right)\cos\left[\frac{\pi}{N_1}\left(n_1+\frac{1}{2}\right)k_1\right]$$

$$= \sum_{n_1=0}^{N_1-1}\sum_{n_2=0}^{N_2-1} x_{n_1,n_2}\cos\left[\frac{\pi}{N_1}\left(n_1+\frac{1}{2}\right)k_1\right]\cos\left[\frac{\pi}{N_2}\left(n_2+\frac{1}{2}\right)k_2\right].$$

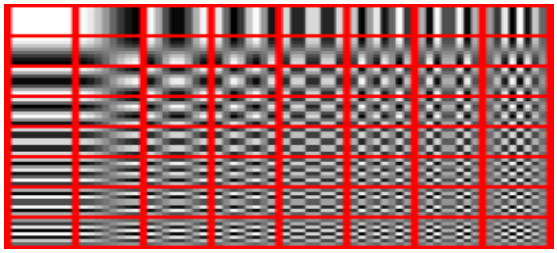


Fig .4 Two-dimensional DCT frequencies from the JPEG DCT

Technically, computing a two- (or multi-) dimensional DCT by sequences of one-dimensional DCTs along each dimension is known as a row-column algorithm (after the two-dimensional case). As with multidimensional FFT algorithms, however, there exist other methods to compute the same thing while performing the computations in a different order (i.e. interleaving/combining the algorithms for the different dimensions).The inverse of a multi-dimensional DCT is just a separable product of the inverse(s) of the corresponding one-dimensional DCT.

2.4 HIGH EFFICIENCY VIDEO CODING

High Efficiency Video Coding (HEVC) is a video compression standard, a successor to H.264/MPEG-4 AVC

(Advanced Video Coding), which was jointly developed by the ISO/IEC JTC 1/SC 29/WG 11 Moving Picture Experts Group (MPEG) and ITU-T SG16/Q.6 Video Coding Experts Group (VCEG) as ISO/IEC 23008-2 MPEG-H Part 2 and ITU-T H.265.MPEG and VCEG established a Joint Collaborative Team on Video Coding (JCT-VC) to develop the HEVC standard. Version 1 of HEVC was finalized on January 25, 2013 and the specification was formally ratified .The eight point integer DCT unit has been designed with CORDIC algorithm, to compute cosine terms in on fly need to compute Integer DCT, where multiplication have to perform at the same time where it have to do addition operation.Fig.5 Shows synthesis result of 8-point DCT with CORDIC.

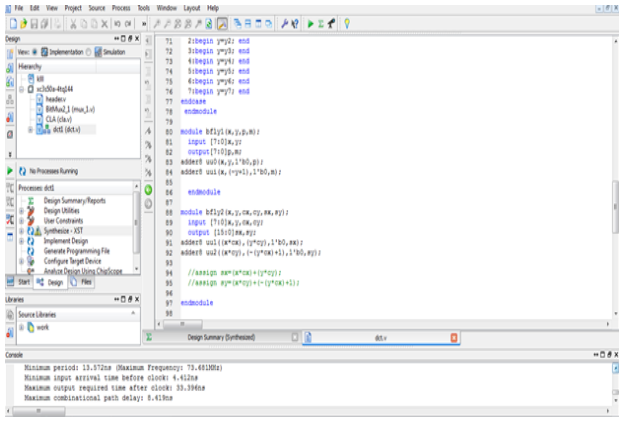


Fig .5 Synthesis of 8 – point IDCT with CORDIC

Video coding standard	Average bit rate reduction compared to H.264/MPEG-4 AVC HP			
	480p	720p	1080p	4K UHD
HEVC	52%	56%	62%	64%

Table .1 bit rate reduction comparision

In a subjective video codec comparison released in by the EPFL, the HM-15.0 HEVC encoder was compared to the VP9 1.2.0-5183 encoder and the JM-18.8 H.264/MPEG-4 AVC encoder. Four 4K resolutions sequences were encoded at five different bit rates with the encoders set to use an intra period of one second. In the comparison, the HM-15.0 HEVC encoder had the highest coding efficiency and, on average, for the same subjective quality the bit rate could be reduced by 49.4% compared to the VP9 1.2.0-5183 encoder, and it could be reduced by 52.6% compared to the JM-18.8 H.264/MPEG-4 AVC encoder.

III. IMPLEMANTATION RESULTS AND DISCUSSIONS

3.1 SYNTHESIS TOOL

3.1.1XILINX ISE

For two-and-a-half decades, Xilinx has been at the forefront of the programmable logic revolution, with the invention and continued migration of FPGA platform technology. During that time, the role of the FPGA has evolved from a vehicle for prototyping and glue-logic to a highly flexible alternative to ASICs and ASSPs for a host of applications and markets. Today, Xilinx® FPGAs have become strategically essential to world-class system companies that are hoping to survive and complete in these times of extreme global economic instability, turning what was once the programmable revolution into the “programmable imperative” for both Xilinx and our customers.

The eight point integer DCT unit has been designed with CSA(Carry Select adder) and for multiplication operation left shifter has been used and it could perform multiplication operation where multiplication and addition operations are follows the algorithm, where multiplication have to perform at the same time where it have to do addition operation.Fig.6 Shows synthesis result of 8-point DCT with CSA.

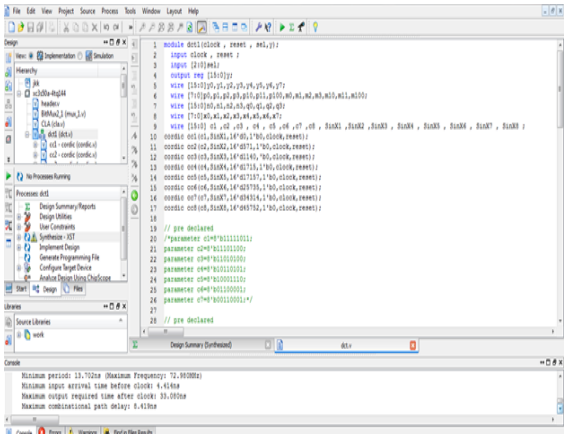
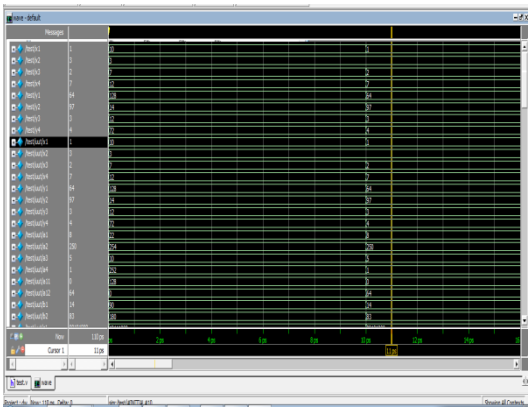


Fig.6 Synthesis result of 8 – point Existing Integer DCT .

IV. RESULT

In this work has acknowledge skillfully a low tangling and awesome DCT change in light of the Cordic computation is shown. The proposed Cordic based Integer DCT building plan simply have need of 78 cuts rather than 120, number of LUT's are 110 rather than 156 and deferral has been diminished to 2ns so speed has been enhanced in ideal level. The proposed count not simply lessens the computational multifaceted design widely stood out from the first customary DCT, it in like manner keeps the considerable

quality change result. In this look upon, the proposed DCT figuring is amazingly suitable for low zone and fast sign changing applications, for instance, HEVC. Usually any VLSI design has been verified using simulation software and it is synthesized using implementation software. For a given input 4-point integer DCT has been verified.



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