Shift Register Design using Pulse Triggered Flipflop

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Abstract- *The timing elements and clock interconnection Networks such as flip-flops and latches, is One of the most power consuming components in modern very large Scale integration (VLSI) system. The area, power and transistor count will compared and designed using several latches and flip flop stages. Flip Flop is a circuit which is used to store state information. Power consumption is one of the main objectives in designing a flip flop. The flip flops used in designing are Hybrid Latch Flip Flop (HLFF), explicit-pulsed data-close-to-output flip-flop (ep-DCO) and Adaptive-Coupling Redundant Flip-Flop (ACFF). Compare pulse triggered latches based on transistor count, power and layout area. Constructing shift registers by using conditional capture pulsed latches instead of normal flipflops, because a pulsed latch is much smaller than a flip-flop. All the latches and flip flop designs are made by using 90nm technology in DSCH2 schematic tool and MICROWIND design tool.*

Keywords- Pulse Triggered Flip Flop design, Microwind, Dsch2,VLSI

I. INTRODUCTION

In VLSI design power consumption has become a very important issue. Sequential logic circuits, such as registers, memory elements, counters etc., are heavily used in the implementation of Very Large Scale Integrated (VLSI) circuits. Power dissipation is critical for battery-operated systems, such as laptops, calculators, cell phones and MP3 players since it determines the battery life. Therefore, designs are needed that can consume less power while maintaining comparable performance. Flip-flop is a data storage element. The operation of the flip-flops is done by its clock frequency. When multistage Flip-Flop is operated with respect to clock frequency, it processes with high clock switching activity and then increases time latency. Therefore it affects the speed and energy performance of the circuit. Various classes of flip-flops have been proposed to achieve high-speed and low-energy operation. In the past decades, many works has been dedicated to improve the performance of the flip-flops.

II. FLIP FLOP DESIGN

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design. The requirements of designing a flip flop are as follows.

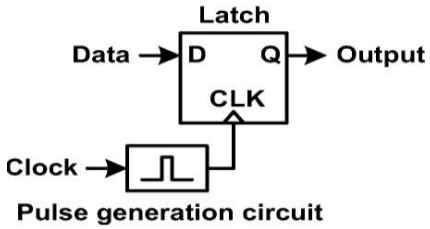

Fig 1 Pulse Generation unit

A. Pulse-Triggered Flip-Flops

Pulse-triggered flip-flops can be classified into two types, implicit and explicit, and this classification is due to the pulse generators they use. In implicit-pulse triggered flip-flops (ip-FF), the pulse is generated inside the flip-flop, for example, hybrid latch flip-flip (HLFF), semi-dynamic flip-flop (SDFF), and implicit-pulsed data-close-to-output flip-flop (ip-DCO). Whereas, in explicit-pulse triggered flip-flops (ep-FF), the pulse is generated externally, for example, explicit- pulsed data-close-to-output flip-flop (ep-DCO) and the flip-flops.

At first glance, ep-FF consumes more energy due to the explicit pulse generator. However, ep-FF has several advantages. First, ep-FF can have the pulse generator shared by neighboring flip-flops, a technique that is not straightforward to use in ip-FF. This sharing can help in distributing the power overhead of the pulse generator across many ep-FF, and a system using ep-FF will be more energy efficient than a system using ip-FF.

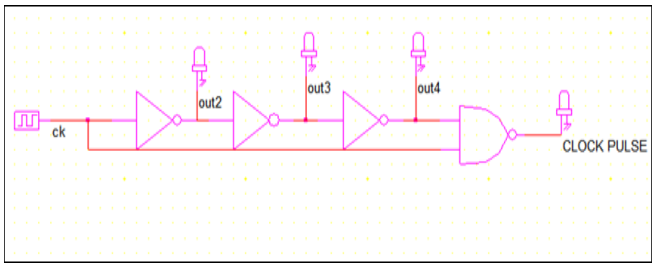

Fig 2 Pulse Generation unit

Second, double-edge triggering is straightforward to implement in ep-FF, but it is difficult to deploy in ip-FF. Using double-edge triggering, where data latching or sampling is issued at both the rising and falling edges, usually allows the clock routing network to consume less power. For example, for a system with a throughput of one operation per cycle and a clock frequency, double-edge triggering results in two operations being executed in one cycle; if we use half the frequency, we can maintain the same throughput of the original system. With half the frequency, the clock switching activity is reduced by half, which leads to considerable power savings in the clock routing network. Third, ep-FF could have the advantage of better performance as the height of the NMOS stack in ep-FF is less than that in ip-FF. With this rationale, the authors believe that ep-FF topology is more suited for low-power and high-performance designs.

B. Explicit Pulsed Data Close to out (Ep-DCO)

The schematic for the ep-dco flip-flop; its semi-dynamic structure consists of two stages: a dynamic (first stage) and a static stage (second). After the rising edge of the clock, transistors N2 and N3 turn on for a short period of time, which is equal to the delay incurred by the pulse generator. During this period, the flip-flop is transparent and the input data propagates to the output. After the transparent period, the pull-down paths in both stages are turned off via the same transistors N2 and N3. Hence any change at the input cannot pass to the output. Keepers are used to maintain the output and internal node states when the circuit is in the hold mode.

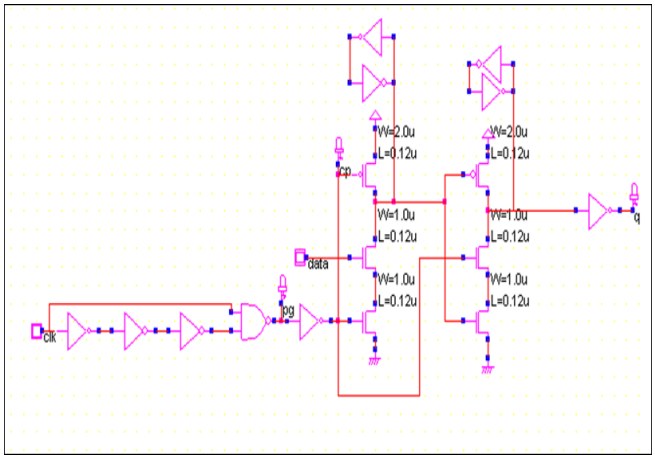

Fig 3 Explicit Pulsed data close to out

C. Transmission Gate Flip Flop Design

The basis of the operation is that the two transmission gates operate alternatively. This is obvious if one looks at the way the enable input is connected to them: EN is connected to the n type transistor of the upper gate, while it is connected to the p type transistor in the lower one. Thus when EN falls to 0, the transmission gate at the input of the latch cuts off and separates the input from the output. At the same moment, the other gate in the feedback branch starts to conduct and will connect the output to the input of the first inverter. This is a stable circuit where the input capacitance of the inverters holds the information

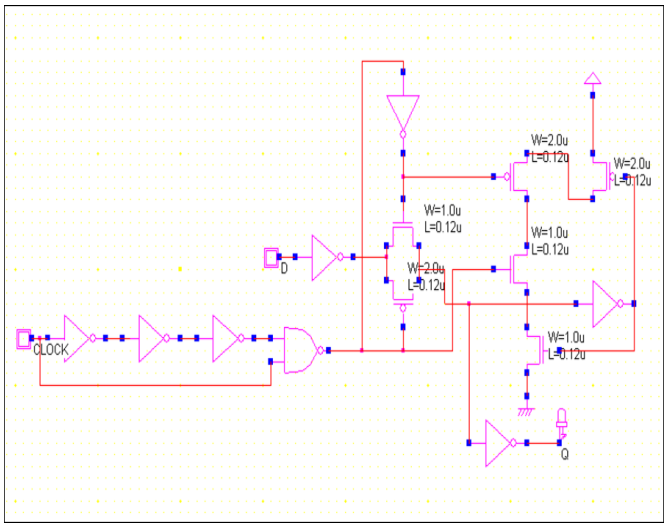

Fig 4 Transmission Gate Flip Flop Design

D. Hybrid Latch Flip Flop Design

Hybrid Latch Flip-Flop is one of today's high-performance flip-flops. The power consumption of HLFF mainly consists of two parts, the static power and the DC leakage power. To reduce the first one, since the toggling rate and supply voltage of the circuit cannot be changed, the only way is to size down the transistors to reduce the capacity. For the second case, there is a tradeoff between decrease current and rising/falling time.

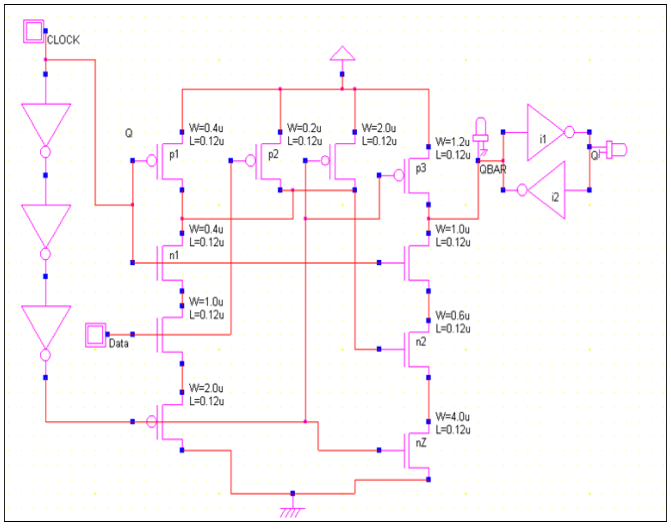

Fig 5 Hybrid Latch Flip Flop Design

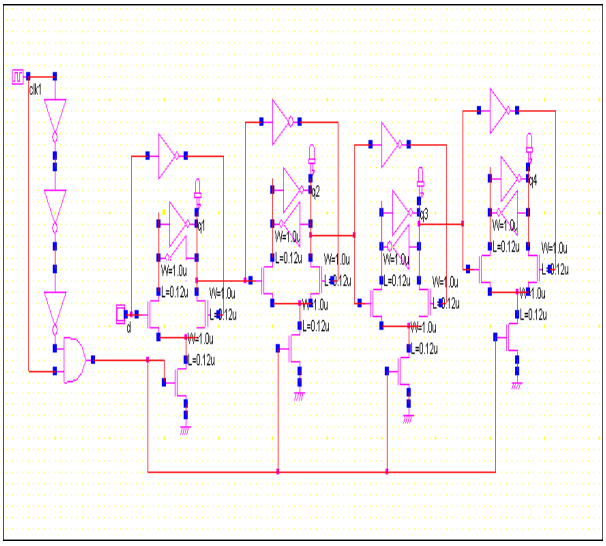

Fig 6 Proposed Design

The several flip flop designs and latches are designed and 4 bit shift register is designed using Static differential sense amp shared pulse latch. The input Data (d), with respect to clock pulse is processed by D flip flop with various latches is designed and its results are shown here. The result shows the data to Q delay and power consumed.

III. RESULTS AND DISCUSSION

Node X shown in fig 3 is charged and discharged at every clock cycle, especially when the input D is not changing. Since these internal activities do not produce useful operation, the part of power dissipated during the charge/discharge events does not contribute to the circuit operation. Moreover, while the output is HIGH, the repeated charging/discharging of node in each clock cycle causes glitches to appear at the output displayed in fig 7.

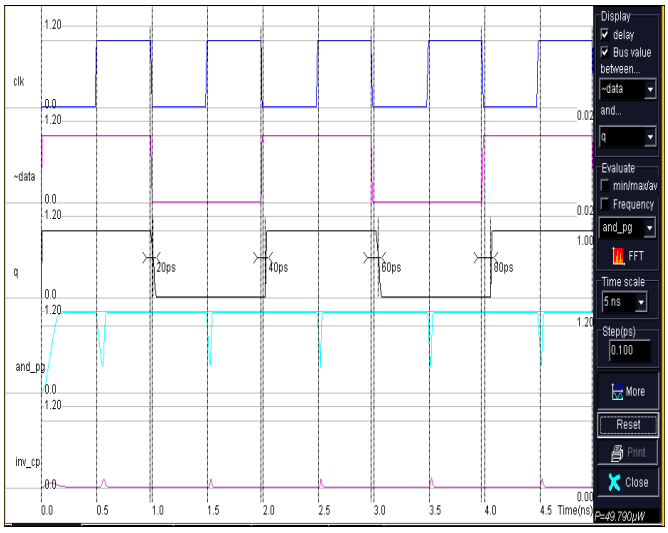

Fig 7 Ex-DCO result

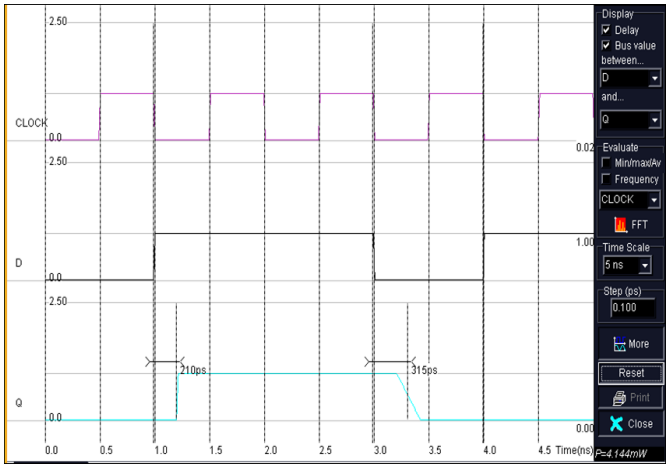

Fig 8 Transmission Gate Flip flop Design result

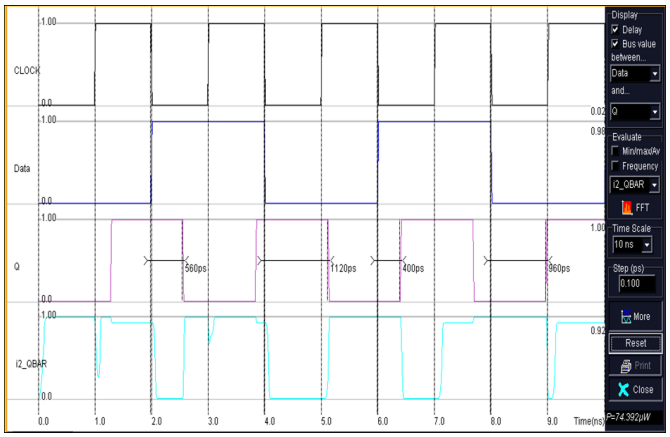

Fig 9 HL Flip flop Design result

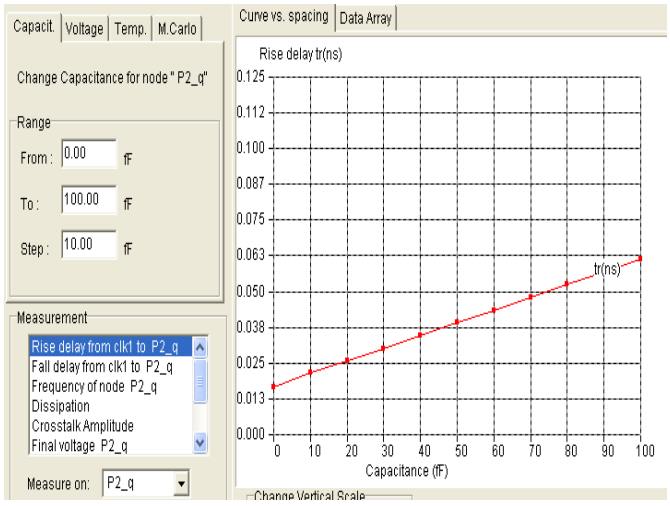

Fig 10 Rise Time Indication of proposed Design

IV. CONCLUSION

The pulse Triggered concept were stuided in flip flops such as Transmission gate flip flop-TGFF, Hybrid latch flip flop, CCFF, Explicit pulse-Data Close to Out and Adaptive-Coupling Redundant Flip-Flop for power

consumption. Using these flip flop design comparison CCFF is considered and it is used to design Shift Registers with delay element were designed. Thus different flip flop structures can be used for different applications considering the parameters such as power, gate count and delay. The shift registers were designed.

V. FUTURE ENCHANCEMENT

There are many other different techniques available to reduce the power consumption in the flip flops such as Low swing Voltage, Conditional operation, Clock gating etc. And power consumption can be reduced by using low swing voltage approach. If supply voltage is halved the switching activity of the transistor will be reduced leads power reduction. Then transistor scaling or layout optimization is another way to reduce power consumption.

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