Implementation and Impact of LNS MAC units in Digital Filter Application

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Abstract- *The logarithmic number system (LNS) is an efficient way to represent data in VLSI processors because its round-off error behavior resembles that of floating point arithmetic. LNS reduce the power dissipation in signal-processing-related application such as hearing-aid devices, video processing and error control.*

This project presents techniques for low-power addition/subtraction in the LNS and quantifies their impact on digital filter VLSI implementation. The operation of addition and subtraction are difficult to perform in LNS as complex look up tables (LUTs) are needed. The impact of partitioning the lookup-tables required for LNS addition/subtraction on complexity performance and power dissipation is quantified. LNS base and LNS word are the two design parameters exploited to minimize complexity. A round-off noise model is used to demonstrate the impact of base and word-length on SNR of the output of FIR filters. In addition, techniques for low-power implementation of an LNS multiply accumulate (MAC) units are investigated. The proposed techniques can be extended to co-transformation-based circuits that employ interpolators. The results are demonstrated by evaluating the power dissipation, complexity and performance of several FIR filter configurations comprising one, two or four MAC units.

Simulation of placed and routed VLSI LNS-based digital filters using Xilinx ISE reveal that significant power dissipation savings are possible by using optimized LNS circuits at no performance penalty, when compared to linear fixed-point two's-complement equivalents.

Keywords- LNS, MAC, XILINX software, FPGA

I. INTRODUCTION

Data representation is an important parameter in the design of low-power processors since it affects both the switching activity and hardware complexity. The logarithmic number system (LNS) has been investigated as an efficient way to represent data in special purpose, since it allows for simple arithmetic circuits under certain conditions. In particular, LNS exploits the properties of the logarithm to reduce the basic arithmetic operations of multiplication, division, roots, and powers to binary addition, subtraction, and right and left shifts, respectively. In
addition to simplifying several operations, LNS provides efficient data representation because its round off error behaviour resembles that of floating-point arithmetic. In fact, LNS-based systems have been proposed that exhibit characteristics similar to 32- bit single-precision floatingpoint representation. The operations of addition and subtraction are rather awkward to perform in LNS as complex look-up tables (LUTs) or other approximation circuitries are needed. While for short word lengths simple techniques based on LUTs suffice, more elaborate approximation techniques are required for longer word lengths.

Need of the LNS MAC units in digital filter: If we done any multiplication operation you required the multiplier and adder operator, similar to division operation required the modals and substation operator, also similar to power element required multiple multiplication. Above mention all are consume more power, gates, area and reduce the speed and performance .in digital filter require the more multiplication, power, division operations. If we use the general method of multiplication, division, power its reduce the performance of digital filter. But if we use the LNS method in the digital filter its reduce the power, gates, area and increase the speed and performance. In LNS method simply done the addition and substation operation .Its required less power as compare to the multiplication.

Objectives of the project:

There are several objectives of this project which are:-

The logarithmic number system (LNS) is an efficient way to represent data in VLSI processors because its roundoff error behaviour resembles that of floating point arithmetic. LNS reduce the power dissipation in signalprocessing-related application such as hearing-aid devices, video processing and error control. LNS base and LNS word are the two design parameters exploited to minimize complexity.

II. LITERATURE SURVEY

1. "Efficient decimal MAC (Multiply Accumulate) architecture for high speed decimal processors based on IEEE 754-2008 Standard for Decimal Floating Point (DFP) Arithmetic."

Finding:

The design of high-speed and low-power VLSI architectures need efficient arithmetic processing units, which are optimized for the performance parameters, namely, speed and power consumption. Adders are the key components in general purpose microprocessors and digital signal processors. They also find use in many other functions such as subtraction, multiplication and division.

As a result, it is very pertinent that its performance augers well for their speed performance. Furthermore, for the applications such as the RISC processor design, where single cycle execution of instructions is the key measure of performance of the circuits, use of an efficient adder circuit becomes necessary, to realize efficient system performance.

Additionally, the area is an essential factor which is to be taken into account in the design of fast adders. Towards this end, high-speed, low power and area efficient addition and multiplication have always been a fundamental requirement of high-performance processors and systems.

Conclusion:

In this chapter, the study of low power, area efficient and high speed adders and multipliers developed by many researchers have been discussed in the literature. Also, the various techniques for reducing power and increasing efficiency for MAC unit have been presented. In this work the various adders and multipliers are analyzed and the optimized adder and multiplier are selected for designing the MAC unit. Then the Multiplier Adder combination is simulated and analyzed. From this analysis, for the selected MAC unit, pipelining technique has been introduced for further increasing speed and efficiency. Finally, the proposed MAC unit is implemented in FIR filter.

2. "An Enhanced Logarithmic Number System Adder / Subtractor for Low power DSP applications."

Finding:

In this paper we are contributing techniques for the Low power addition/subtraction of Logarithmic number system (LNS) on digital filters. In this the impact of portioning the lookup tables (LUT) required for addition/subtraction on complexity, performance is studied. Two design parameters are examined to minimize complexity, namely the LNS base and the organizations of the LNS word are taken into consideration. With LNS, multiplication and division operations reduce to simple addition and subtraction providing arithmetic over a wide dynamic range. In addition, techniques for the low-power implementation of an LNS multiply accumulate (MAC) units are examined. The results are stored in partitioned LUTs and obtained through Verilog code written in Xilinx. These are compared to linear fixed-point two's-complement equivalents.

Conclusion:

This paper successfully provides the design techniques and quantitative performance analysis of LNS MAC units and filter implementations, shows that LNS can offer aviable solution for low-power signal processing systems with moderate word length requirements. The gated clock technique has been used to further reduce power consumption performed to latched inputs due to the clock signal. Reduce of power dissipation also depends on the partitioning of LUTs and also it has been shown that the choice of number of sub-LUTs is an important design parameter that can be employed for exploration of the area, time, power design space.

3. "A 32-Bit Logarithmic Arithmetic Unit and Its Performance Compared to Floating-Point"

Finding:

As an alternative to floating-point, this paper proposed the use of a logarithmic number system, in which a real number is represented as a fixed-point logarithm. Multiplication and division therefore proceed in minimal time with no rounding error. However, the system can only offer an overall advantage if addition and subtraction can be performed with speed and accuracy at least equal to that of floating-point, but these operations require the interpolation of a non-linear function which has hitherto been either time consuming or inaccurate. this paper present a procedure by which additions and subtractions can be performed rapidly and accurately, and show that these operations are there by competitive with their floating-point equivalents. then show that the average performance of the logarithmic system exceeds floating-point, in terms of both speed and accuracy.

Conclusion:

Hitherto, LNS arithmetic devices had offered either better speed or better accuracy than FLP but not both. Alternatively they had been restricted to short word lengths.

We have now demonstrated that it is possible to design a 32-bit LNS arithmetic unit which will perform with substantially better speed and accuracy than FLP. The exact speed improvement depends on the ratio of adds to multiplies, but is about twofold at 40% to60%. The improvement in accuracy is harder to predict, as it depends also on the range of the operands, but is generally around twofold in simulated arithmetic kernels. A further advantage is that a LNS ALU requires the design of only one substantial piece of hardware, whereas the design of a FLP unit involves separate consideration of the adder, multiplier and divider. Algorithmic complexity is exploding in almost all areas of advanced computation, and a great many applications are now becoming bounded by the limits currently imposed by FLP execution. Examples include real-time applications such as the large class of RLS based algorithms and sub-space methods which will be required in broadcasting and cellular telephony; Kalman filtering and Riccati-like equations used in advanced real-time control; and graphics systems. Ways are urgently being sought to bypass this limitation by improving the speed at which the basic arithmetic operations can be performed. The results we have presented here suggest that a logarithmic arithmetic unit will offer a valuable means by which to achieve this objective.

Block Diagram-

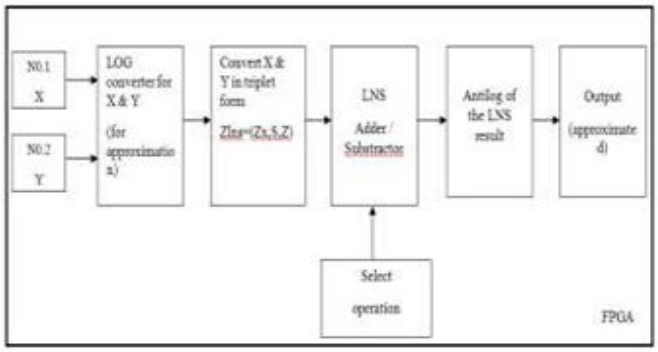

fig. system overview

1) Take the two number of n-bit is X and Y . X and Y is the input of the FPGA and select operation also input to FPGA, its 2-bit.
2) The select operation is use to select arithmetic operation like addition, subtraction, multiplication, and division.
3) Input X and Y convert into logarithmic form using verilog code.
4) The X and Y number convert into LNS triplet :
   xLNS = (zx ,sx ,x), yLNS = (zy ,sy ,y).
   Where zx is asserted in the case that X is zero, sx is the sign of X and x=log b(|X|), zy is asserted in the case thatY is zero, sy is the sign of Y and y=logb(|Y|),
5) According to the select operation input bit LNS adder / subtractor .Perform the operation and generate the result in the form of logarithmic .The multiplication of XLNS and YLNS is reduced to the computation of the triplet ZLNS.
   ZLNS = (zz, sz, z),
   Where zz = zx and zy, sz = sX xor sY, and z = x + y.
   Similarly, the case of division reduces to binary subtraction.
6) Take the antilog of logarithmic form result i.e ZLNS = (zz, sz, z), we get actual result of the multiplication of X and Y number.

III. ADVANTAGES AND APPLICATION

Advantages:

- A low-power design framework for LNS systems.
- The quantification of power dissipation reduction.
- Performance improvement made possible by using LNS, compared to equivalent binary implementations, the design space exploration using the number of LUTs For addition /subtraction as a parameter, for the case of using combinational logic for LUT implementation, and the extensions of SNR models in LNS for the case of.

Applications:

- LNS reduce the power dissipation in signal processing related application such as hearing aid devices, video processing and error control.
- In particular, LNS exploits the properties of the logarithm to reduce the basic arithmetic operations of multiplication, division, roots, and powers to binary addition, subtraction, and right and left shifts, respectively.
- The application of retiming is particularly useful in avoiding unnecessary switching activity, due to unbalanced delay paths in LNS arithmetic circuits.
- The area time- power design space of a low-pass finite impulse response (FIR) filter is explored for several configurations of MAC units.

IV. RESULT

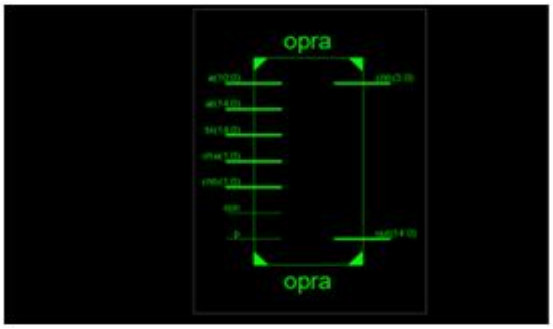

fig. sematic result

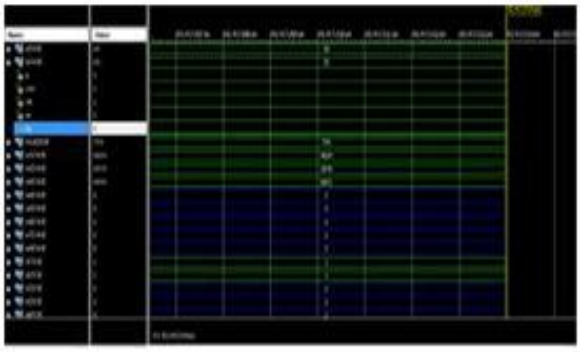

fig. simulation of lns mac

V. CONCLUSION

The logarithmic number system (LNS) is an efficient way to represent data in VLSI processors. In DSP application required the number of multiplication ,power, division operation .If we use the previous method for multiplication, power, division, its required more time ,gates ,power and also decrease performance of the operation .But if we use the LNS method for this multiplication, power, division it very useful because its required less gates, delay ,time and increase the performance of the operation as compare to previous method. In this project only done the simply add, sub operation. Because add ,sub. Operation less power ,and gate as compare to multiplication operation.

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