# A Comparative Study of Vedic Multiplier without and with Pipeline Technique

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***Abstract-*** *The algorithm of Vedic Mathematics relies on 16 sutras for the intention of simplification of long and bulky mathematics. Vedic mathematics describes several algorithms for the single operation. A variety of Vedic multiplication sutras like Urdhva tiryakbhyam, Nikhilam has been thoroughly discussed for arithmetic multiplication in Vedas. Out of the proposed 16 sutras the Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm), which produces minimum delay for multiplication of all types of numbers, either small or large. This Vedic mathematics improves the performance of the multiplier in terms of speed. By using this technique RTL coding for 4×4 Vedic multipliers with and without Pipelining can be done and implemented on hardware which will decrease the delay of the multiplier.*

***Keywords***- FPGA, Pipeline Technique, U-T Sutra, Vedic mathematics, Vedic multiplier.

## I. INTRODUCTION

The methods of Vedic mathematics are derived from four Vedas (books of wisdom). It is described in Sthapatya-Veda (a book written on civil engineering and architecture), which is an Upa-Veda (supplement) of Atharva Veda. The description of several recent mathematical expressions including arithmetic, factorization, geometry, quadratic equations, trigonometry and even calculus [9].

The Jagadguru Shree Shankaracharya Bharati Krishna Teerthaji Maharaja (1884 - 1960) comprised all this methods together and provided its mathematical clarification while discussing it for various purposes. Swahiji gave 16 sutras (formulae) and 16 Upa sutras (sub formulae) after broad study in Atharva Veda. Noticeably these formulae are not to be found in present content of Atharva Veda. The Vedic mathematics is not simply a mathematical wonder but also it is logical. That is why Vedic Mathematics has such an amount of distinction which cannot be disapproved. Vedic Mathematics can be applied for numerous basic as well as compound mathematical operations. The methods of basic arithmetic are extremely effortless and powerful.

The "Vedic" word came in existence from the "Vedas" which means the store-house of all knowledge. Vedic mathematics is primarily based on 16 Sutras (or aphorisms) dealing with a variety of branches of mathematics like arithmetic, algebra, geometry etc. The given Sutras along wih their concise meanings are given alphabetically [9].

1) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2) Chalana-Kalanabyham – Differences and Similarities.
3) Ekadhikina Purvena – By one more than the previous One.
4) Ekanyunena Purvena – By one less than the previous one.
5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6) Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7) Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
8) Paraavartya Yojayet – Transpose and adjust.
9) Puranapuranabyham – By the completion or noncompletion.
10) Sankalana- vyavakalanabhyam – By addition and by subtraction.
11) Shesanyankena Charamena – The remainders by the last digit.
12) Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13) Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14) Urdhva-tiryakbhyam – Vertically and crosswise.
15) Vyashtisamanstih – Part and Whole.
16) Yaavadunam – Whatever the extent of its deficiency.

## II. VEDIC MATHEMATICS

The proposed design of Vedic multiplier is based on the Vedic multiplication formulae (Sutras) of Vedic multiplication. These Sutras have been usually used for the multiplication of two numbers in the decimal number system. In this work, we adopt the same logic to the binary number system to make the proposed method compatible with the digital hardware [6] [7]. Vedic multiplication based on Vedic algorithms, some of them are discussed below:

**1. Urdhva Tiryakbhyam sutra**

The working of the multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. The general multiplication formula of Urdhva Tiryakbhyam Sutra is valid to the entire group of multiplication which is having meaning "Vertically and diagonally". It is a novel concept through which the generation of all partial products can be determined with the parallel addition of these partial products. The parallelism in generation of partial products and their sums is determined by using Urdhava Triyakbhyam [4]. This algorithm can be generalized for n x n bit number. The partial products and their sums are calculated in parallel, the multiplier is free from the clock frequency. Therefore the multiplier requires the same quantity of time to calculate the product and thus is independent of the clock frequency Even if a superior clock frequency results in increased processing power, its drawback is that it also increases the power dissipation that results in advanced device operating temperatures. By using the Because of its regular structure, it can be effortlessly layout in a silicon chip. Therefore this is time, power and space efficient. It is confirmed that this design is rather efficient with respect to the silicon area and speed [5] [7] [8].

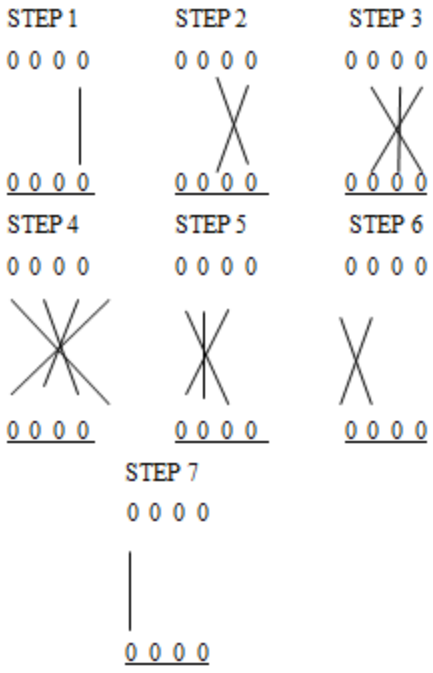


Fig. Vedic Multiplication

**III. PIPELINE TECHNIQUE**

The implementation performance is enhanced with pipeline technique when compared with sequential traditional execution. In a pipeline technique a job is divided into subtask and these subtasks are executed at the same time. In the design of Vedic multiplier the multiplier as well as multiplicand are subdivided and given to individual stages of pipeline technique [6]. At times smaller word length microprocessor only cannot calculate higher bit multiplication. For large scale calculation the pipeline technique is the finest way to perform faster operation. In the improved method a pipeline technique is integrated to carry the MSB of the operands. Usually the fundamental pipeline technique consists of latches and stages [9]. The stages are the logic elements, where computations are performed. The results of given calculated elements are provided to the next stages by latches. The operands those are left for computations in the next machine cycle are also feed forward through latches to next stages [9] [10].

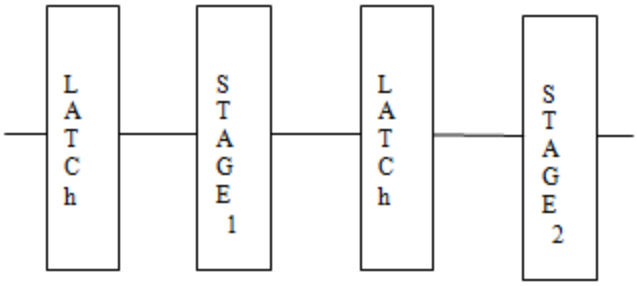


Fig. Pipeline Technique.

**III. COMPARATIVE RESULTS OF PROPOSED VEDIC MULTIPLIER WITH PIPELINE TECHNIQUEFOR MULTIPLIER UNIT**

To show the efficiency of proposed Vedic multiplier for Multiplier unit, it has been compared with other popular existing designs. The comparison has been made between Vedic multiplier without and with pipeline technique on the basis of area, delay and power.

In the following given table no. I the comparison has been made on the basis of total logic elements used. The Vedic multiplier with pipeline technique consists of greater area because of registers used in the hardware design in order to implement pipeline technique.

In the following given table no. II the comparison has been made on the basis of power in mW. The Vedic multiplier with pipeline technique consumes more power as compare to traditional design.

In the following given table no. III the comparison has been made on the basis of delay. The Vedic multiplier with pipeline technique comes out to be more faster than the traditional design. Pipeline technique improves the Vedic multiplier in terms of delay.

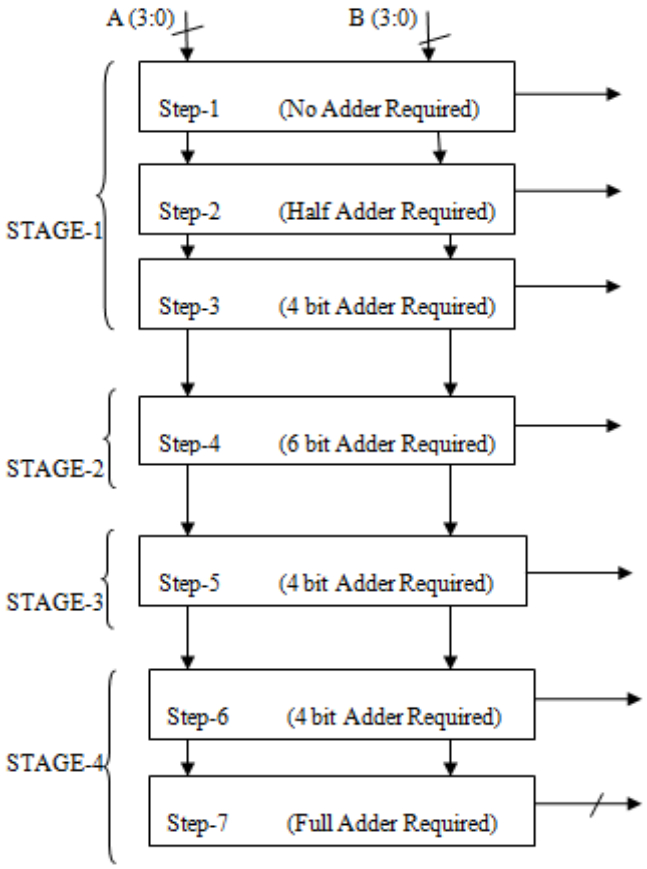


Fig. Pipeline Technique Stages

Table-I Delay Comparison Table

| Ref. No. | Target Device | Tech. (nm) | Delay (ns) | |
|---|---|---|---|---|
| | | | Vedic Mult. | Pipeline Vedic Mult. |
| [1] | Spartan | - | 13.228 | - |
| [2] | - | 180 | - | - |
| [3] | Xilinx VHDL | - | 5.352 | - |
| [4] | Cadence | 45 | 2.8 | 2.5 |
| [5] | Spartan | - | 3.073 | - |
| [6] | Cadence | 180 | 3.010 | 1.953 |
| [7] | Spartan | - | 4.545 | - |
| [8] | Spartan | - | 13.102 | - |

Table-II Area Comparison Table

| Ref. No. | Target Device | Tech. (nm) | Total Logic Elements | |
|---|---|---|---|---|
| | | | Vedic Mult. | Pipeline Vedic Mult. |
| [1] | Spartan | - | 16 slices, 30LUT | - |
| [2] | - | 180 | 56 No. of gates | - |
| [3] | Xilinx VHDL | - | - | - |
| [4] | Cadence | 45 | 47 | 59 |
| [5] | Spartan | - | 28 slices | - |
| [6] | Cadence | 180 | - | - |
| [7] | Spartan | - | 11 slices, 18LUT | - |
| [8] | Spartan | - | - | - |

Table-III Power Comparison Table

| Ref. No. | Target Device | Tech. (nm) | Power (mW) | |
|---|---|---|---|---|
| | | | Vedic Mult. | Pipeline Vedic Mult. |
| [1] | Spartan | - | - | - |
| [2] | - | 180 | 0.50427 | - |
| [3] | Xilinx VHDL | - | - | - |
| [4] | Cadence | 45 | 0.00496 | 0.005699 |
| [5] | Spartan | - | 57.81 | - |
| [6] | Cadence | 180 | - | - |
| [7] | Spartan | - | - | - |
| [8] | Spartan | - | - | - |

## IV. CONCLUSION

We have proposed a design for the NXN bit Multiplier Unit using a unique Vedic multiplier with pipeline technique which provides better results with respect to the conventional Vedic multiplier unit. This Proposed Multiplier Unit is very useful for designing the high speed digital signal processors, multipliers, MAC units and DSP units etc. The proposed design will be efficient in terms of delay that is the multiplier unit will have more speed than conventional multiplier unit.

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