Area and Delay Efficient Vedic Multiplier Using Pipeline Technique

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Abstract- *This paper describes the design and implementation of Area and Delay efficient Vedic Multiplier using Pipeline Technique. The hardware kit utilized for implementation is Altera FPGA model no. EP3C16F484C6 at 65 nm technology at 1.2 V. The implementation of Vedic Multiplier without and with Pipeline Technique on Altera Quartus II 9.0 at 65 nm technology at 1.2V has been done.*

Keywords- FPGA, Pipeline Technique, U-T Sutra, Vedic mathematics, Vedic multiplier

I. INTRODUCTION

Vedic Mathematics is one of the ancient methods for solving mathematics problem mentally. It is used to convert the tough calculations into simpler, orally manageable operation without much help of pen and paper. We can do mental calculations for very small numbers and hence it provides techniques to calculate the magnitude of large numbers easily. In Vedic mathematics several methods are given for basic operations like multiplication and division [1] [2].

Today's CPUs are processing fast on high frequencies with smaller size of Transistor. Arithmetic and Logic Unit - ALU is one of the most important and significant blocks in CPU. Hence it is vital to have fast and efficient ALU [3]. In today's computing technology functions like Sine and Cosine are also often vital and can be implemented in hardware. With these considerations, it is significant to have quick and well-organized method to design any complex mathematical functions [4] [5]. Vedic mathematics provides algorithms to simplify the mathematics and hence the methods provided by the Vedic Mathematics is ideal answer for the problem stated.

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The aim is to design and implementation of an area and power efficient fast multiplier by using pipeline approach with self testing, so that it can be used in any processor application. This paper deals with the study, design and implementation of Vedic multiplier without and with pipeline technique. In this work, study of Vedic multiplication algorithms has been explored without and with pipeline technique. Architecture of Vedic multiplier based on speed specification has been designed. We proposed first time the implementation of Vedic Multiplier without and with Pipeline Technique on Altera Quartus II 9.0 at 65 nm technology at 1.2V.

II. VEDIC MATHEMATICS

The proposed design of Vedic multiplier is based on the Vedic multiplication formulae (Sutras) of Vedic multiplication. These Sutras have been usually used for the multiplication of two numbers in the decimal number system. In this work, we adopt the same logic to the binary number system to make the proposed method compatible with the digital hardware [6] [7]. Vedic multiplication based on Vedic algorithms, some of them are discussed below:

1. Urdhva Tiryakbhyam sutra

The working of the multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. The general multiplication formula of Urdhva Tiryakbhyam Sutra is valid to the entire group of multiplication which is having meaning "Vertically and diagonally". It is a novel concept through which the generation of all partial products can be determined with the parallel addition of these partial products. The parallelism in generation of partial products and their sums is determined by using Urdhava Triyakbhyam [4]. This algorithm can be generalized for n x n bit number. The partial products and their sums are calculated in parallel, the multiplier is free from the clock frequency. Therefore the multiplier requires the same quantity of time to calculate the product and thus is independent of the clock frequency. The benefit of doing so is that it reduces the need of microprocessors to function at relatively high clock frequencies. Even if a superior clock frequency results in increased processing power, its drawback is that it also increases the power dissipation that results in advanced device operating temperatures. By using the Vedic multiplier, the designers of microprocessors can easily avoid these problems to keep away from catastrophic device failures.

The processing power of multiplier can be improved by increasing the input and output data bus widths as it has a quite a regular structure. Because of its regular structure, it can be effortlessly layout in a silicon chip. As the number of bits increases, gate delay and area increases very gradually as compared to other multipliers. Therefore this is time, power and space efficient. It is confirmed that this design is rather efficient with respect to the silicon area and speed [5] [7] [8].

III. PIPELINE TECHNIQUE

The implementation performance is enhanced with pipeline technique when compared with sequential traditional execution. In a pipeline technique a job is divided into subtask and these subtasks are executed at the same time. In the design of Vedic multiplier the multiplier as well as multiplicand are subdivided and given to individual stages of pipeline technique [6]. The parallel multiplier for example Vedic multiplier efficiently gives the results of a 4bit or 8bit multiplication on 8-bit processor. At times smaller word length microprocessor only cannot calculate higher bit multiplication. For large scale calculation the pipeline technique is the finest way to perform faster operation. In the improved method a pipeline technique is integrated to carry the MSB of the operands. Usually the fundamental pipeline technique consists of latches and stages [9]. The stages are the logic elements, where computations are performed. The results of given calculated elements are provided to the next stages by latches. The operands those are left for computations in the next machine cycle are also feed forward through latches to next stages [9] [10].

IV. IMPLEMENTED WORK

The proposed Arithmetic Module has first been split into three smaller modules, which are 1. 2X2 Vedic Multiplier Module 2. 4X4 Vedic Multiplier Module 3. 4X4 Vedic Multiplier Arithmetic module using Pipeline Technique. These modules have been made using Verilog HDL.

The implementation of first Vedic Multiplier is based on a unique method of digital multiplication which is somewhat different from the usual method of multiplication like adding and shifting where smaller blocks are used to form the bigger blocks. The Vedic Multiplier by using Urdhva Tiryakbhyam Sutra is designed in Verilog HDL, as its give effective & efficient use of structural method of modelling. The individual block is implemented using Verilog hardware description language. The functionality of each block is verified by using simulation software Altera Quartus II 9.0.

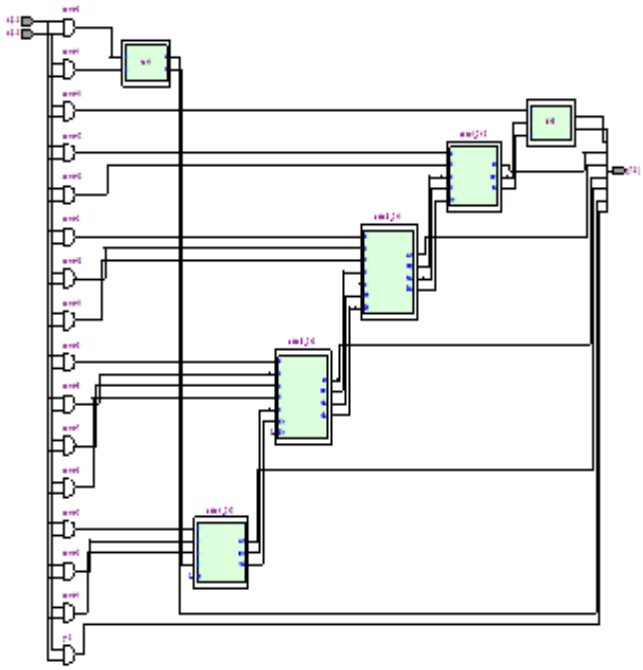

Fig. RTL view of 4X4 Vedic Multiplier

While the implementation of the second multiplier with pipeline technique will be done by using number of stages which will enhance the speed further but also it has increased the core area, but the delay has been decreased when compared with the previous design which was not implemented by using pipeline technique.

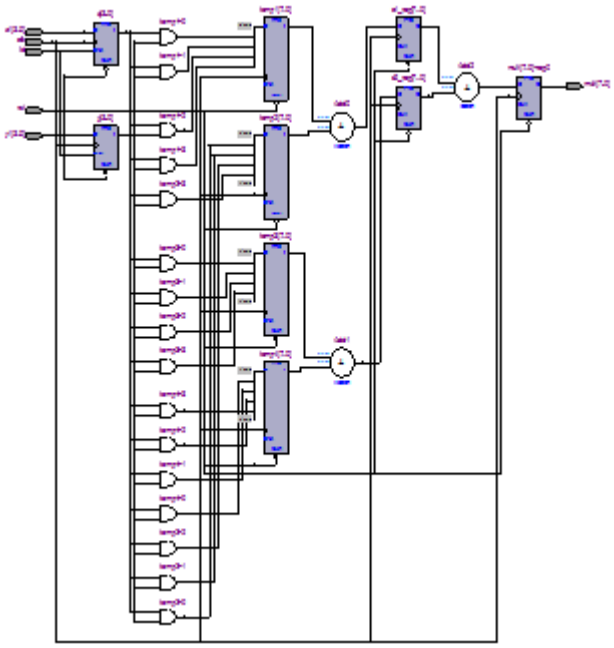

Fig. RTL view of 4X4 Vedic Multiplier using Pipeline Technique

The RTL Schematic for both pipelined and without pipelined architecture are obtained using Altera Quartus II 9.0.

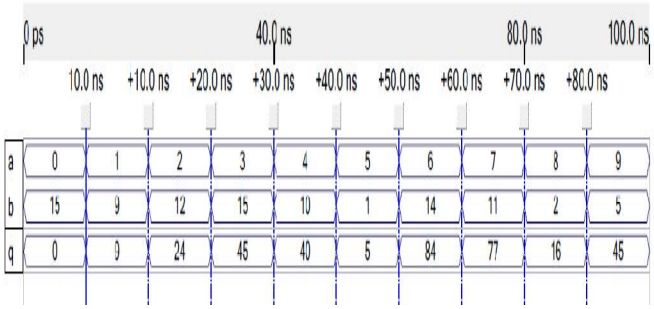

Fig Simulation results for 4X4 Vedic Multiplier

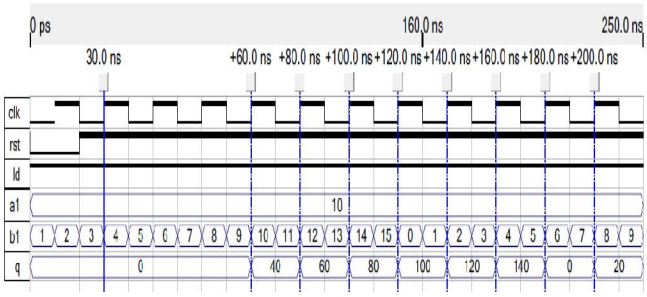

Fig. Simulation results for 4X4 Vedic Multiplier using Pipeline Technique

TABLE I
Comparison of Synthesis Results for 65 nm Technology

FPGA Device Package	Type of Multiplier	Total Logic Elements	Delay (ns)	Speed (MHz)	Power (mW)
Altera Quartus II 9.0	VEDIC MULT. 4X4	33	12.0	82.5	65.47
	VEDIC MULT. USING PIPELINE TECHNIQUE 4X4	44	2.3	422.1	187.5

The power analysis, timing, area report have performed in Altera Quartus II 9.0 at 65 nm technology at 1.2 V.

V. CONCLUSION

The designs of 4x4 bits Vedic multiplier without & with pipeline technique have been implemented on Altera Quartus II 9.0 device. The computation delay for 4x4 bits Vedic Multiplier (UT) was 12.108 ns and for 4x4 bits Vedic Multiplier using pipeline technique was 2.369 ns. It is therefore seen that the Vedic multipliers with pipeline technique are much faster than the conventional Vedic Multipliers. Udrhva Tiryakbhayam Sutra of Vedic Multiplier is highly efficient algorithm for multiplication. The algorithms of Udrhva Tiryakbhayam Sutra become even more efficient if it is used by implementing Pipeline technique.

The proposed Vedic Multipliers without and with Pipeline technique have found to be area and delay efficient as compare to previous designs while the design is suffering in terms of power dissipation. The Vedic Multiplier without Pipeline Technique results in area and power saving by 25% and 65.08% respectively while the Vedic Multiplier with Pipeline Technique results in delay savings by 80.28%

Definitely Vedic Multiplier approach becomes faster if it is designed by using Pipeline Technique but the area and power dissipation will become more. Thus it will be fast and time efficient design while suffering from factors like power and size.

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