# Performance Analysis of H.264 Video Decoder on TI DSP Processor

**Imran Ullah Khan[1], Mohd Javed Khan[2]**
[1, 2] Department of Electronics & Communication Engineering
[1, 2] Integral University Lucknow, India

***Abstract-*** *The H.264 is developed by the ITU-T ISO/IEC Joint Video Team (JVT) and is projected to become a standard in the year 2003. H.264/AVC (Advanced Video Coding) is the newest video coding standard of the moving video coding experts group. Although the technical content of the standard is mature, there is still ongoing development, and this paper refers to the reference software joint model 4.2(JM-4.2).[2] The H.264 standard is designed in two distinct layers Video Coding Layer(VCL) and a Network Abstraction Layer(NAL).The decoder is standardized by imposing restrictions on the bit stream and syntax, and defining the process of decoding syntax elements such that every decoder conforming to the standard will produce similar output when encoded bit stream is provided as input. It uses state of art coding tools and provides enhanced coding efficiency for a wide range of applications, including video telephony, real-time video conferencing, direct-broadcast TV (television), blue-ray disc, DVB (Digital video broadcast) broadcast, streaming video and others. The paper proposes to port the H.264/AVC decoder on the TI DSP (Digital signal processor). The paper proposes to investigate the decoder performance on different video quality measures.*

***Keywords-*** Mean square error, TI DSP, macro blocks, codec, Intra Prediction

## I. INTRODUCTION

Digital video compression techniques have played a key role in recent multimedia communications. The limitation of bandwidth in communication channels and storage media demands more efficient video coding methods. Introducing new applications and advances in multimedia technology demands video coding methods to include more complex and advanced features. Compression is the process of compacting data into a smaller number of bits. Video compression (video coding) is the process of compacting or condensing a digital video sequence into a smaller number of bits. Compression involves a complementary pair of systems, a compressor (encoder) and a decompressor (decoder). The encoder converts the source data into a compressed form (occupying a reduced number of bits) prior to transmission or storage and the decoder converts the compressed form back into a representation of the original video data. The encoder/decoder pair is often described as a CODEC (enCOder/ DECoder). H.264 decoder complexity is higher on the encoder side and on the decoder side, the complexity is estimated to be two to three times higher than an H.263 decoder for the same bit rate [4]. Several studies examined H.264/AVC decoder performance on a general purpose processor [1]-[4]. The paper describes a comparative work which examines H.264/AVC decoder performance on three processors.

A baseline profile version is used for experimentation and the purpose of the paper is to examine the performance in terms of video quality measurements on different processors. The paper also investigates the performance of the decoder on different processors with and without the use of deblocking filter.

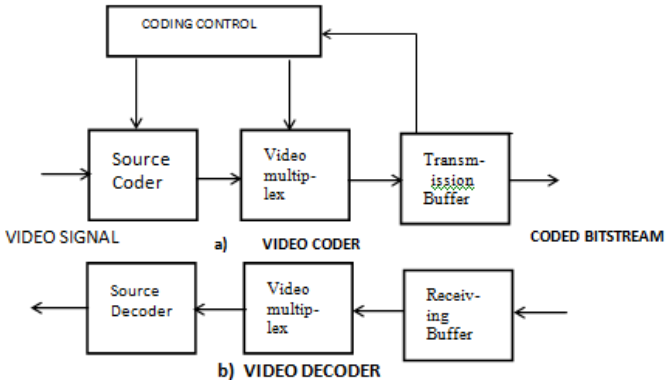


Figure-1: Outline block diagram of the Codec

## II. OVERVIEW OF H.264 DECODER

The decoder receives a compressed bit stream from the NAL (network abstraction layer). The data elements are entropy decoded and reordered to produce a set of quantized coefficients. These are rescaled and inverse transformed and using the header information decoded from the bit stream, the decoder creates a prediction macro block identical to the original prediction formed in the encoder.

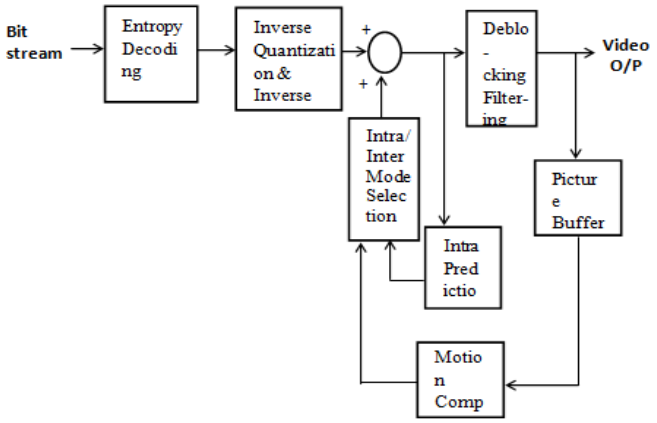


Figure 2: Block diagram of H.264 Decoder

## III. OVERVIEW OF THE PROCESSOR

The TMS320C64x DSPs (including the TMS320DM642 device) are the highest-performance fixed-point DSP generation in the TMS320C6000 DSP platform. The TMS320DM642 (DM642) device is based on the second-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture (VelociTI.2™) developed by Texas Instruments (TI), making these DSPs an excellent choice for digital media applications. The C64x™ is a code-compatible member of the C6000™ DSP platform.With performance of up to 5760 million instructions per second (MIPS) at a clock rate of 720 MHz, the DM642 device offers cost-effective solutions to high-performance DSP programming challenges. The DM642 DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. High-Performance Digital Media Processor (TMS320DM642) 2, 1.67, 1.39-ns Instruction Cycle Time .500, 600, 720-MHz Clock Rate. Eight 32-Bit Instructions/Cycle,4000, 4800, 5760 MIPS.Fully Software-Compatible With C64x™.VelociTI.2™ Extensions to VelociTI™ Advanced Very-Long-Instruction-Word VLIW)

TMS320C64x™ DSP Core. Eight Highly Independent Functional Units With VelociTI.2™ Extensions: Six ALUs (32-/40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle. Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle. Load-Store Architecture With Non-Aligned Support.

## IV. COMPARISON PARAMETERS

The H.264 decoder is implemented on the different processors and comparison is done based on different parameters. The parameters considered for comparison are MSE, PSNR.

1. **PSNR:** Peak Signal to Noise Ratio (PSNR) is measured on a logarithmic scale and depends on the mean squared error (MSE) of between an original and an impaired image or video frame.

$$PSNR = 10\log_{10}(\frac{255}{MSE})^2 = 20\log_{10}(\frac{255}{MSE})(\ for\ each\ Y,U,V)$$

Where MSE is Mean square error

**MSE:** The Mean Square Error measures the difference between the frames which is usually applied to Human Visual System. It is based on pixel-pixel comparison of the image frames.

$$MSE = \frac{1}{XY}\sum_{x=1}^{X}\sum_{y=1}^{Y}[i(x,y) - e(x,y)]^2$$

Where i(x,y) = intensity of input pixel(for each Y,U,V)
e(x,y) = intensity of output pixel(for each Y,U,V)

## IV. IMPLEMENTATION DETAILS

The H.264 decoder is implemented on TI DSP TMS320 DM642 operating at 600 MHz. The different video inputs are considered for the experimentation. The experimentation is done with and without deblocking filter. The sample result is displayed for further discussion.

Sequence title : Foreman
Resolution : 176x144
Number of frames : 150
Color space : YUV 4:2:0
Frames per Second : 30
Source : Uncompressed progressive

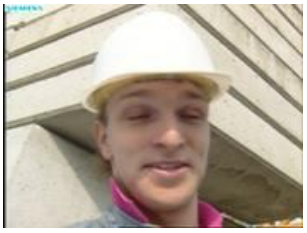

Figure 3: Snapshot of “Foreman” video sequence, frame 30

Sequence title : Salesman
Resolution : 176x144
Number of frames : 150
Color space : YUV 4:2:0
Frames per Second : 30
Source : Uncompressed progressive

Figure 4: Snapshot of "Salesman" video sequence, frame 20

| Frame No. | MSE for Video sequence Foreman | MSE for Video sequence Salesman | PSNR for Video sequence Foreman | PSNR for Video sequence Salesman |
|---|---|---|---|---|
| 1 | 1.75 | 1.81 | 43.2 | 42.8 |
| 10 | 1.78 | 1.83 | 42.9 | 42.8 |
| 20 | 1.94 | 1.96 | 42.3 | 42.2 |
| 30 | 2.19 | 2.23 | 41.1 | 40.8 |
| 40 | 2.4 | 2.46 | 40.6 | 40.2 |
| 50 | 2.6 | 2.68 | 40.1 | 39.4 |
| 60 | 2.74 | 2.82 | 39.5 | 39 |
| 70 | 2.87 | 2.91 | 39 | 38.8 |
| 80 | 2.95 | 2.99 | 38.9 | 38.6 |
| 90 | 3.03 | 3.06 | 38.5 | 38.4 |
| 100 | 3.1 | 3.15 | 38.2 | 38 |

Table-1:Video quality measures of H.264 decoder on TI DSP processor for various encoded streams

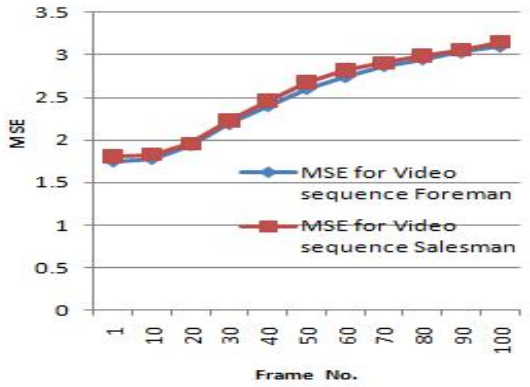


Figure 5: (a) MSE Plot

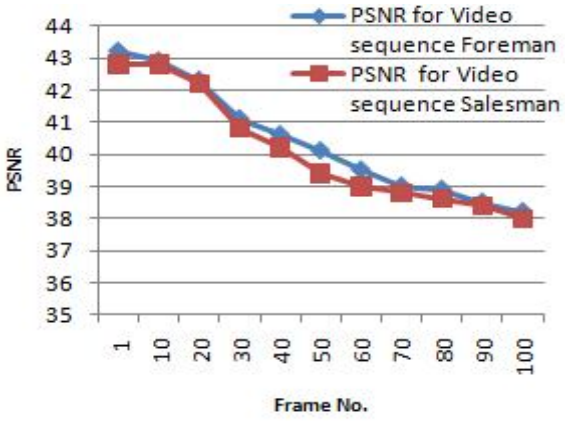


Figure 5: (b) PSNR Plot

## VI. CONCLUSIONS

The H.264 decoder is implemented on TMS320DM642 processor. PSNR and MSE are calculated for the different video sequences on the processors. It is observed TI DSP performs better than the other processors for implementing H.264 decoder without deblocking filter than any other processors. Also the decoding time for TI processor is less compared to other processors

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