A Novel 4-Bit Full Adder Design for Power and Area Optimization

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Abstract- *In the modern era, power dissipation and area of the circuit under fabrication has become a major and vital constraint in the electronic industry. The objective of this paper is to reduce the power dissipation in the circuit by using gate diffusion input technique. The purpose of this paper is to design and implementation of Full Adder circuit using Gate Diffusion Input (GDI) which is area optimized techniques. GDI technique reduces average power consumption and number of transistor than CMOS transistor. The simulation tool used is TANNER EDA 15.0 using 180nm technology with 1.8V as a supply voltage.*

Keywords- Gate Diffusion Input, Full Adder, Half Adder

I. INTRODUCTION

In VLSI addition is a basic arithmetic operation. Their applications are in digital signal processing architecture and also in microprocessor. Area and power are the most important factor in electronics for high performance in portable device. Continues increase of VLSI technology power consumption is an important factor in creation of very large scale integration. For longer life of portable devices designers are forced to create low power consumption, small area and reduced delay in circuit and more reliable electronic circuit. In VLSI the high speed and reduced surface area of silicon can be designed with different combination of logic. The Full adder circuit is a fundamental block arithmetic circuit as it used in comparator, ALU ,Multipliers etc. reduction in delay and power consumption in full adder will leads to directly reductionin Comparator, multipliers etc. too Increasing demand for battery operated applications; power consumption is a very important factor.

1.1 Gate Diffusion Input Technique

Morgenshtein has proposed basic GDI cell for low power digital combination circuit this is the new approach which is shown in fig1.GDI cell provide in-cell swing restoration under certain operating condition basically GDI is a two transistor implementation of complex logic function. This approach leads to reduction in power consumption, propagation delay and area of digital circuits is obtained while having low complexity of logic design. Source of the PMOS in a GDI cell is not connected to VDD it is an important feature of a GDI cell and GND is not connected to source of NMOS. hence GDI cell gives two extra input pins for input which makes the GDI design more flexible as the input can connect to any terminal.

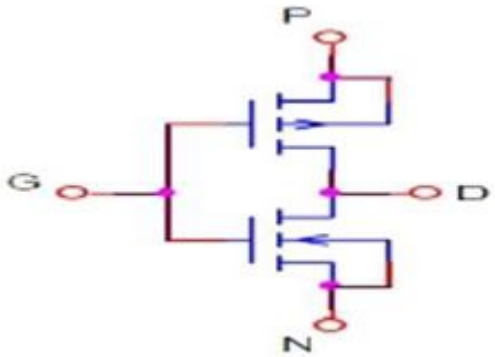

Fig. 1 Basic GDI Cell

There are three inputs in a GDI cell - G which is common gate input of NMOS and PMOS, P as a input to the source/drain of PMOS and N as a input to the source/drain of NMOS. Bulks of NMOS connected to N and bulk of PMOS is connected to P. Table 1 shows different logic functions implemented by GDI logic based on different input values. So, various logic functions can be implemented with less power and high speed with GDI technique as compared to conventional CMOS design.

S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F_1
2.	B	1	A	A'+B	F_2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

Table 1 Basic Function of GDI Cell

From table 1 most of the fundamental circuits can be made.

II. IMPLEMENTATION

The basic GDI cell for 180nm is shown in Fig2. This circuit is similar to the invertor but P and N terminals are not connected with VDD and Ground terminal always. When Vdd and Ground terminals are connected to P and N respectively it act as a normal invertor but its bulk is connected .result where obtained while GDI act as a invertor.

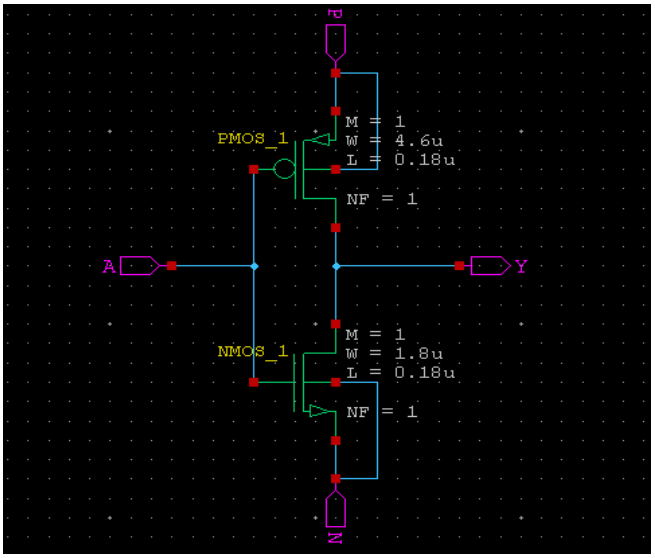

Fig.2 GDI Cell

For 180nm technology the parameter selected for PMOS and NMOS are 4.6um and 1.8um respectively. Test made on 1.8v supply voltage

Simulated Output GDI CELL:-

Avg. Power- 35.19nw
Delay- 0.2ns
Number of Transistor - 2

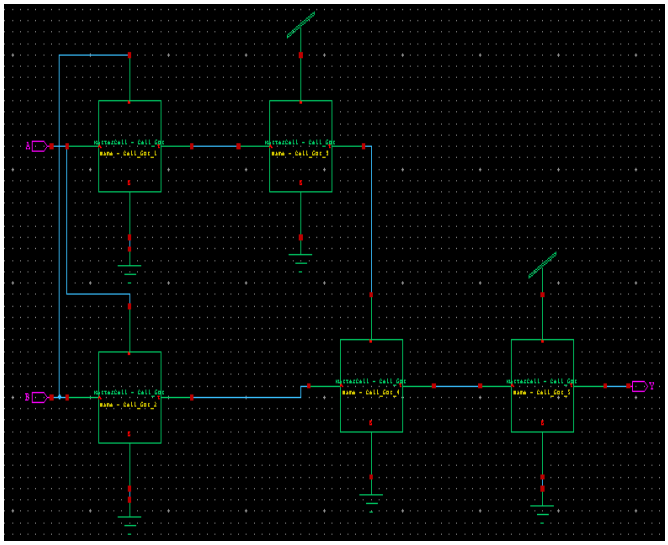

Fig.3 XOR Gate Using F1 Function

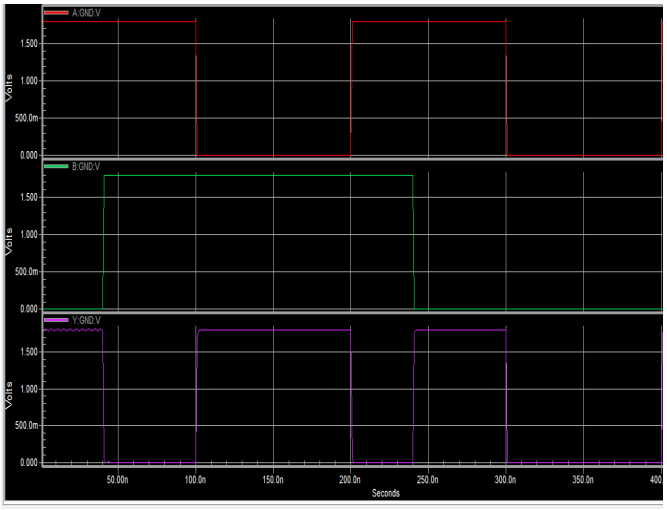

Fig.4 W-EDIT of XOR Gate

EXOR function is the key variable in adder equations. If the generation of them is optimized, this could greatly enhance the performance of the full adder cell. The GDI EXOR gate requires only 10 transistors by using F1 function shown in fig. 3. The propose GDI EXOR gate use less transistor when compared with CMOS counterpart. Input voltage is given as 1.8V. W-Edit of GDI EXOR Gate is shown in Fig 4.

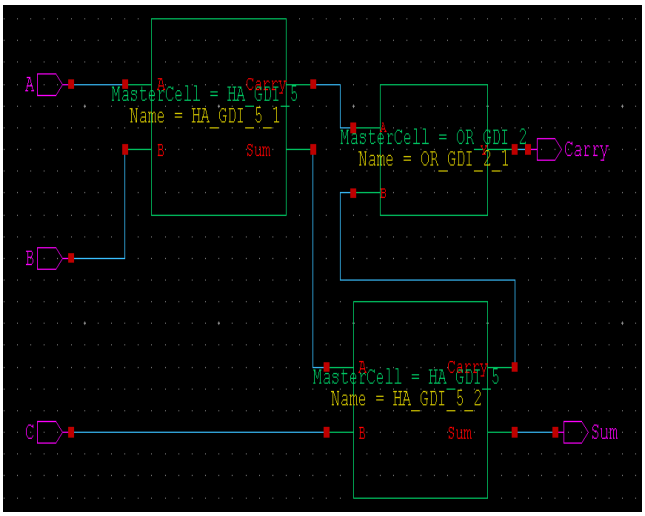

Fig.5 1-Bit Full Adder By GDI

The transistor level implementation of GDI Full Adder using 34 transistors is shown in Fig 5. We propose a Novel Full Adder using 34 Transistors. This full adder consists of two modules one half adder anda OR Gate both are implemented by F1 function of GDI technique. These Full adders use fewer transistors when compared with CMOS counterpart. Due to the advantages of GDI cell, less transistor count this circuit can achieve its benefit of low power consumption. GDI Full Adder is shown in Fig 5. The W-EDIT of GDI Full Adder is shown in Fig 6

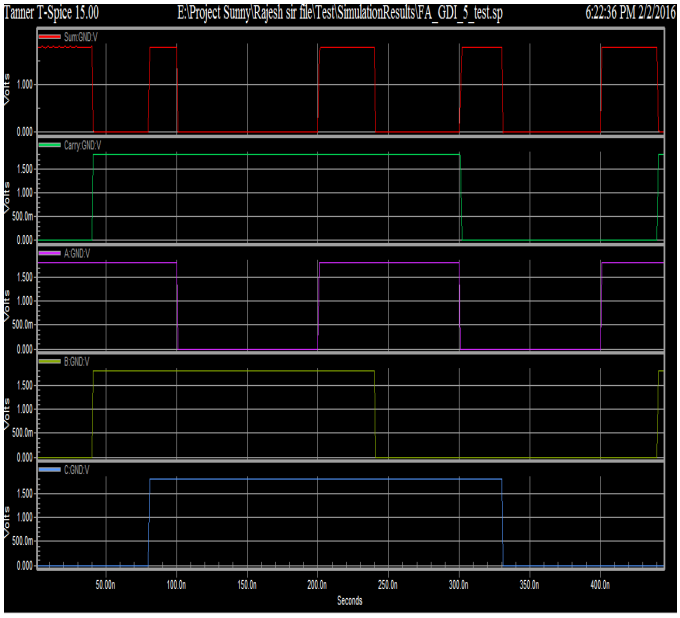

Fig.6 W-EDIT for 1-BIT Full Adder By GDI

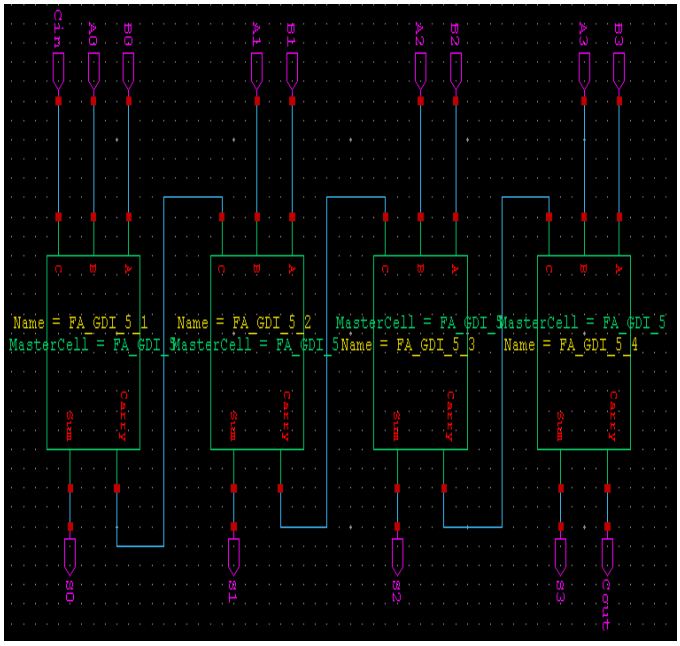

Fig.7 4-Bit Full Adder

Fig. 7 Shown the cascaded formation of 1-bit FA and it act as a 4-bit Full Adder in which A0,A1,A2,A3, B0,B1,B2,B3 and Cin are the input signals to the circuit which are taken as a bit format.

Also the S0, S1, S2, S3 are the output as a sum in Full adder and Cout as a Carry in the circuit.

SUM = (A) XOR (B) XOR (Cin)

CARRY = AB+BC+ACin

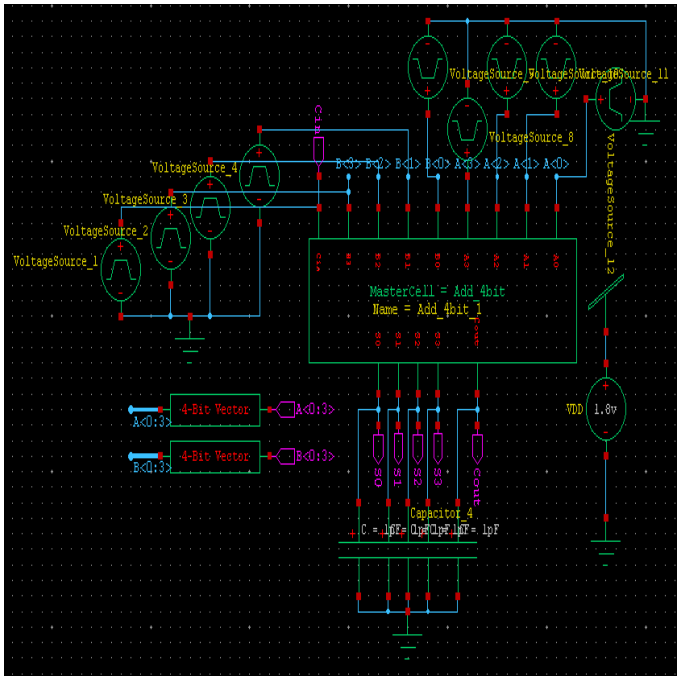

Fig.8 4-Bit Full Adder Test

Fig. 8 shows the test vector for the 4bit FA where inputs are access to the circuit and output obtained as SUM (4-bit) and Cout.

Fig. 9 shows W-edit of the test where 4-bit are given as a input. All parameters are shown in table 2 and 3 for comparative study with conventional CMOS design and GDI design.

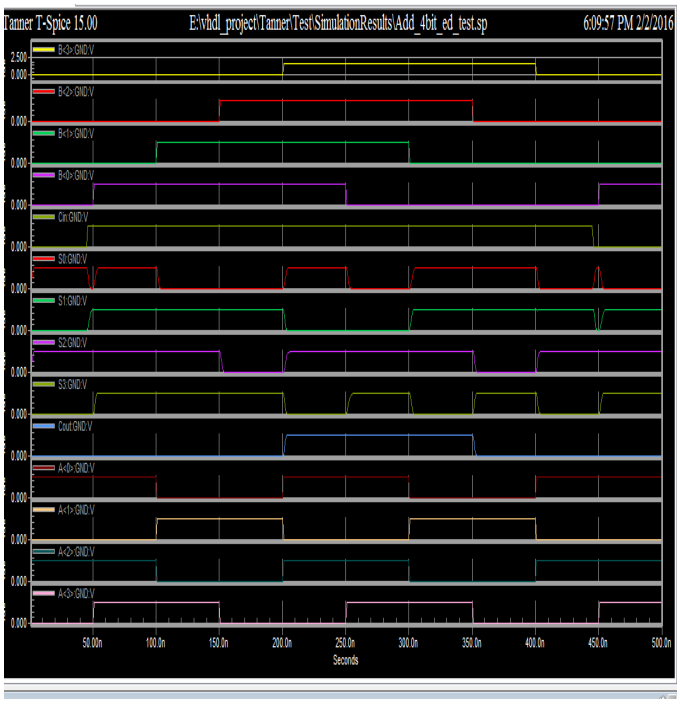

Fig.9 W-edit 4-Bit Full Adder

S. NO.	DESIGN TYPE	AVG POWER (µ W)	NO. OF TRANSISTOR
1.	CMOS	16.67 µ W	58
2.	PASS TRANSISTOR GATE	11.99 µ W	24
3.	PRAPOSED GDI DESIGN	4.23 µ W	34

TABLE 2. FOR 1-Bit Full Adder

S. NO.	DESIGN TYPE	AVG POWER (µ W)	NO. OF TRANSISTOR
1.	CMOS	178.968µ W	232
2.	PRAPOSED GDI DESIGN	153.886µW	56

TABLE 3. FOR 4-Bit Full Adder

III. CONCLUSION

Power consumption in modern devices are a growing concern on demand for increased battery life , lower heat dissipation and increased device reliability is on the rise. In this paper the power optimization at architecture level is demonstrated by design of 4-bit Full Adder using GDI technique. Also reduction number of transistor automatically leads to minimum possible area of the circuit i.e. reduced surface area of silicon.GDI proves that it have better result in terms of performance characteristics.

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