Modeling and Analysis of Current Source Multilevel Inverter using PI Controllers with Multicarrier PWM Technique

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Abstract- *Multilevel inverters are most familiar with power converter's applications due to reduced dv/dt, di/dt stress, very efficient for reducing harmonic distortion in the output voltage and output current, lower switch ratings, lower electromagnetic interference and higher DC link voltages used for high-voltage and high-power applications. This paper presents the modeling and analysis of nine-level current source multilevel inverter using proportional integral (PI) controllers with multicarrier pulse width modulation (PWM) control technique. The nine-level current source multilevel inverter with single rating inductor topology under symmetrical and asymmetrical modes of operation using PI controllers with multicarrier PWM control is proposed. This single rating inverter topology with reduced switching components is proposed to improve the multilevel inverter performance and the overall cost and circuit complexity are greatly reduced. The effectiveness of the proposed system is proved with the help of simulation. The simulation is performed in MATLAB/Simulink. From the simulation results, it shows that the proposed multilevel inverter works properly to generate the multilevel output waveform with minimum number of semiconductor devices and to achieve high dynamic performance with low total harmonic distortion (THD).*

Keywords- Multilevel Inverter (MLI), Current Source Inverter, Pulse Width Modulation (PWM), Proportional Integral (PI) Controller, Total Harmonic Distortion (THD).

I. INTRODUCTION

Today, the energy demand is moving on increasing toward generating power with renewable energy source that may be dispersed in a wide area, and most of them are renewable, as they have greater advantages due to their environmentally friendly nature. Photovoltaic (PV) energy has augmented interest in wide range of electrical power applications, since it is considered as a basically limitless and generally on hand energy resource with the focus on greener sources of power particularly for distant locations where utility power is engaged [1-4]. The solar can be used by all in universe which doesn't need more investigations of producing electricity [5-7]. This leads to research in multilevel inverters.

The multilevel inverters are classified into three types namely: (i) Diode clamped multilevel inverters; (ii) Flying capacitor multilevel inverter; and (iii) Cascaded H bridge multilevel inverter. Of these the cascaded H bridge multilevel inverter topologies give better results. The research goes on increasing to propose a new structure of inverter with reduced semiconductor devices with increased multilevel at the output waveform [8-9]. The study of the multi sampled multilevel inverters and their control techniques to improve the performance of the multilevel inverters. This also deals with the different control techniques to be implemented in multilevel inverters in order to reduce the THD. But they don't concentrate on the structure of the multilevel inverters [10-11]. A way to balance the capacitor voltage to produce voltage levels of equal width. Therefore the THD is reduced. There is no change in the structure of the inverter. Only the technique has been implemented with conventional structure but they achieved better THD [12-13]. The new algorithm for producing the switching signals. Here they propose BEE algorithm to produce the modulation signals; the algorithm works better than the other techniques but the structure of cascaded multilevel inverter remains same. Hence the switching loss is more and the number of switches used is same as that of the conventional one. Therefore it is necessary to find the new structural way of producing multilevel with reduced semiconductor devices [14].

The cascaded H bridge topology to be used, to reduce THD and the multilevel inverter fed multiphase induction motor; here they use diode clamped inverter to produce multiple levels at the output and they are used to drive the five phase motor. The performance analysis is done using this. Since they use diode clamped multilevel inverter the number of semiconductor devices is high and hence the losses are heavy. On replacing it with a new structure and by increasing the number of levels can improve the performance of the system [15-16]. The closed loop control strategy implemented in multilevel inverter is explained and the control circuit is also big which again increases the circuit complexity thus reducing the effectiveness of the proposed system [17-18].

Current source inverters with pulse width modulation strategies are employed to deliver a minimum distorted input and output waveforms. This inverter circuit is the double cascaded H-bridge multilevel current source inverter. Tragically, the need for isolated DC sources, power devices, and their gating circuits are a few issues of this inverter circuit. The multilevel current source inverters topology utilizing H-bridge and inductor-cell and this topology streamlines the necessity of isolated DC sources in the parallel H-bridge multilevel current source inverters is explained in [19]. An alternate circuit design of multilevel current source inverters is made by using a multi-cell arrangement of multilevel current source inverters [20-22], which is the double flying capacitor multilevel voltage source inverter. Various control, strategies have been exhibited to control the voltage at intermediate levels and highlighted in [23-25]. However, the inverter still requires expensive larger size middle inductors. These inductors will result in more losses in the inverter circuits and the inverter circuits will have lower efficiency.

From all the above analysis, conclude that the researches have been done on the control circuitry of the current source multilevel inverter is shown in Fig.1. But the structure of inverter remains same. On increasing the levels the structure becomes more complex and bigger in size reducing the efficiency of the system. Here propose a new structural current source multilevel inverter to produce multiple levels at the output voltage with minimum number of power semiconductor devices. The multi carrier PWM has also been implemented. Hence the THD is reduced lot with minimum number of devices with low switching noise.

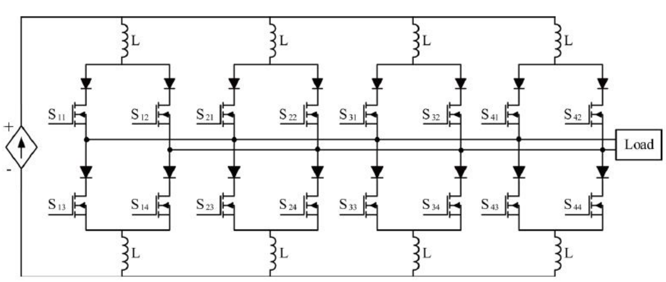

Fig. 1 Nine-level current source multilevel inverter symmetrical topology

II. CURRENT SOURCE MULTILEVEL INVERTER TOPOLOGY

A current source inverter converts the input DC to an AC at its output terminals. In these inverters, the input voltage is kept constant, and the amplitude of output voltage does not depend on the load. Nevertheless, the wave form of load current, as well as its magnitude, depends on the nature of the load impedance. In this inverter, the input current is constant, but adjustable. The amplitude of output current from current source inverter is independent of the load. A DC source supplies current source inverter. In an adjustable speed drive, DC source is usually an AC/DC rectifier with a large inductor to provide stable current supply. Usually, a current source inverter has a boost operation function and its output voltage peak value can be higher than the DC-link voltage.

III. SYMMETRICAL TYPE-NINE-LEVEL CURRENT SOURCE INVERTER TOPOLOGY

The power circuit of the nine-level single rating inductor type symmetrical current source inverter is shown in Fig.1. From this figure, it is observed that the circuit model is obtained by connecting four H-bridge unidirectional controlled power devices, and a DC source with equal inductors L.

The DC module is working with different intermediate levels for nine-level output waveform generation. All DC sources connected at the common point and due to this the isolated DC sources are no longer necessary in the circuit. The switching sequences of nine-level, single rating inductor type symmetrical current source inverter are shown in Fig.2. The switching sequences show the current level generation of positive, negative and zero level of +I, +2I, +3I, +4I, −I, −2I, −3I, −4I and 0 respectively.

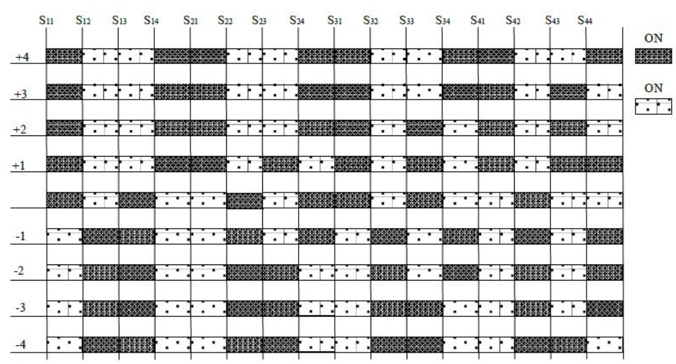

Fig. 2 Switching-sequence of symmetrical nine-level current source multilevel inverter

IV. ASYMMETRICAL TYPE-NINE-LEVEL CURRENT SOURCE INVERTER TOPOLOGY

The power circuit of the nine-level single rating inductor asymmetrical current source inverter is shown in Fig.3. The switching sequences of nine-level single rating inductor asymmetrical current source inverter shown in Table 1.

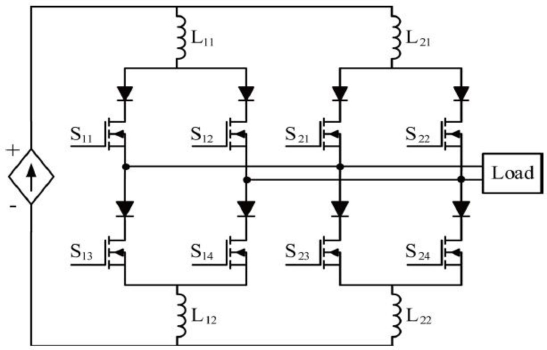

Fig. 3 Proposed nine-level current source multilevel inverter asymmetrical topology

Table 1 Switching-sequence of asymmetrical nine-level current source multilevel inverter

Levels	*Switching States*							
	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}
+4	1	0	0	1	1	0	0	1
+3	1	0	1	0	1	0	0	1
+2	0	1	1	0	1	0	0	1
+1	1	0	0	1	1	0	1	0
0	1	0	1	0	0	1	0	1
-1	0	1	1	0	0	1	0	1
-2	1	0	0	1	0	1	1	0
-3	0	1	0	1	0	1	1	0
-4	0	1	1	0	0	1	1	0

From Fig.3, it is observed that the circuit model is obtained by connecting two H-bridge, unidirectional controlled power devices and a DC source with inductors. It is implemented using the power circuit consists of eight IGBT switches and two pairs of inductors of L_{11} and L_{12} whose values are *300 mH* and L_{21} and L_{22} are *100 mH* with a common current source. The switching sequence shows the symmetrical nine-level current generations with addition and subtraction process of inverter (active level) are. *+I (I + 0)*, *+2I (3I − I)*, *+3I (3I + 0)*, *+4I (3I + I)*, negative level *−I (−I + 0)*, *−2I (−3I + I)*, *−3I (−3I+ 0)*, *−4I (−3I − I)* and *0* respectively.

V. MULTICARRIER PULSE WIDTH MODULATION CONTROL TECHNIQUE

In the proposed current source inverter topology, a level based multicarrier PWM strategy implemented for firing the gate terminals of the MOSFET switches to obtain the current waveform of nine-level current source inverter. Multicarrier PWM strategy is a comparison of a reference waveform, with vertically shifted carrier signals.

In multicarrier PWM technique, *(n−1)* triangular carriers are used for *n*-level inverter output voltage or current. In this proposed topology, eight triangular carriers are preferred. In phase opposition disposition, the carriers above the Sinusoidal reference zero points are 180 degree out of phase with those below the zero point.
Fig. 4 shows the gate pulse generation of proposed current source inverter with phase opposition disposition strategy with sine reference of modulation index *mi=0.9* and the carrier frequency of *2 kHz*.

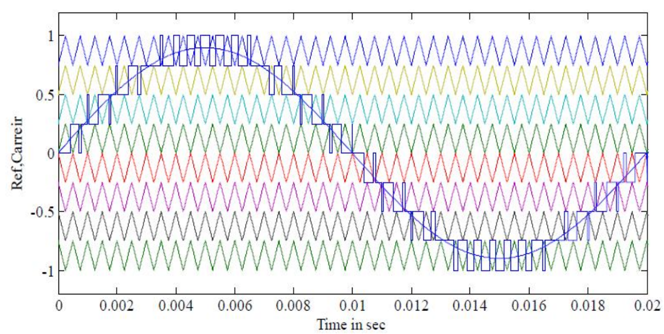

Fig. 4 Proposed nine-level current source multilevel inverter PWM control

The carrier waveforms have same amplitude *Ac* and frequency *fc*. Similarly, the reference waveforms have frequency f_{ref} and amplitude A_{ref}. At every instant, the response of the comparator is decoded to generate the correct switching sequences with respect to the output of the inverter.
The frequency modulation index *(mf)* is calculated in Eqn. (1).

$$m_f = (f_c / fr_{ef}) \quad (1)$$

The amplitude modulation index *(mi)* is calculated in Eqn. (2).

$$m_i = [\, A_{ref} / ((n-1)A_c) \,] \quad (2)$$

In the level shifted multicarrier PWM, phase opposite disposition strategy is used.

VI. SIMULATION RESULS AND DISCUSSION

The Simulink representation of nine-level single rating inductor type symmetrical current source inverter is implemented and this power circuit consists of sixteen IGBT switches and eight identical inductors with rating of 100 *mH* with a common current source generated from PV array. The current source is shared by the four H-bridge inverter with suitable switching sequences generates the nine-level output. Multi carrier pulse width modulation is tuned with proposed PI Controller in Fig. 5. The current THD is shown in Fig. 6.

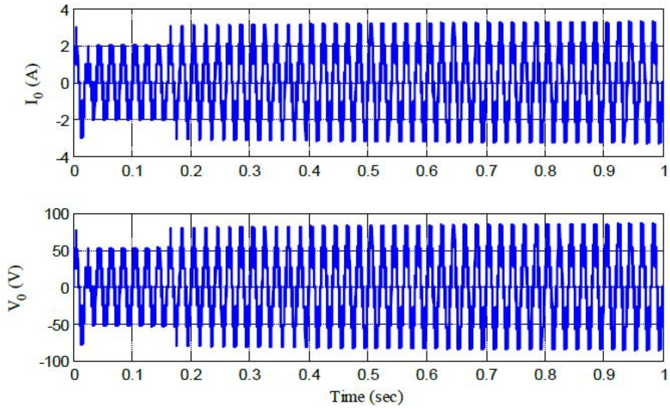

Fig. 5 Output current and voltage of symmetrical nine-level current source multilevel inverter using PI controller

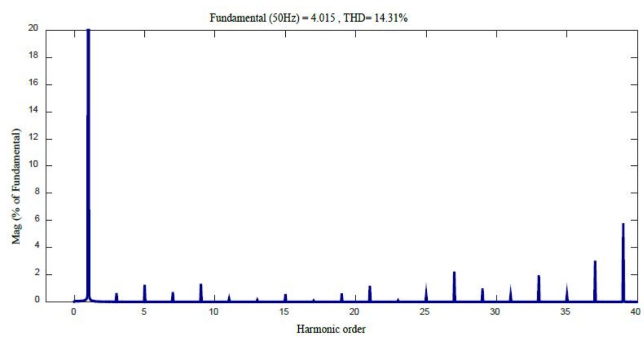

Fig. 6 Output current THD of symmetrical nine-level current source multilevel inverter

Fig. 5 shows the overall simulated responses of the nine-level single rating inductor symmetrical current source inverter output current and voltage with PI controllers and their output responses obtained.

Fig. 6 shows the current harmonic response of symmetrical nine-level current source inverter, which shows the total current harmonic distortion to be 14.31%.

In the spectrum analysis, the total harmonic produced is 14.31%. Maximum amount of low order harmonics has been removed and the order of the harmonics is less than 0.5% except fundamental. Fig. 7 shows the overall simulated responses of the asymmetrical nine-level single rating inductor current source inverter output current and voltage with PI controllers and THD in Fig.8.

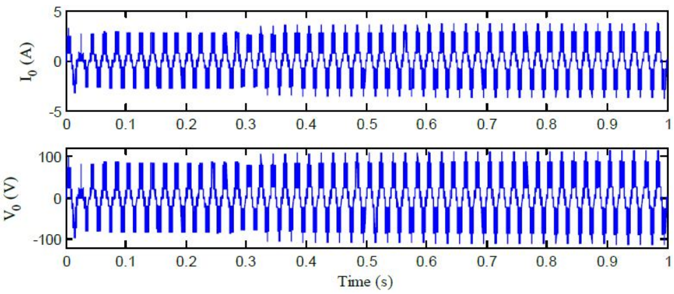

Fig. 7 Output current and voltage of asymmetrical nine-level current source multilevel inverter using PI controller

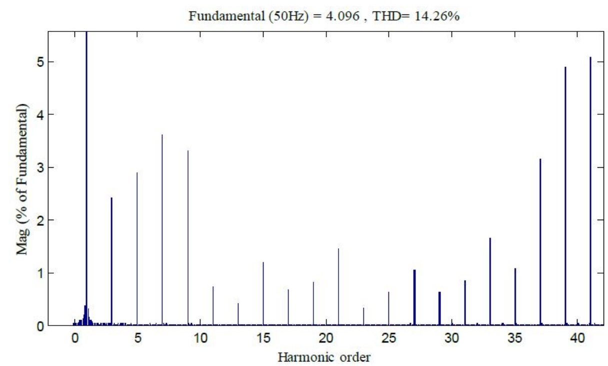

Fig. 8 Output current THD of asymmetrical nine-level current source multilevel inverter

Multicarrier pulse width modulation strategy is implemented for IGBT switching with PI Controller. Fig. 8 shows the current harmonic response of asymmetrical nine-level current source inverter, with the total current harmonic distortion of 14.26%.

VII. CONCLUSION

The modeling and analysis of nine-level current source multilevel inverter using proportional integral (PI) controllers with multicarrier pulse width modulation (PWM) control technique platform is implemented. The configuration for the proposed system is designed and simulated using MATLAB/Simulink. Current source multilevel inverter is built with state-of-the-art power devices that have fast switching times. It is observed that the asymmetrical current source multilevel inverter circuit provided a good %THD and steady state analysis controlled by PI controllers. Based on topology wise the asymmetrical inverter is economical with less number of components to achieve the same (nine) level compared with symmetrical current source multilevel inverter. The switching and conduction losses minimized due to the presence of fewer components in the power circuit of asymmetrical current source multilevel inverter. The multicarrier pulse width modulation technique involved to further improve the performance of the current source inverter by reduces the THD. This system guarantees a fast transient response, a high disturbance rejection capability, a robust performance and lower THD is obtained. The simulation also proves that if any failure occurs in any one of the switches it is still capable of producing multiple voltage levels without shunt downing the entire systems. The simulation result also proves the effectiveness of the proposed current source multilevel inverter which uses less number of power semiconductor devices. The results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of switches and carriers for PWM.

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