10-Bit Current Steering DAC in CMOS 130nm Technology

KolupuriKiran Kumar[1], Ashok Kumar Adepu[2]
[1, 2] Department of ECE
[1]MVGR College of Engineering
[2] Assistant Professor, MVGR College of Engineering

Abstract- *This paper proposed a 10-bit current steering (segmented architecture)digital-to-analog converter, with different sizes of current sources. The proposed 10-bit digital-to-analog converter was implemented using TSMC CMOS 130 nm 1P2M technology. The power consumption was approximately 23.015 mW at the sample rate of 200 MHz, and the supply voltage was 3.3 V. It achieved a DNL (differential nonlinearity) and an INL (integral nonlinearity) of 0.06 LSB and 0.04 LSB, respectively. In segmented (4LSB-6MSB) architecture the measured SFDR (spurious free dynamic range) was 88.156 dB. This work presented a good performance compared with other researches in DNL, INL and area.*

Keywords- Current steering DAC, Current source, INL, DNL, SFDR, Area.

I. INTRODUCTION

Real world signals are in analog form but digital signals are processed easily with simple circuits so analog signals are converted into digital form. The digital signals are converted back to analog form to do some practical functions. The circuit that perform this conversions are digital-to-analog converters, and at the output of this DACs load is connected. In this paper CMOS current steering DAC is designed with BA decoders, current sources and resistor at the output stage.

Basically there are three types of current steering architectures unary array, binary array, and segmented array architecture. Unary current DACs use a single-current element for each quantization step. Unary current DACs are analogous to resistor divider DACs with a resistor element for each LSB. The drawback of unary arrays is that the complexity of the digital decoder is exponentially related to the resolution. Binary current DACs group current elements into binary multiples that are turned on or off directly with the input bits. This eliminates the decoder required in unary current DACs.

Segmented arrays consist of different sub-arrays, or segments, each with a potentially different array coding. The MSB-segment is a unary array with 2M-1 element and represents the upper M bits. The LSB-segment realizes the lower L bits in a binary array.

The current source used here has no capacitance so the circuits need not to be charge or discharge in ON state. For high speed and high resolution designs current steering Digital to Analog Converters are more suitable. As frequencies and conversion rates increases, frequency domain parameters like SNR, SFDR parameters become more useful than static parameters like INL and DNL.

The static performance of DACs such as DNL and INL must be considered, as well as the dynamic performance of DACs such as SFDR. A DNL should be smaller than 1 LSB, and the DAC converter should be kept monotonic. Every increase of the digital input code increases the analog output value. The DNL is always smaller than 1 LSB if the INL is smaller than 0.5 LSB. An INL should be less than 0.5 LSB, which ensures that the maximum linearity error is smaller than the maximum quantization error.

II. CIRCUIT ANDLAYOUT

2.1 BA DECODER

Fig.1. shows the 2-bit Binary to Abacus decoder. It consisted of AND gate and OR gate.S0-S2are the control signals for current source. The Binary to Abacus (BA) module uses to transform binary code (I1I0)2 to 3 thermometric codes (S2S1S0).The output current of the current source is I0i.e 1mA. This DAC uses a BA decoder instead of conversional decoding construction, which provides some advantages. The BA decoder contains one AND gate and one OR gate. The advantages of the BA decoder are a reduction of DAC circuit complexity, delay and power consumption respectively. All these gates are implemented using CMOS logic. This requires six transistors for each logic gate. Fig.2. shows 4-bit BA decoder. This decoder is a combination of two 2-bit BA decoders.Fig.3. shows the layout of 2-bit Binary to Abacus decoder.

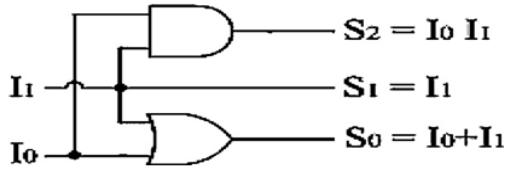

Figure1: 2-Bit BA Decoder

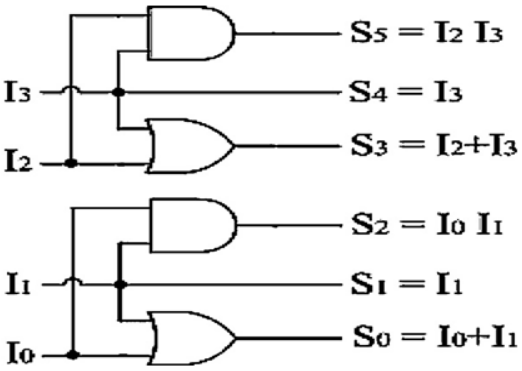

Figure2: 4-Bit BA Decoder

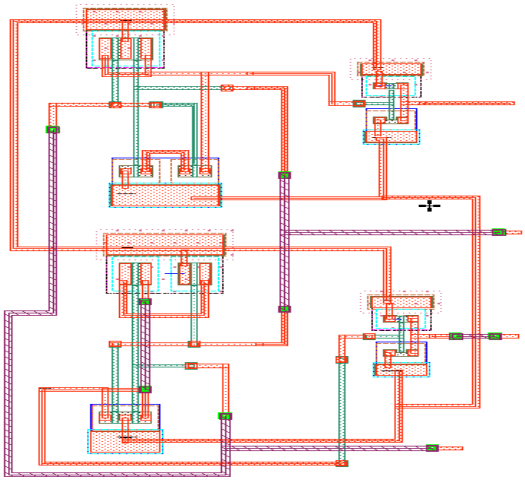

Figure3: Layout of 2-Bit BA Decoder

2.2 CURRENT SOURCE

The current source used here is driven by the binary input. To act as a current source the gate voltage must be constant. The current source performance is improved by improving two parameters i) small signal output resistance by increasing resistance a more constant current over a large range of Vout values. ii) Reduce the Vmin voltage by allowing a large range of Vout over which current source work properly. To reduce Vmin by increasing value of W/L and adjusting the gate to source voltage to get the same output current.

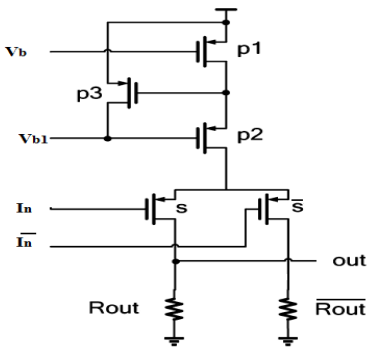

Figure4: Schematic diagram of current source

In the Figure 4: P1 controls the value of current by varying width of P1. The goal of MOSFETs Sand S¯they act like switches. The gate terminal of Sis connected to binary input. MOS Sturns on the switch and S¯turns off the switch for a given input. The current sources that are turned on generate current flows through the output resistor Rout to generate an analog output from the DAC. MOSFET P3 is used to increase the output impedance. The high output impedance can improve the performance of INL and SFDR. The schematic of current sourceis shown in Figure 5.

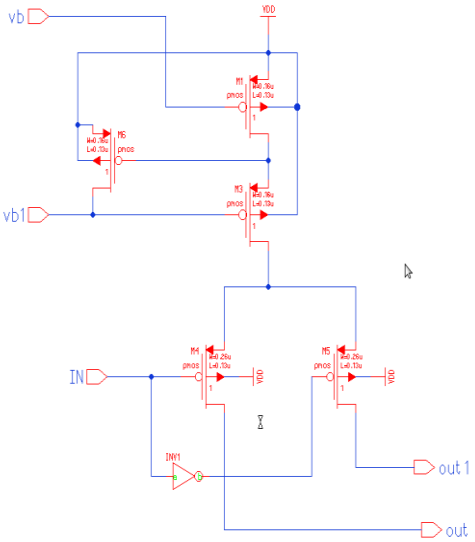

Figure 5:Schematic of Current Source

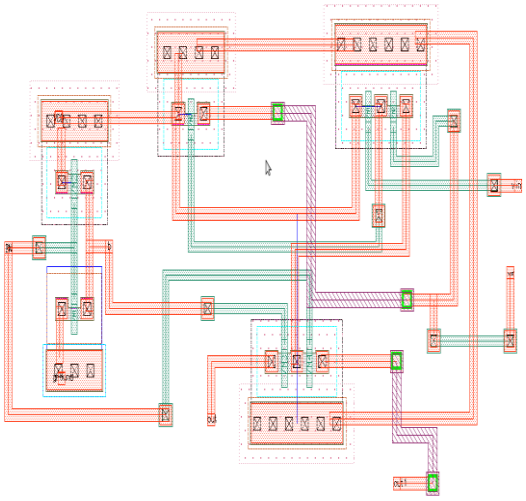

Figure 6: Layout of Current Source

III. PROPOSED 10-BIT DAC

This circuit includes both BA (binary to Abacus) modules called BA decoder and current source modules (which includes both current mirror and switch circuit).The general 10-bit DAC module contains three BA decoders, as shown in

Fig.7.The first BA decoder transfers A0–A3 to thermometric code, which controls the on/off of I0 and 4I0 current source. The second BA decoders transfer A4–A7 to thermometric codes, which controls the on/off of 16I0 and 64I0 current source. And the third BA decoders transfer A8–A9 to thermometric codes, which controls the on/off of 256I0 current sources, respectively.

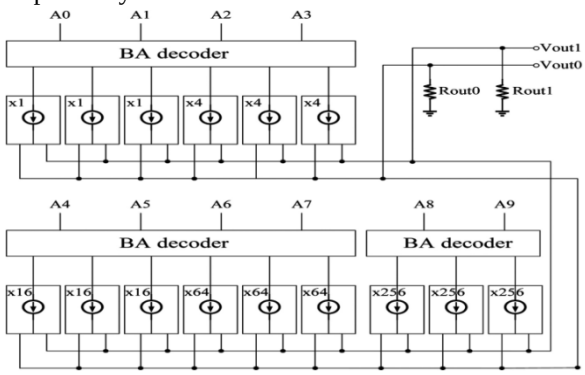

Figure7: 10-bit current-steering DAC Architecture

Each bit of thermometric code controls a current source in the current source module. All the current source cells are divided into five different unit groups, i.e. I0, 4I0, 16I0, 64I0and 256I0. Each group contains three cells. Therefore, the above two modules constitute an10-bit DAC. The analog signal is converted by current flowing directly through the output resistor. It can generate a voltage varying from 0 to 1023 units, which of equally spaced level output voltage. Fig. 7 shows the general construction of a 10-bit current-steering DAC.

3.1 BINARY 10-BIT DAC

Figure8: Shows the Binary Weighted Current Steering DAC. This DAC uses 10 current sources each current source has its own weights according to the position where it is used. Figure9: Shows the Layout of Binary Weighted DAC.

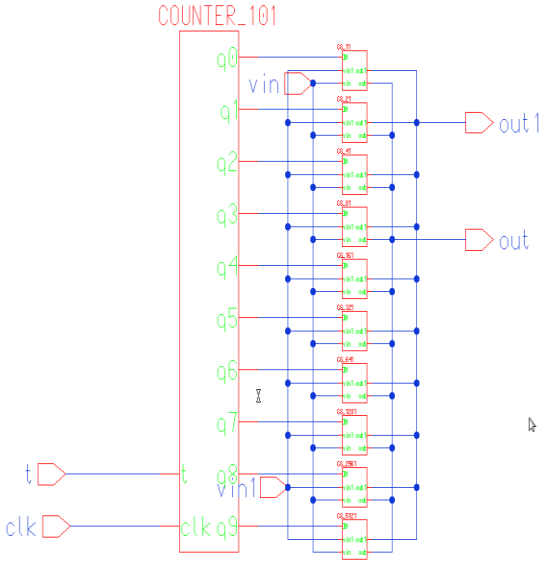

Figure8: 10-bit Binary Weighted DAC Architecture

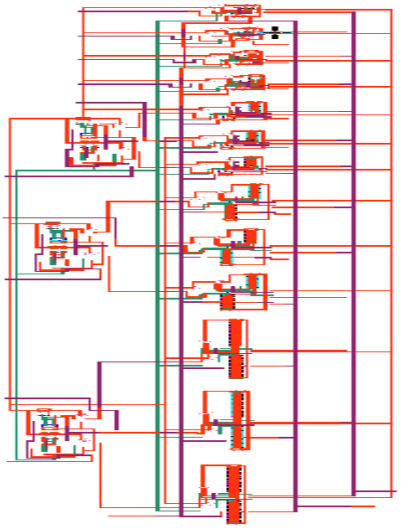

Figure9: Layout of 10-bit Binary Weighted DAC

3.2 SEGMENTED 10-BIT DAC

Figure10: Shows the Segmented DAC. In this DAC three BA decoders and seven current sources are used as it is a 4-LSB 6-MSB segmented DAC. Figure11: Shows the layout of segmented DAC.

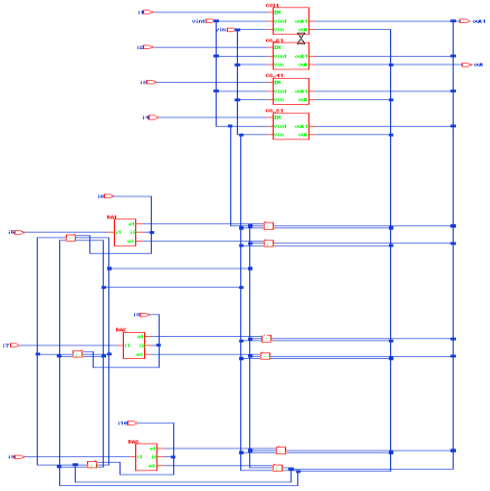

Figure10: 10-bit current-steering DAC Architecture

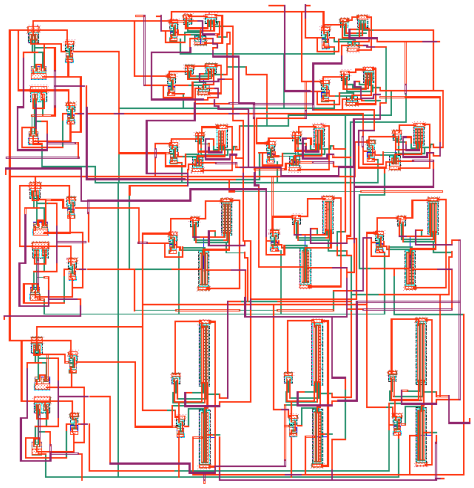

Figure11: Layout of 10-bit current-steering DAC

IV. SIMULATION RESULTS

Figure12: Shows the simulation result of 10-Bit Segmented DAC.

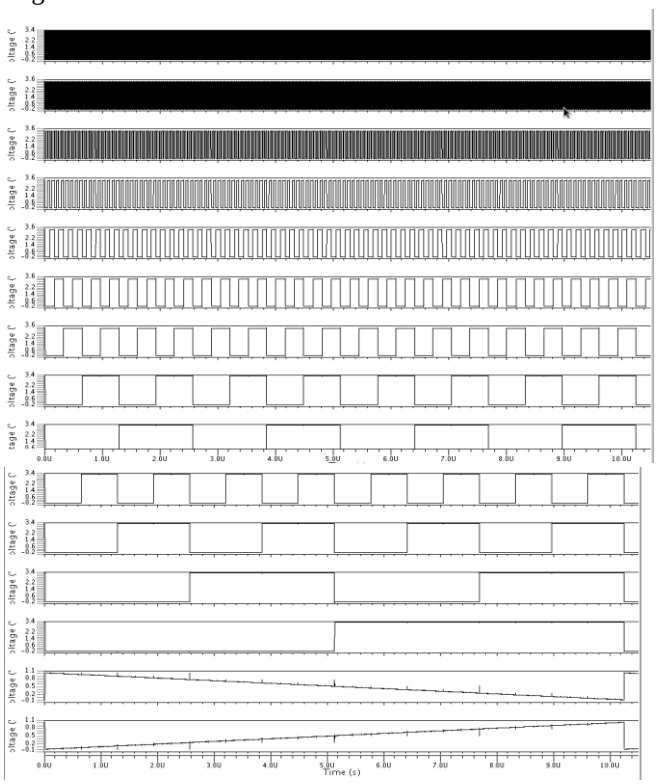

Figure12: Shows the simulation result of 10-Bit Segmented DAC

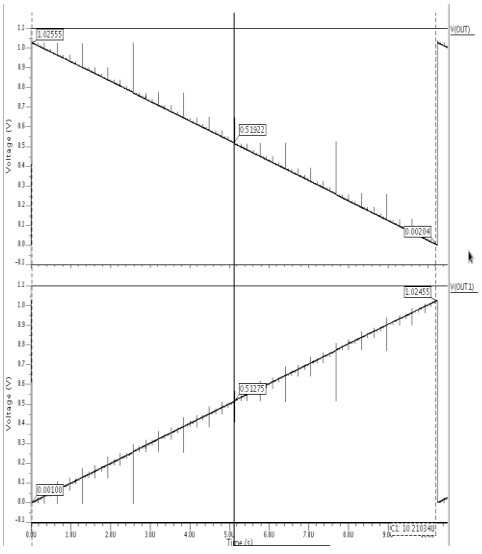

Figure13: Shows the Result of Some Input Bits

Figure12: Shows the simulation result of 10-Bit Segmented DAC, in which the result of a given input 0010000000is 127.021 mV. The segmented DAC consists of current source modules of different weights. The digital input bits In1, In2, In3, In4 drives the first four current sources of having weights 1, 2, 4 and 8 gives a current of I1, I2, I3, I4 andI7respectively.All these current sources produce different currents and all these currents are added finally to get the output current. Differential nonlinearity is the difference of the output level between two adjacent codes. Integral nonlinearity is the measure of the actual output voltage level minus the ideal level. The values of DNL and INL after simulation are ± 0.04 and ± 0.05. The SFDR calculated is 88.156 dB.The loading effect may degrade the performance of the DAC as it adds parasitic capacitance in the circuit.

Table 1: Comparison of Experimental Results

Parameters	Ref [1]	Ref [2]	Ref [3]	This Work
Resolution	10	10	10	10
Sample Rate (MHz)	200	210	80	200
DNL	0.16	0.7	0.55	0.06
INL	0.13	1.1	0.4	0.040
Supply Voltage (V)	3.3	3.3	2.5	3.3
Power Dissipation(mw)	7.9	83	27.65	23.015
SFDR (dB)	77.9	59.36	68.15	88.156
Area (mm^2)	0.0378	5	0.185	0.0190
Technology (nm)	350	350	250	130

VI. CONCLUSION

In this paper, a 10-bit current-steering segmented (4LSB-6MSB) DAC was proposed. The technology is TSMC 130 nm CMOS process. The power consumption was about 23.015 mW at the sample rate of 200 MHz. The supply voltage was 3.3 V. It achieved a DNL and INL of 0.06 LSB and 0.04 LSB, respectively. The SFDR of simulation was about 88.15 dB. This work presented a good performance when compared with researches in DNL, INL, SFDR and area. This design is suitable for low-power electrical productions.

ACKNOWLEDGMENT

We the authors would like to take this opportunity to extend our thanks to Department of ECE, MVGR College of Engineering, Vizianagaram for providing required tools to do research in VLSI Domain.

REFERENCES

[1] Yi S-C. A 10-bit CMOS current-steering digital to analog converter. AEU – Int J Electron Commun 2012;66:433–7.
[2] Cho H-H, Park C-Y, Yune G-S, Yoon K-S. A 10-bit 210 MHz CMOS D/A converter for WLAN. In: IEEE Asia-

Pacific conference on advanced system integrated circuits. August 2004. p. 106–9.

[3] Halder S, Banerjee S, Ghosh A, Prasad R, Chatterjee A, Dey SK. A 10-bit 80-MSPS 2.5-V 27.65-mW 0.185-mm2 segmented current steering CMOS DAC'. In: 18th international conference on VLSI design. January 2005. p. 319–22.

[4] Ashok Kumar Adepu and Kiran Kumar Kolupuri. "A 130-nm CMOS 400 MHz 8-bit Low Power Binary Weighted Current Steering DAC". International Journal on Cybernetics & Informatics (IJCI) Vol. 5, No. 4, August 2016.

[5] Yi S-C. An 8-bit current-steering digital to analog converter. AEU – Int J Electron Commun 2012;66:433–7.

[6] B. Razavi, Principles of Data Conversion System Design. New York IEEE Press, 1995.

[7] Huei-Chi Wang, Hong-Sing Kao, and Tai-Cheng Lee. An %bit 2-V 2-mW 0.25-mm2 CMOS DAC in 2004 IEEE Asia-Pacific Conference on Advanced System Integrated Circuits(AP-ASIC2004).

[8] Hong GM, Hsu S-H, Peng Y-H, Chen AH-H, Wang Y-T, Lu H-H." A 10-bit 300 MHz 0.1 mm2 triple-channel current-steering DAC 75.98 dB SFDR in 65 nm". In: VLSI DAT 2008, IEEE international symposium on VLSI design, automation and test. April 2008