Multiplexer Design And Analysis Using 18nm Finfet Technology

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Abstract- *Multiplexer is a basic block of many processors or ready to use board like FPGA's. This work explores multiplexer design with different technology and logic style for improvement in performance. Conventional CMOS technology is useful at 45nm and above technology due to low power consumption and perfect logic zero and logic transition. Advantage multiple gates in FinFET technology makes it more suitable for high-speed logic transitions. Use of FinFET increases drive current and improves the circuit speed at compromise in term of power. FinFET technology with logic style improves power overhead on IC per unit area. In this paper, a multiplexer is designed using 18nm FinFET and result are compared with CMOS technology for similar operating conditions. Also, FinFET is explored with different logic style for the optimization in delay and power calculations. All the design and simulations are performed on QCA designer.*

Keywords- FinFET, CMOS, Pseudo NMOS, Multiplexer, power, delay etc.

I. INTRODUCTION

Flexible design with different ready-to-use boards leads designer to explore more on performance improvement of CMOS based IC's and hardware optimizations. FPGA is one of the examples of such flexible designing whose basic building block is 2x1 multiplexer block for logic implementations. Technology scaling affect more on performance that need new logic style and techniques for power, delay and area improvements. Conventional CMOS are found suitable with technology 45nm or higher withsub threshold performance under limit. For the improvement in IC area, lower technology nodes are preferred but they suffer from higher power consumption and higher power density per IC area.

Multiple gate transistor shows more control on gate and helps in controlling leakage current in transistor with lower dimensions. As conventions MOSFET has single gate while in in FinFET gates are there on all three sides of vertical channel called Fin. Multiple gates like fin also increases effective channel width that leads to higher drive current and higher speed of IC. FinFET are available in double or triple gate format depending upon the tope oxide layer thickness. When oxide thickness under top gate is more than it work like double gate. FinFET emerged as promising device in different logic and memory applications. Various techniques used further for power improvement in FinFET using different FinFET architecture or material by improving ON/OFF current ratio and sub-threshold performance improvement.Quantum Cellular Automata (QCA) refers to models of quantum computation, which have been devised in analogy to conventional models of cellular automata introduced by von Neumann. It may also refer to quantum dot cellular automata, which is a proposed physical implementation of "classical" cellular automata by exploiting quantum mechanical phenomena. QCA has attracted a lot of attention as a result of its extremely small feature size (at the molecular or even atomic scale) and its ultra-low power consumption, making it one candidate for replacing CMOS technology.

In QCA, a quantum cell normally consists of four quantum dots at the corners of a square pattern, with two excess electrons that are free to tunnel between the dots but which cannot leave the cell. Due to Coulomb repulsion, these two electrons tend strongly to occupy diagonally opposite dots. In a second type of QCA cell, the dots are located at the middle of the sides of the cell, instead of at the corners. In either cell type, there are just two configurations with energetically equivalent polarizations designated as +1 and −1. This means that quantum cells can be employed as binary systems to represent logical true and false (or digital 1 and 0). Moreover, multiple quantum cells can be arranged in various linear formations to produce logic gates, which can in turn be used to build devices for computation. The basic logic elements in QCA logic are the majority gate and the inverter (or NOT gate).

Compared to CMOS technology, QCA and MQCA are two promising contenders for alternative computing paradigms. QCA accomplishes computation via Coulomb interactions of the electrons confined in quantum dots. A typical QCA cell design contains four quantum dots and two electrons hopping among them. QCA is extremely energy

efficient but requires low operation temperature due to the current state of semiconductor technology. Magnetic-QCA, on the other hand, is spin-based and utilizes the magnetic dipole interactions among the Nanomagnet pillars. Room temperature realization of magnetic QCA gives a new aspect to the computing paradigm. MQCA works at room temperature, which is the immediate advantage over QCA. Its switching depends on the external field and magnetostatic interaction from its nearest Nanomagnet neighbor. There are many ways to make logic devices using magnets. One of the most straightforward approaches: is building logic gates and wires out of small patches of magnetic material. These "Nanomagnets" act just like tiny bar magnets. Imreet al. presented logic functionality in networks of physically coupled, nanometer-scale magnets designed for digital computation in MQCA systems.

Additionally, researchers realized that planar, magnetically-coupled, nanometer-scale magnets perform binary computation. In standard applications, the magnetization direction of the nanomagnet points up and down representing binary values '1' and '0', respectively. The easy axis corresponds to the low energy polarization, and the hard axis has the highest energy polarization. To date MQCA-based Majority Gate using driver magnets, universal gates , wire architecture , XOR gate using shape anisotropy, and implementation of full adder are investigated. Existing designs like full adders and XOR are based on vertical layout (column based design) and horizontal layout (row based design) approaches. Varga et al. demonstrated the working of full adder using slant edge nanomagnets , afterwards using inclined clocking field with 45° alignment in NML-based adder was implemented, which reduced the operational error rate. Subsequently, Siva subramani et al. proposed shape and positional hybrid anisotropy based full adder. In recent years 2:1 Mux was implemented using semiconductor and Nanomagnetic QCA. Motivated by the above research approach, we implemented, first of its kind, Magnetic QCA based 2:1 Mux with the help of the compact, horizontal, and vertical design approaches based on mixed positional strategy and shape anisotropy.

II.LITERATURE REVIEW

2.1 QUANTUM CELLULAR AUTOMATA: THE PHYSICS OF COMPUTING WITH ARRAYS OF QUANTUM DOT MOLECULES

AUTHOR: Craig. S. Lent, P. Douglas Tougaw, and Wolfgang Porod

The fundamental limits of computing using a new paradigm for quantum computation, cellular automata composed of arrays of Coulombically coupled quantum dot molecules, which we term quantum cellular automata (QCA). Any logical or arithmetic operation can be performed in this scheme. QCA's provide a valuable concrete example of quantum computation in which a number of fundamental issues come to light. We examine the physics of the computing process in this paradigm. We show to what extent thermodynamic considerations impose limits on the ultimate size of individual QCA arrays. Adiabatic operation of the QCA is examined and the implications for dissipation less computing are explored.

2.2 QCADESIGNER: A RAPID DESIGN AND SIMULATION TOOL FOR QUANTUM-DOT CELLULAR AUTOMATA

Author: Konrad Walus, Timothy J. Dysart, Graham A. Jullien, and R. Arief Budiman

This paper describes a project to create a novel design and simulation tool for quantum-dot cellular automata (QCA), namely QCADesigner. QCA logic and circuit designers require a rapid and accurate simulation and design layout tool to determine the functionality of QCA circuits. QCADesigner gives the designer the ability to quickly layout a QCA design by providing an extensive set of CAD tools. As well, several simulation engines facilitate rapid and accurate simulation.

2.3 NEIGHBORHOOD DETECTION USING MUTUAL INFORMATION FOR THE IDENTIFICATION OF CELLULAR AUTOMATA

Author: Y. Zhao and S. A. Billings

Extracting the rules from spatiotemporal patterns generated by the evolution of cellular automata (CA) usually requires a priori information about the observed system, but in many applications little information will beknown about the pattern. This paper introduces a new neighborhood detection algorithm which can determine the range of the neighborhood without any knowledge of the system by introducing a criterion based on mutual information (and an indication of over-estimation). A coarse-to-fine identification routine is then proposed to determine the CA rule from the observed pattern. Examples, including data from a real experiment, are employed to evaluate the new algorithm.

III. METHODOLOGY

QCA TECHNOLOGY

A brief description about Multiplier is given in this section used to data encoded using QCA method.

3.1 QCA DEVICE BACKGROUND

QCA cells perform computation by interacting coulombically with neigh boring cells to influence each other's polarization. In the following subsections we review some simple, yet essential, QCA logical devices: a majority gate, QCA "wires", and more complex combinations of QCA cells.

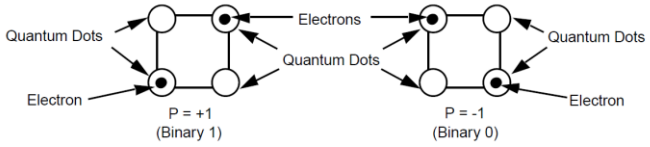

Figure1: QCA cell polarizations and representation of binary1 and binary 0

The isolated cell there are two energetically minimal equivalent arrangements of the two electrons in the QCA cell, denoted cell polarization P = +1 and cell polarization P = -1. Cell polarization P = +1 represents a binary 1 while cell polarization P = -1 represents a binary 0. This concept is also illustrated graphically Figure 1.

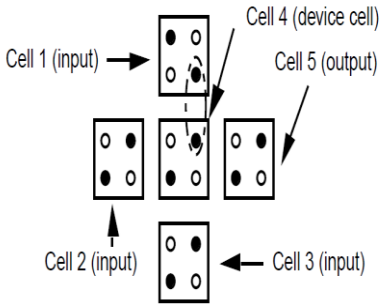

Figure2:The fundamental QCA logical device - the majority gate

For example of three inputs are cell 1, cell 2, and cell 3. The cell 4 is device cell (it is a fixed polarization) the fixed polarization is two categories such as the fixed polarization is -1 that is AND gate operation and the fixed polarization is +1 that is OR gate operation. The majority gate three input operation has combined to both (AND and OR) operation. The bit value 0 that is called as polarization of -1 and the bit value 1 that is called as polarization of +1.

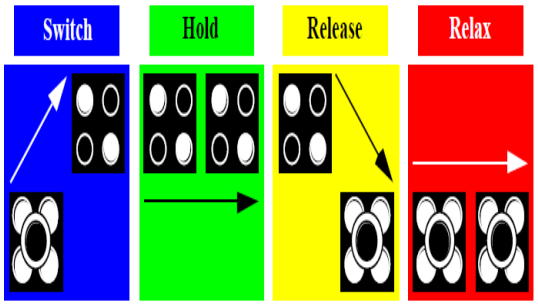

Figure 3: The four phases of the QCA clock

During the first clock phase, the switch phase, QCA cells begin un-polarized and their interdot potential barriers are low. The barriers are then raised during this phase and the QCA cells become polarized according to the state of their driver (i.e. their input cell). It is in this clock phase that the actual computation (or switching) occurs. By the end of this clock phase, barriers are high enough to suppress any electron tunnelling and cell states are fixed. During the second clock phase, the holdphase, barriers are held high so the outputs of the sub array can be used as inputs to the next stage. In the third clock phase, the release phase, barriers are lowered and cells are allowed to relax to an un-polarized state. Finally, during the fourth clock phase, the relax phase, cell barriers remain lowered and cells remain in an Un-polarized state. The four clock phases are illustrated in two different ways while an example of a value being transmitted on a QCA wire is illustrated in.

3.2 MULTIPLEXER DESIGN IN QCA TECHNOLOGY

Multiplexing means transmitting a large number of information over a smaller number of channels or lines. A digital multiplexer (data selector) is a combinational circuits that selects binary information from one of many input lines and directs it to a single output line. With two input signals and one output signal, the device is referred to as a 2-to-1 multiplexer; with four input signals it is a 4-to-1 multiplexer; etc.

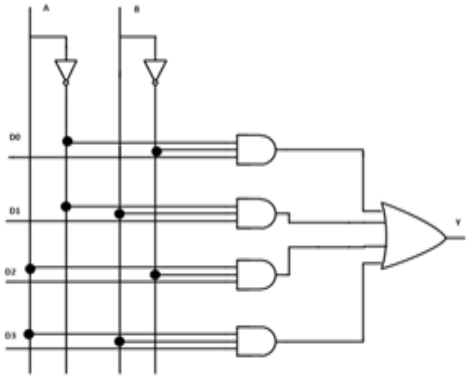

Figure 4: Logic diagram of 4:1 multiplexer

Expression of multiplexer:

Y=majority([majority(D0,A',B',0),majority(D1A',B,0),majority(D2,A,B',0),majority(D3,A,B,0),],1)

1V. SIMULATION RESULTS

4.1SIMULATION MODEL OF MULTIPLEXER

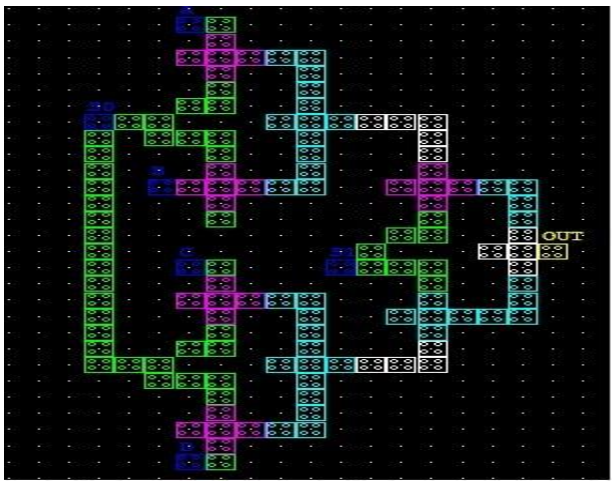

Figure 4:Simulation circuit of 4:1 Multiplexer

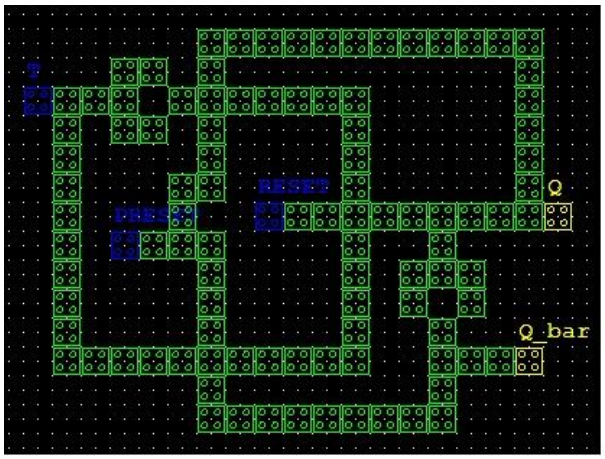

Figure 5: Simulation circuit of T Flip Flop

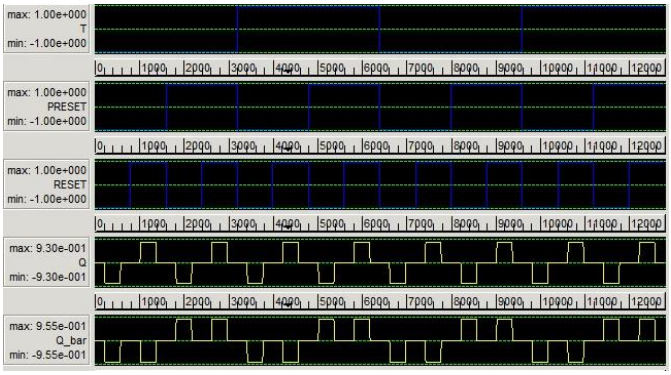

Figure 6: Simulation output of T Flip Flop

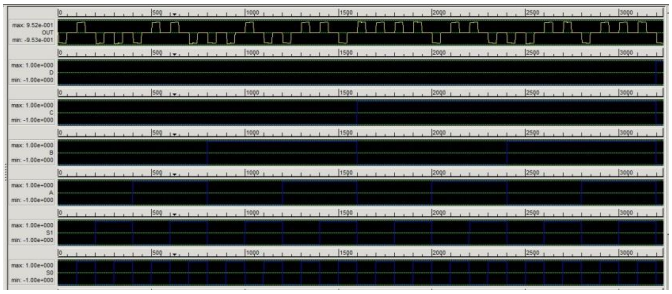

Figure 9: Simulation output of 4:1 Multiplier

V. CONCLUSION

A comparative analysis of Multiplexer designed using 18nm FinFET and 45nm CMOS are compared for CMOS logic and Pseudo NMOS logic in terms of power, delay and IC area. Due higher physical size of 45nm CMOS based multiplexer is showing less power consumption and similar values of delays as compared to 18nm FinFET based multiplexer at the cost of higher IC area. The advantage of using 18nm FinFET, showing similar delay, less IC area at the cost of higher power consumption that can be reduced by reducing power supply. FinFET give perfect logic at lower voltages than similar CMOS based designs. Also, further power optimization techniques with use of different logic style reduces power consumption drastically in FinFET. There are chances of power reduction with new power reductions techniques that can be explored in future. FinFET based designed are preferred for the design of low power devices to reduce overhead on battery backup and suitable for IoT based portable devices.

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