An Improved Switching Activity Optimised LFSR For Energy Efficient Bist Applications

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Abstract- *Since many years, BIST has used (LFSRs) linear feedback shift registers to generate test patterns; nevertheless, a recent issue with design limitations has caused significant advancements in this area. In order to create test patterns for a given primitive polynomial LFSR TPG, this study provides a switching activity optimized bit swapping LFSR technique. In this case, LFSR test patterns are transformed into numerous test patterns. Moreover, to support updated Multiple Input Signature Register testing that includes expanded output response analyses. In the LFSR generation phase, reconfigurable LFSR with better reseeding is used to broaden fault coverage. The length of TPG can be changed using parametric initialization to allow a wide variety of CUTs. The BS-LFSR is coupled with a modified MISR to reduce the peak and average power (scan and capture) during the test cycle or in response to a signature analyzer. These methods significantly reduce the peak testing power while improving fault coverage or testing time.*

Keywords- LFSR, BIST, MISR.

I. INTRODUCTION

Built-in Self-Test (BIST) techniques constitute a class of schemes that provide the capability of performing at-speed testing with high fault coverage, whereas simultaneously they relax the reliance on expensive external testing equipment. Hence, they constitute an attractive solution to the problem of testing VLSI devices. BIST techniques are typically classified into offline and online. Offline architectures operate in either normal mode or test mode. During test mode, the inputs generated by a test generator module are applied to the inputs of the Circuit Under Test (CUT) and the responses are captured into a Response Verifier (RV). The normal operation of the CUT is stalled and, consequently, the performance of the system in which the circuit is included, is degraded. Input vector monitoring concurrent BIST techniques have been proposed to avoid this performance degradation. These architectures test the CUT concurrently with its normal operation by exploiting input vectors appearing to the inputs of the CUT; if the incoming vector belongs to a set called active test set, the RV is enabled to capture the CUT response. The block diagram of an input vector monitoring concurrent BIST architecture The Concurrent Test Latency (CTL) of an input vector monitoring scheme is the mean time (counted either in number of clock cycles or time units) required to complete the test while the CUT operates in normal mode. In this brief, a novel input vector monitoring concurrent BIST scheme is proposed, which compares favorably to previously proposed scheme with respect to the hardware overhead/CTL tradeoff. This brief is organized as follows. In this Section, we introduce the proposed approach and in Section, we calculate its hardware overhead. In Section, we compare the proposed scheme with previously proposed input vector monitoring concurrent BIST techniques.

Basic fault models in digital circuits include: Stuck-at fault model: A signal, or gate output, is stuck at a 0 or 1 value, independent of the inputs to the circuit. The bridging fault model: Two signals are connected together when they should not be. Depending on the logic circuitry employed, this may result in a wired-OR or wired-AND logic function. Since there are O (n^2) potential bridging faults, they are normally restricted to signals that are physically adjacent in the design. The transistor faults: This model is used to describe faults for CMOS logic gates. At transistor level, a transistor maybe stuck-short or stuck-open. In stuck-short, a transistor behaves as it is always conducts (or stuck-on), and stuck-open is when a transistor never conducts current (or stuck-off). Stuckshort will produce a short between VDD and VSS. The open fault model: Here a wire is assumed broken, and one or more inputs are disconnected from the output that should drive them. As with bridging faults, the resulting behavior depends on the circuit implementation. The delay fault model, where the signal eventually assumes the correct value, but more slowly (or rarely, more quickly) than normal produce same faulty behavior for all input patterns these faults are called equivalent faults.

Machine fault diagnosis is a field of Mechanical Engineering concerned with finding faults arising in machines. A particularly well developed part of it applies specifically to rotating machinery, one of the most common types

encountered. To identify the most probable faults leading to failure, many methods are used for data collection, including vibration monitoring, thermal imaging, oil particle analysis, etc. Then these data are processed utilizing methods like spectral analysis, wavelet analysis, wavelet transform, short term Fourier transform, Gabor Expansion, Wigner-Ville Distribution (WVD), cestrum, bi-spectrum, correlation method, high resolution spectral analysis, waveform analysis (in the time domain, because spectral analysis usually concerns only frequency distribution and not phase information) and others. The results of this analysis are used in a root cause failure analysis in order to determine the original cause of the fault. For example, if a bearing fault is diagnosed, then it is likely that the bearing was not itself damaged at installation, but rather as the consequence of another installation error (e.g., misalignment) which then led to bearing damage. Diagnosing the bearing's damaged state is not enough for precision maintenance purposes. The root cause needs to be identified and remedied. If this is not done, the replacement bearing will soon wear out for the same reason and the machine will suffer more damage, remaining dangerous. Of course, the cause may also be visible as a result of the spectral analysis undertaken at the data-collection stage, but this may not always be the case. The most common technique of detecting fault is the time-frequency analysis technique. For a rotating machine, the rotational speed of the machine is not a constant, especially not during the start-up and shutdown stages of the machine. Even if the machine is running in the steady state the rotational speed would vary around a steady-state mean value, and such a variation depends on load and other factors.

II. LITERATURE REVIEW

2.1IOANNIS VOYIATZIS, ANTONIS PASCHALIS, "A CONCURRENT BUILT-IN SELF-TEST ARCHITECTURE BASED ON A SELF-TESTING RAM"

In this paper novel input-vector monitoring concurrent BIST technique for combinational circuits based on a self-testing RAM, termed R-CBIST. Small hardware overhead, whereas there is no need to stop the ROM normal operation .In off-line BIST, the normal operation of the CUT is stalled in order to perform the test. The total circuit performance is degraded. We propose a novel technique for online testing, which we call Built-In Concurrent Self -Test (BICST). BICST assumes the presence of underlying BIST resources for off-line testing. These resources are modified in such a way that they can be used for both off-line and online testing. We also propose a technique for sharing the BICST hardware resources between identical circuits, thereby reducing the overall extra overhead for testing.

2.2.IOANNIS VOYIATZIS AND CONSTANTIN HALATSIS "A LOW-COST CONCURRENT BIST SCHEME FOR INCREASED DEPENDABILITY"

In this paper a concurrent BIST technique for combinational circuits is presented. Significantly more efficient than the input vector monitoring techniques proposed. Concurrent Test Latency and hardware overhead trade-off, for low values of the hardware overhead. Number of theorems required Input vector-monitoring concurrent BIST techniques are suitable for the testing of ROM because they meet both above requirements. The results in low hardware overhead, and therefore it is a practical solution for the concurrent testing of ROM modules, a BIST scheme for ROM modules should meet two basic requirements no need to set the ROM off-line very high effective fault coverage.

2.3SOBEEH ALMUKHAIZIM, AND YIORGOS MAKRIS "CONCURRENT ERROR DETECTIONMETHODS FOR ASYNCHRONOUS BURST-MODE MACHINES"

In this paper an Asynchronous controllers exhibit various characteristics that limit the effectiveness and applicability of the Concurrent Error Detection (CED) methods developed for their synchronous counterparts. To avoid false alarms cost is reduced by allowing hazards in the duplicate circuit. It requires re encoding of the fault. In order to address the hazard detection problem, we propose the addition of specialized circuitry that detects errors causing only hazards but no functional discrepancy at the outputs of the circuit. By using the checking synchronization method and the Hazard Detection Circuit (HDC), we develop three CED methods, all of which guarantee detection of all functional errors and hazards.

III. METHODOLOGY

3.1 BUILT IN LOGIC BLOCK OBSERVER

A brief description about BILBO is given in this section used to decode data encoded using Multiple Input Signature Register.

Built In Logic Block Observer has gained importance for its ability to take up different types of responsibilities depending upon the control signals forced on it. For instance, it can function as a simple register and in other, it can function as a Pseudo Random Test Pattern Generator (PRTPG); also, to generate signatures for analysis, it can act as a Multiple Input Signature Register (MISR) too . The different modes of BILBO are tabulated in Table I for a better understanding. The

clear distinction of its modes and functionality is detailed in . BILBO allows the design engineers to execute the process of testing the logic circuits in a scheduled manner so as to have a good understanding of the outputs for the state in which the BILBO functions. For example, in a clock cycle if a particular of the BILBO registers acts as a MISR; its availability for that instance is reserved. It is only in the next clock cycle, it can act as an LFSR or as a simple registerdepending upon the need of testing application.

Control Signal-1 (B1)	Control Signal-2 (B2)	Mode of Operation
0	0	Serial Scan Chain
0	1	LFSR Test Pattern Generator
1	0	Normal D Flip-Flop
1	1	MISR Response Compactor

TABLE 3.1 MODES OF OPERATION FOR BUILT IN LOGIC BLOCK OBSERVER

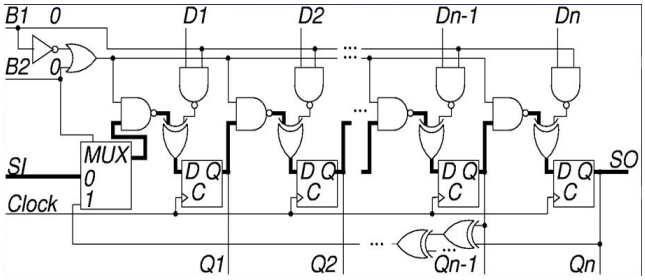

FIG: 3.1 8 BIT BILBO

Flip-flops from the CUT to construct the TPG and ORA functions. The basic idea is to partition the CUT into groups of flip-flops and groups of combinational logic. Each group of flip-flops is augmented with additional logic to provide multiple modes of operation. When the BILBO functions as a TPG, it provides pseudo-random test patterns by operating as an LFSR. When the BILBO functions as an ORA, it performs multiple-input signature analysis by operating as a MISR [138]. The application of BILBO to a CUT in its simplest form is illustrated, where the flip-flops at the primary inputs and outputs are used to construct two BILBOs. The BILBO at the primary inputs generates pseudo-random test patterns as a TPG and the BILBO at the primary outputs operates as a MISR-based ORA. The task of determining whether fabricated chips are fully functional is highly complex and will be take much more time, energy and cost. It is know the debugging cost increase by abouttenfold from chip level to system level. Therefore the Design for Testability (DFT) is introduced in order to detect faults as early as possible. DFT is a name for design techniques that add certain testability features to the premise of the added features is that they make it easier to develop and apply manufacturing tests for the designed hardware. The purpose of manufacturing tests is to validate that the product hardware contains no defects that could, otherwise, adversely affect the product's correct functioning. The figure shows how the Built in Self-Test (BIST) running in the ICs. Built-in logic block observation (BILBO) has become one of the most widely accepted techniques for self-testing of complex digital ICs. This technique is based on grouping the storage elements of the circuit in the two registers which give this technique its name. ABILBO register has four functional modes: with each of the stages acting as independent registers; as a generator of pseudorandom sequences; as analyzer of multiple-input signatures; and reset of all stages. Now days, an engineer design the BILBO with the various type in order to make it reliability to use. As the number of transistor integrated into a single chip increase, mean that more power dissipated will be produce.

3.2 LFSR

Logic BIST (LFSR and BILBO) based Very Large Scale Integration (VLSI) Integrated Circuit(IC) testing. A Reconfigurable LFSR can be used as the test pattern generator as well as a response compactor inside Logic BIST to improve the fault coverage of IC testing. In Proposed System, 8-Bit MISR architecture is simulated in Modelism RTL simulator. The 8-Bit programmable MISR structures are synthesized in Xilinx Spartan 3E for implementing MISR on FPGA. All the designs are synthesized for ASIC in RTL compiler using 90nm standard cell technology library. Xilinx Tool has been utilized to implement programmable designs, and, analyzed for speed, power and area.

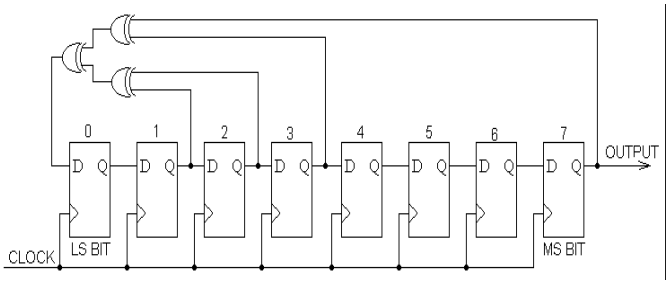

FIGURE 3.2: 8-BIT LFSR

In proposed dual-LFSR using high performance LFSRreseeding to reduces the total number of test patterns needed to cover every possible fault and also optimize the testing power. Here two LFSRs are used to generate the test sequences with improved correlation and allow controlled bit, transition over two successive test patterns which can significantly reduces the overall switching activity during testing. The performance metrics of dual-LFSR is

validatedusing ISCAS'89 benchmark circuits and showed significantreduction in test volume and associated switching activity. Inintroduced scalable test pattern generator and hierarchical concatenation of LFSR output to generate unified test sequence for BIST applications. The scalable characteristic reduces the memory space requirements with reduced number of seed values. The improvement in randomness characteristics allows maximum fault coverage.

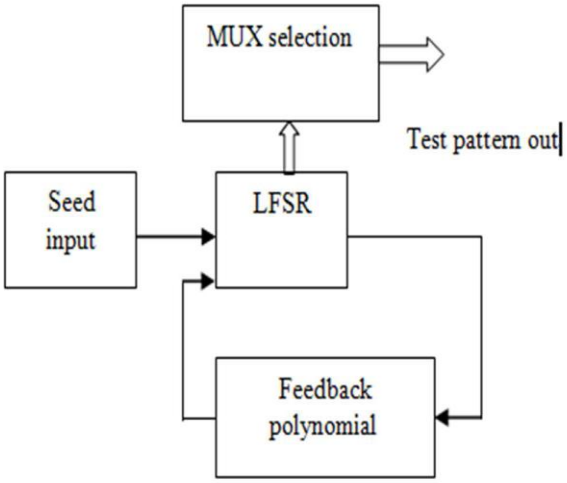

FIGURE 3.3:THE PROPOSED MUX BASED BIT SWAPPING LFSR TPG

Here the 100% fault coverage can be achieved with reduced number of actual LFSR test pattern generated usingoptimal bit swapping which is also used to reduce the overallswitching activity during testing process. In this TPG measures MUX units are used to influence the LFSR generated random output sequence. Based on test patternlength and associated LFSR size the MUX units are extendedfor bit swapping process. In proposed BS-LFSR both therandomness and switching activity are normalized by simplyre-ordering the LFSR generated test patterns using multiplexers which are included with the actual reseedingbased fixed polynomial LFSR. During testing process LFSR output formulated by MUX units controlled the bit transition associated to the two successive random patterns for each given LFSR pattern with the same level of randomization in terms of hamming distance which can discover more number of faults from CUT. As compared to conventional LFSR and multi polynomial LFSR model the proposed bit swapping LFSR offered more number of random sequence for each generated LFSR output patterns. For some complex BIST environments, the test sequence comes out from MUX selection units are reducing the overall switching activity.

1V. SIMULATION RESULTS

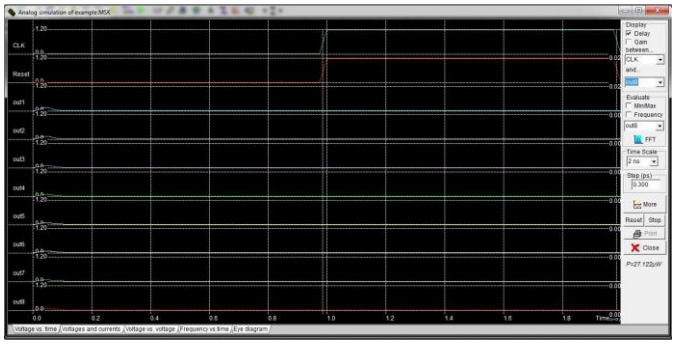

FIGURE 4.1: 8 BIT LFSR MICROWIND OUTPUT

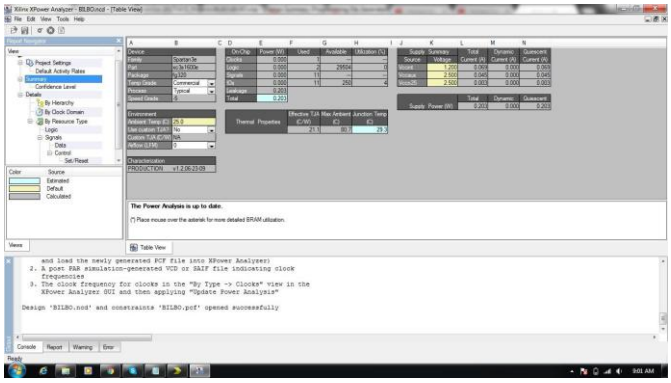

FIGURE 4.2: 8 BIT LFSR XILINUX POWEROUTPUT

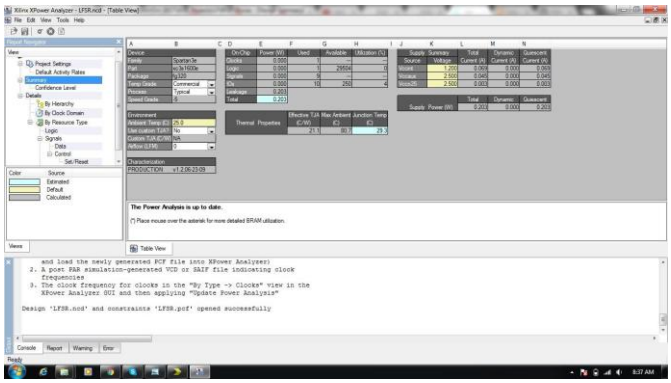

FIGURE 4.3: 8 BIT BILBO XILINUX POWER OUTPUT

V. CONCLUSION

In this project, we analyzed the performance of bit swapping LFSR with switch controlled priority based test pattern generation in BIST applications. The proposed LFSR's effectiveness in reducing the overall testing power reduction is validated experimentally and analogized with state-of-the-art LFSR reseeding and multi polynomial TPG methods. The simulation results proved that the randomness characteristics of test pattern generator and hardware synthesis results well proved the energy efficiency of proposed TPG with associated switching activity reduction. Here memory efficiency is also considered as potential advantages of proposed bit swapping

LFSR due to its inherent randomness characteristics which required only minimal number of LFSR seed values for desired fault coverage. It is also proved that the increasing number of seed values in ROM has no impact on attainable randomness. To extend the response analyzes the overall energy efficiency can be maximized by incorporating some post priority controlled switching mechanism.

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