Design of Low Noise Amplifier For WLAN IEEE 802.11ax Standard

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Abstract- *The receiver's sensitivity can be increased by using a low noise amplifier (LNA) which is able to effectively amplify low radio frequency signals while diminishing overall system noise. The fundamental performance indices and design techniques for the LNA are described in this paper. The circuit features three stages of which the first two stages are for minimum noise amplification and the final stage is for maximum gain amplification. A wideband amplifier is developed and simulated using Agilent's ADS, and the amplifying stage makes use of the common source topology to enhance gain and achieve greater isolation. For the purpose of increasing the stability of the circuit through the influence of impedance matching, small microstrip lines are added to the source tone in this design. To minimize the noise figure, traditional source inductive degeneration is used. The developed circuit is subsequently analyzed and simulated. It illustrates that the gain is between 29 dB and 31 dB between 5.9 GHz and 7.1 GHz (6 GHz center frequency), the noise figure is less than 1.5 dB, and the input and output reflection coefficients are less than -15 dB.*

Keywords- LNA, WLAN, IEEE 802.11ax, Noise Figure, Gain, ADS Simulation

I. INTRODUCTION

OW-NOISE amplifiers are an essential component in RF systems including satellite communications, radars, and WLAN applications. The primary function of a low-noise amplifier is to amplify the weak signal received by the receiver system while suppressing the noise signal, thereby reducing the noise figure and increasing the Signal to Noise Ratio(SNR).

The placement of the LNA as the first component of the receiver system is due to the Friis equation (Eq. 1), where F_1, F_2, F_3, etc. represent the noise figure produced by the respective RF components and G_1, G_2, G_3, etc. represent the gain produced by the RF components. F represents the overall noise factor of the system. Thus, minimizing F_1 as much as possible reduces the overall noise figure F of the entire system. Consequently, an LNA is placed at the start of the RF system receiver to reduce the overall noise figure of the entire system. Recent research has focused on obtaining optimally de- signed LNAs in terms of noise figure as the lowest possible and linearity as the maximum possible. Thus, to minimize the noise figure, the paper proposes the conventional source inductive degeneration technique. Before designing the LNA,a compromise between the noise figure and gain must be made and designed accordingly. To ensure maximum power transfer in the circuit topology, input and output matching of the LNA is a primary requirement. The 50-ohm matching at the input and output is necessary. The matching network transforms the impedance up, giving gain (voltage gain) which helps suppress noise in the circuit.

IEEE 802.11 is a set of LAN technical standards that specify MAC and PHY protocols for implementing WLAN computer communication. IEEE 802.11ax, officially marketed by the Wi-Fi Alliance as Wi-Fi 6 (2.4 GHz and 5 GHz) and Wi-Fi 6E (6 GHz), is an IEEE standard for wireless local-area networks (WLANs) and the successor of 802.11ac. It is also known as high-efficiency Wi-Fi, improving the overall performance of Wi-Fi 6 clients in dense environments. The standard is designed to operate in license-exempt bands between 1 and 7.125 GHz, including the 2.4 and 5 GHz bands already in common use, as well as the much wider 6 GHz band (e.g., 5.925–7.125 GHz in the US, a band 1.200 GHz wide).

II. RELATED WORK

The Internet of Things (IoT) revolution has significantly changed wireless communication. Issues and obstacles are removed by advances in wireless communication technology which promote the creation of low-power high-performance LNAs. LNAs are the noise-selecting element in the RF receiver that enhances the intended signal while suppressing noise. The objective is to achieve the lowest noise and maximum gain for the receiver's performance. In order to improve gain performance while lowering the noise figure (NF), a low-power LNA operating at 5 GHz is the main topic of this work. To reduce power loss, further methods include forward-body bias and current reuse. The 5 GHz bands are currently used by Wi-Fi standards and this paper is built to operate at this frequency. In recent years, a large number of CMOS LNA circuits have been presented with an emphasis on reducing power consumption, improving gain performance,

and reducing NF. These objectives have been accomplished by using a capacitive coupling topology. The creation of next-generation wireless communication systems for the IoT age is made possible by the considerable developments in low-power LNA design. Designing LNAs for high-performance wireless communication systems comes with a number of difficulties. Low-power LNAs have been created as a result of technological breakthroughs and they offer a practical alternative for the construction of high-performance wireless communication systems. The development of RF receivers that can achieve optimal performance while using little power depends on the research being done in this area.

LNAs are essential parts of the wireless network and mobile device reception chain, and they must be continually enhanced to meet evolving performance criteria. The creation of high- speed communication networks with dependable quality has become necessary due to the considerable rise of the 802.11 family of standards, which includes the well-known Wi-Fi (Wireless Fidelity) protocol. The choice of transistor is critical for constructing LNAs for these applications and should have a low noise level, such as GaAs or GaN field effect transistors. Since it affects variables like bandwidth range, gain, noise levels, power dissipation, and chip size, choosing the right architecture is crucial. In this article, we outline the design of a planar LNA for 2.4 GHz wireless utilizing an RF4 substrate. The transistor selection and bias point, LNA theory, and design approach are covered in the study. The electromagnetic simulation results of the 2.4 GHz layout are then explained and compared to earlier studies.

III. LNA DESIGN

This section provides a detailed account of the design process for a low-noise amplifier (LNA) optimized for WLAN IEEE 802.11ax standards using ADS software. The design methodology and techniques employed are described in a clear and concise manner.

A. Choosing of Transistor

The Hewlett-Packard-recommended transistor ATF-13136, which meets the criteria for wireless applications, will be used in the LNA's design. Within the frequency range of 2 GHz to 16 GHz, this gallium arsenide Schottky barrier gate field effect transistor can generate a maximum noise of 1.4 dB and a minimum gain of 6 dB. The equivalent circuit for small-signal operation of the transistor, which is contained in a low-cost microstrip package, is shown in figure 2.

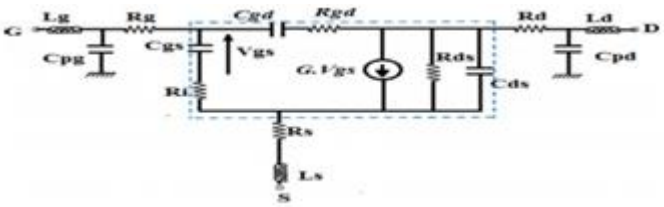

Fig. 1. Small Signal Equivalent Circuit of the GaAs FET

B. Q point selection and DC biasing of the GaAs FET

The GaAs FET is operated as a class A amplifier with a Q point of operation set at V_{DS} = 2.5 V, I_{DS} = 24 mA,

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S^* \Delta| + |S_{21}S_{12}|} > 1 \quad (3)$$

and V_{GS} = −0.3 V to provide the best performance. The FET tracer curve was used to determine this Q point. The amplifier's I_{DS} needs to be set to half of its I_{DSS} in order to function as a class A amplifier.

In order to assure effective performance, the DC biasing circuit of the GaAs FET is built utilizing a resistor negative feedback technique rather than a voltage divider bias which uses more resistors and produces lossy elements. Achieving the correct Q point is confirmed by the DC simulation of the circuit in Figure 3.

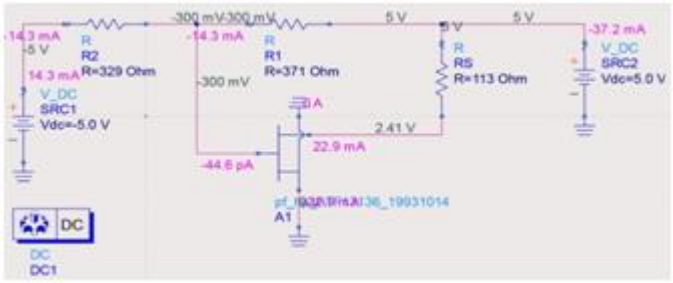

Fig. 2. DC Simulation of the DC Bias Circuit

C. Stability Network Design and Noise Optimization

In the context of the ATF-13136 GaAs FET, achieving unconditional stability is a critical component of the stability network design. To ensure that the RF amplifier circuit stays stable under all operational circumstances, such as changes in component values, temperature, and input/output impedance mismatches, unconditional stability must be attained. Failure to establish unconditional stability can lead to oscillation, poor amplifier performance, or even circuit damage. To achieve unconditional stability, shunt and series impedances are in- corporated into the gate and drain terminals of the GaAs FET as illustrated in figure 5. Equations 2, 3, and 4 outline the conditions required for unconditional

stability, which must be met to guarantee steady amplifier performance.

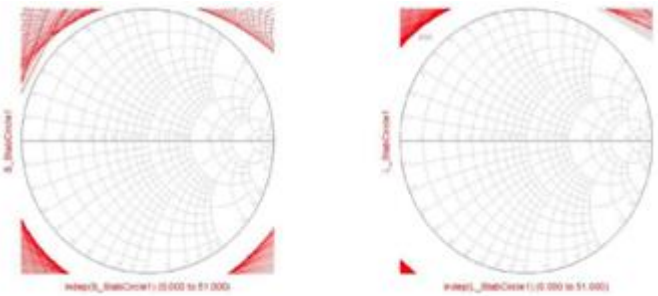

Fig. 3. Source and Load Stability Circles

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1 \quad (1)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (2)$$

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^{*}\Delta| + |S_{12}S_{21}|} > 1 \quad (3)$$

The term ”noise optimization using source inductive degen- eration” refers to a technique for RF amplifier noise reduc- tion that involves connecting an inductor in series with the amplifier transistor’s source (see figure 5). The inductor, also referred to as a degeneration inductor, raises the transistor’s source impedance, which aids in lowering the amplifier’s input noise. When designing low-noise amplifiers (LNAs) for wireless communication systems, where low noise is essential for optimum system performance, this approach is frequently utilised. The noise figure of the amplifier can be reduced while retaining the necessary degree of gain and stability by adjusting the value of the degeneration inductor.

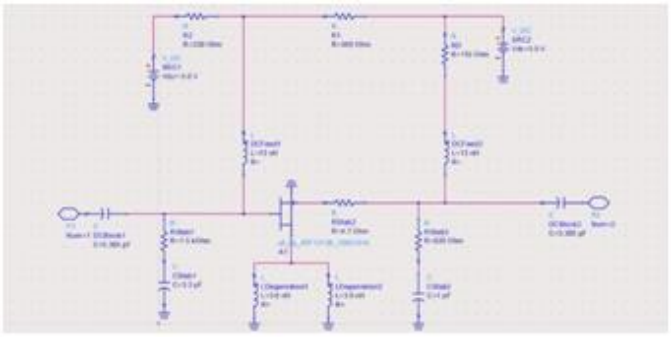

Fig. 4. Stability Network and Noise Optimized Circuit of a Basic Amplifier

D. Design of a Minimum Noise Amplifier and Maximum Gain Amplifier

The design of a three-stage LNA for WLAN IEEE 802.11ax standards is described in this research paper. The third stage is intended for maximum gain amplification (MGA) whereas the preceding two stages are intended to produce minimum noise amplification (MNA). Using the matching conditions shown in Figure 6, impedance matching circuits are designed for input, output, and interstage impedance matching network design. The methods used to calculate the matching conditions are depicted in Figures 7 and 8. The impedance matching circuit is initially designed with ideal transmission lines, but the LineCalc tool eventually replaces these with real microstrip lines. The substrate chosen for the synthesis of the microstrip lines is the frequently used RO4350B.

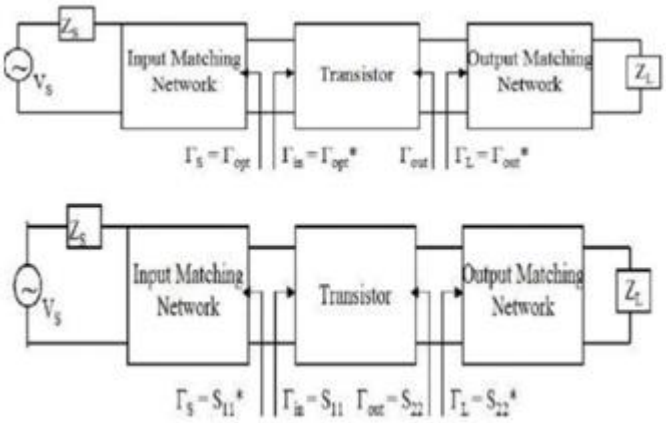

Fig. 5. Matching Network Design Conditions

IV. FINAL LNA

The final design of the LNA is obtained by combining the three stages of amplifiers. The first two stages are designed for MNA while the third stage is designed for MGA. The block diagram of the final LNA is illustrated in Figure 9 and the overall circuit diagram is presented in Figure 10. For

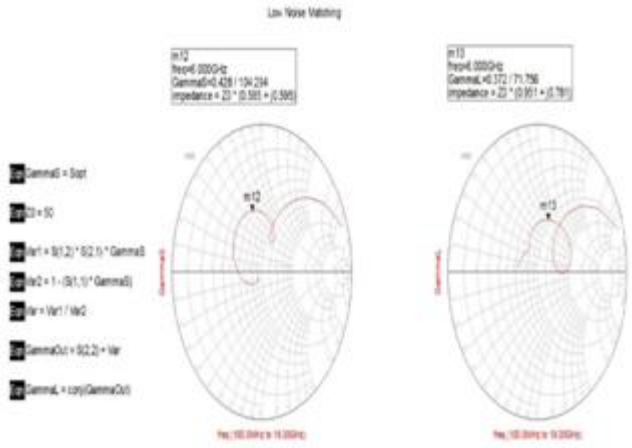

Fig. 6. Low Noise Matching (MNA Design)

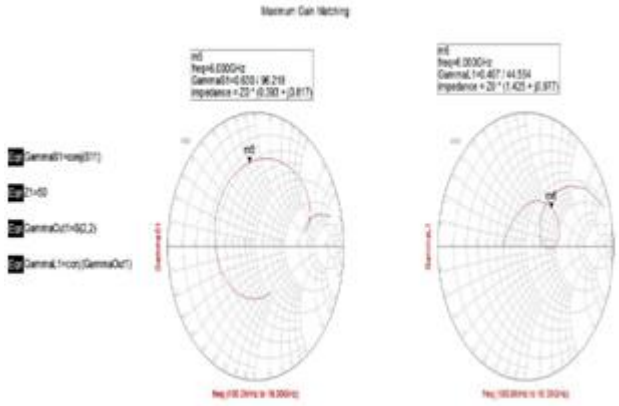

Fig. 7. Maximum Gain Matching (MGA Design)

practical implementation, ideal transmission lines in the design are substituted with microstrip lines which form the input, intermediate, and output matching networks of the final LNA.

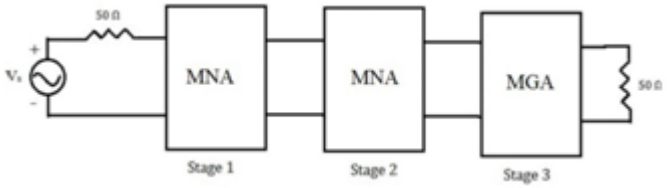

Fig. 8. Block Diagram of the Proposed LNA

V. SIMULATION RESULTS

The proposed low power LNA for 6-GHz band WLAN IEEE 802.11ax applications has been designed using Agilent's ADS software. The LNA utilizes an ATF-13136 GaAs FET and has a drain and gate bias of 2.41 V and -0.3 V respectively, drawing a current of 22.9 mA from a 5 V supply voltage. The power dissipation (Pdc) of the LNA is 59 mW. Simulated results of the LNA are presented in Figures 10-14. The ADS software was used for optimization and simulation of the circuit design.

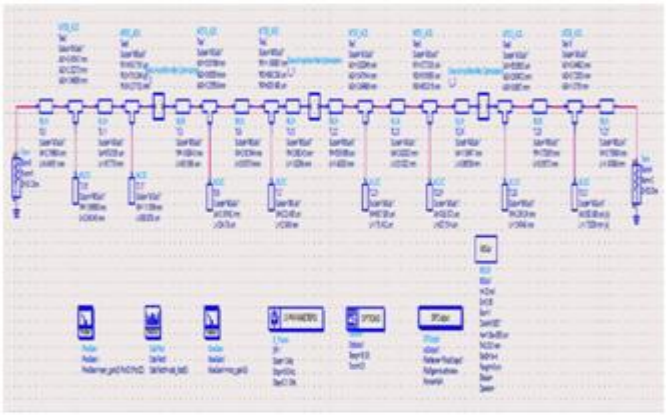

Fig. 9. Final LNA

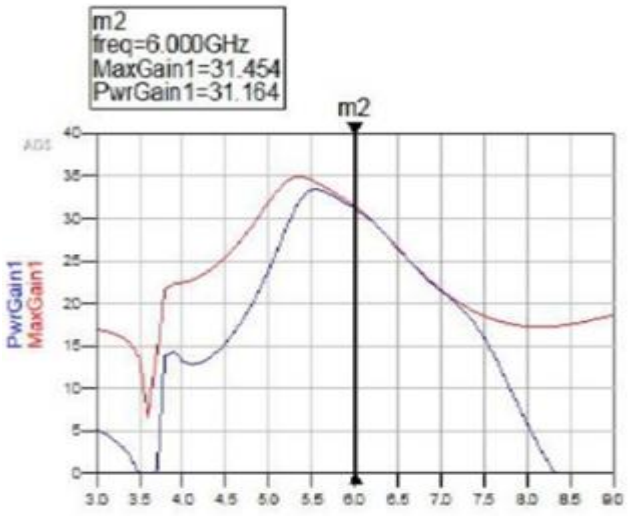

Fig. 10. Power Gain and Voltage Gain

The simulation results presented in this paper reveal that the designed LNA exhibits a maximum gain of approximately 31 dB and a noise figure of around 1.042 dB over the frequency range of 5.9 to 7.2 GHz as evidenced by Figures 10 and 12. Since the noise figure of the LNA is a critical factor in determining the overall noise figure of the RF system, these results indicate that the LNA provides an exceptionally low noise figure for the entire RF system. Furthermore, Figure 11 shows that the input and output reflection coefficients are approximately -15 dB which indicates that the LNA is well matched. This conclusion is reinforced by the data in Figure 14 which shows that the S11 and S22 parameters are close to the unity point of 1 indicating that the overall LNA is well matched. These results suggest that the designed LNA provides superior performance characteristics which are

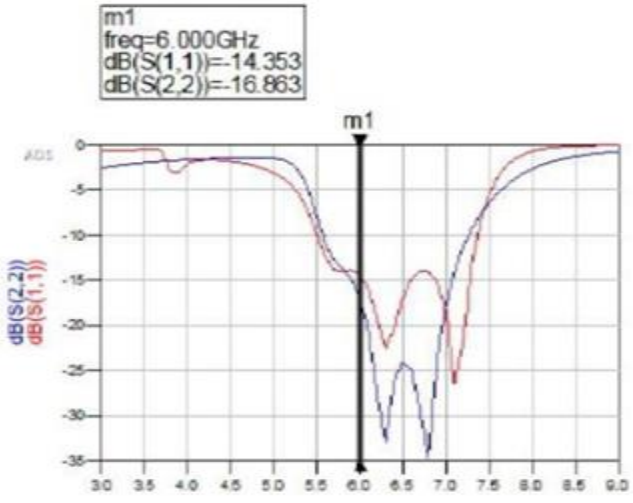

Fig. 11. Input and Output Reflection Coefficient

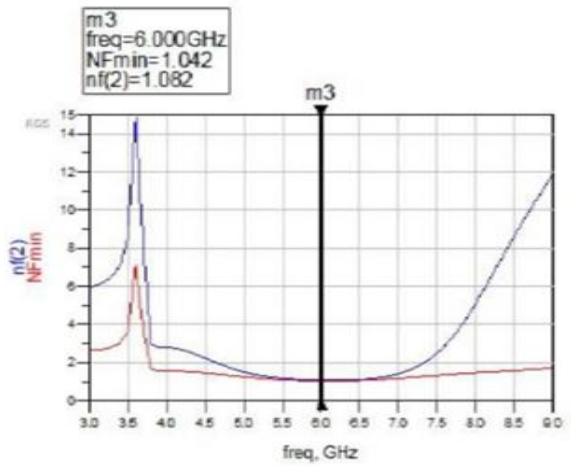

Fig. 12. Noise Figure

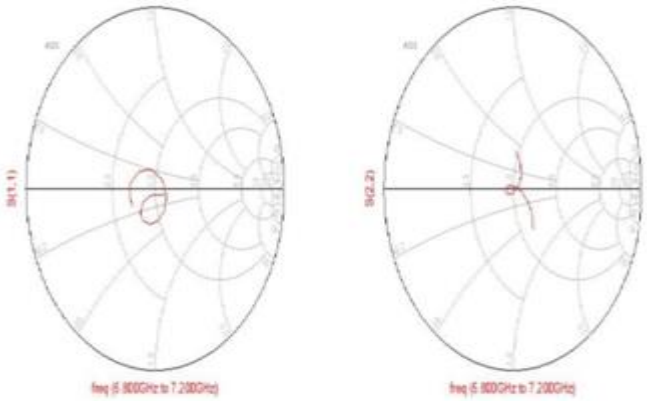

Fig. 13. Input and Output Reflection Coefficients in the Smith Chart

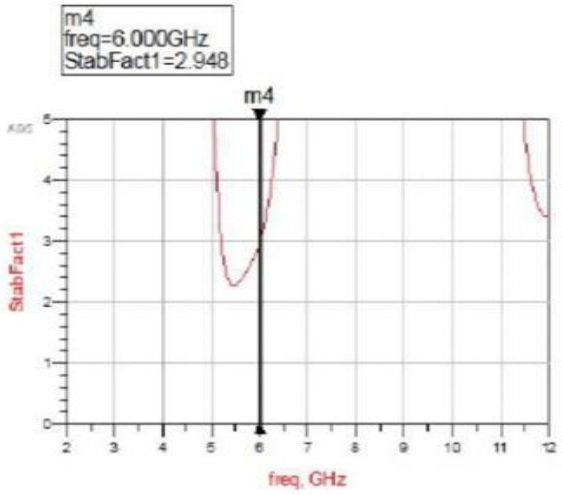

Fig. 14. Stability Factor K

essential for 6-GHz band WLAN IEEE 802.11ax applications.

VI. CONCLUSION

This project presents the development of a three-stage low-noise amplifier (LNA) for WLAN IEEE 802.11ax. The active device, the ATF-13136 transistor, was selected among more than 20 manufacturers and the ideal bias circuit, input matching network, output network, and inter-stage network were sequentially designed and added to the transistor. The practical LNA was then developed based on the ideal design after tuning and optimization. The final LNA has a maximum gain of 31.54 dB, noise figure less of 1.042 dB, and output return loss of -16.86 dB in the frequency band of 5.9-7.2 GHz. Microstrip lines were used to replace the transmission line and the frequency range was expanded from the central frequency to the design goal band.

TABLE I Simulated Result

Parameter	Result Achieved
Maximum Gain	31.45 dB
Power Gain Noise Figure	31.16 dB
Input Reflection Coefficient	1.042 dB
(S11) Output Reflection	-14.35 dB
Coefficient (S22) Power	-16.86 dB
Consumption	59 mW
VDS (Drain to Source Voltage)	2.41 V
VGS (Gate to Source Voltage)	-0.3 V
IDS (Drain to Source Current)	22.9 mA

TABLE II Performance Comparison with Recent Papers

Specification	[1]	[2]
Year of Publication	2022	2019
Transistor Process Technology	CMOS 180 nm TSMC	GaAs FET (ATF-21170)
Frequency of Operation	1.57 dB (L1 band)	2.4 GHz
Bandwidth	NA	NA
Maximum Gain	23.89 dB	15.11 dB
Noise Figure	1.77 dB	0.37 dB
Input Reflection Coefficient (S11)	NA	-15.8 dB
Output Reflection Coefficient (S22)	NA	-15.8 dB
Power Consumption	6.543 mW	NA
Operating Voltage	1.2 V	NA

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