Variability Aware Design Of Full Adder

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Abstract- *Under Ultra-deep sub-micron technology node as there is continues reduction in the feature size to few nanometers will results adverse effect of Process, Voltage and temperature (PVT) variations on design metrics of circuit. Hence it is proposed that how to mitigate the effect Variability on design metrics of a Full Adder Circuit. It can be achieved by using Schmitt trigger inverter sub-Circuit instead of normal Inverter in CMOS Full Adder and dynamic body-bias technique is applied through a feedback mechanism to the low voltage Schmitt trigger to operate it in near threshold region.*

I. INTRODUCTION

As modern digital circuits are facing aggressive technology and voltage scaling under emerging technology generations. It makes a very sharp reduction in size of CMOS to 16-nm under ultra-deep sub-micron technology nodes and hence integration capacity increase which intern increase the processing speed. But in resent era there is requirement of design battery operated device. i.e the designed device mute be a high speed and it must be operate with low power. Hence process, voltage and temperature are considered as design metric and variability in this metrics are significant in high scaling node. Variability in this metrics has equal importance.

Due to the advancement in the VLSI technology integration capacity increases drastically. Which intern increase the processing speed at the cast of power dissipation in ICs and also increases the heat dissipation in the IC. One solution to minimize power dissipation and heat dissipation is that reduce the supply voltage i.e there is requirement of low power devices. Which intern reduces the threshold voltage required and hence noise sensitivity of transistor increase. That is noise margin of the low power digital circuit is poor.

As there is continuous growth of recent mobile and portable devices and applications has caused a tremendous thrust for low power circuit design. Although the sub-threshold region of transistor operation is extremely energy-efficient, offering ultra-low power dissipation, it has remained limited to few market places because of its major performance penalty. The near-threshold region (NTR), where the supply voltage is approximately equal to or in the range of the threshold voltage of the transistors used, instead retains much of the energy savings of sub-threshold operation with substantial performance and variability improvement.

The variability in the design metrics can be minimized by using a low voltage Schmitt trigger in place of conventional CMOS inverter and a dynamic body-bias technique is applied through a feedback mechanism to the low voltage Schmitt trigger to operate it in near threshold region.

VLSI is often abbreviated as Very large scale integration. The electronic industry has been achieved a phenomenal growth for the past last two decades because of the rapid advances in integration technologies, very large-scale system design in short, due to the advances of VLSI. Further, the required computational power or, in another terms, the intelligence of these applications is the one and only force for the rapid development of field. The present leading edge of the technology is low bit rate for video and cellular communication that provides the users an certain amount of processing power and portability.

During the 1st half of the 20thcentury, electronic circuits are large, power-hungry, economical and unreliable because of use of vacuum tubes. John Bardeen and Walter Brattain built the 1stfunctioning point contact transistor at Bell Laboratories in 1947.At that time it became a military secret, but Bell Labs publicly introduced the device Transistor. They called it as transistor because it is a Trans- resistive device which transfers resistance from input to output terminals and also act as amplifier.

Transistor is a semiconductor device which can amplify and transfer electrical signals through it from i/p to o/p terminals. It has no filament, no vacuum, and no glass tube. It is composed entirely of cold, solid substances.

Transistors can be viewed as electrically controlled switches with a control terminal and two other terminals that are connected / disconnected depending on the applied voltage or current to its control terminals. Soon after inventing the

point contact transistor, Bell Labs developed BJT. Bipolar devices are more reliable, noise immune, more power-efficient and speedy. Early IC designs primarily used BJTs. Bipolar transistors require small currents to base terminal to switch larger currents b/w emitter and collector terminals. As transistor dissipates quiescent power by base currents, drawn even when the circuit is not switching, limits the integration of maximum no. of transistors integrated on a single die. By1960 onwards, MOS Transistors began to enter production. MOS Transistor offers almost zero current when idle. They come in two flavors: NMOS and PMOS respectively. The original idea of field effect transistors dated back to the German scientist - Julius Lilienfield in 1925 and a structure closely resembling the MOSFET was proposed in 1935 by Oskar Heil, but materials problems foiled early attempts to make functioning devices. But nowadays there is need of battery operated portable design devices with high-performance at much lower power. It can be achieved by combining PMOS and NMOS in device called Complementary metal oxide semiconductor (CMOS).

In 1965, Gordon Moore observed that plotting the no. of transistors that are most economically manufactured on a chip gives a straight line on a semi logarithmic scale. At the time, he found, transistor count is doubling for everyone and half year. This observation has been called as Moore's Law which becomes a self-fulfilling prophecy. Figure 1.1 shows no. of transistors integrated in IC. Moore's Law is driven primarily by scaling down the size of transistors and, to a minor extent, by building larger chips. Level of integration of chips has been classified as SSI, MSI, LSI, VLSI and ULSI.

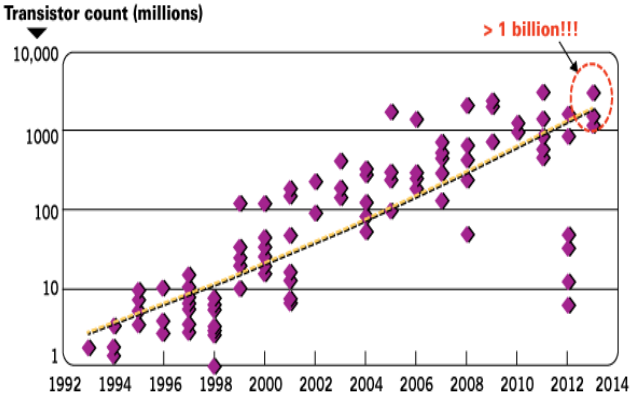


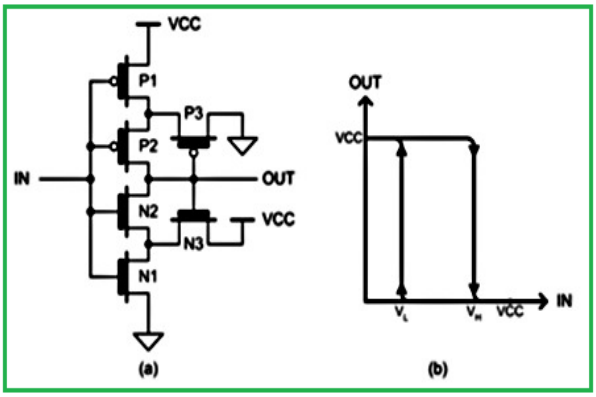
Figure 1.1: Transistors integration capacity.

Small-scale integration (SSI) circuits have less than 100 transistors i.e nearly 10 Gates, with roughly six transistors per Gate. Medium scale integration (MSI) circuits contain less than 500 transistors i.e nearly 100 Gates. Large-scale integration circuits contain few thousands of transistors and integrated more than 100 Gate. It soon became apparent that new names have to be created for every 5 years. If this naming trend continues, the term VLSI is used to describe most integrated circuits from 1980s onward. Anidea of Moore's law is Dennard's Scaling Law: as transistors shrink, they become faster, consume less power, and are cheaper to manufacture. Computer performance, measured in time to run an application, has advanced even more than raw clock speed. Presently, the performance is driven by the number of cores on a chip rather than by the clock. Power consumption is the major factor in case of integrated design as it consists of more transistors which will consume enormous power, even though a single transistor consumes less power. Moreover, as transistors have become so small, they cease to turn completely OFF. Small amounts of current leaking through each transistor now lead to significant power consumption when multiplied by millions or billions of transistors on a chip.

Moore's Law has become a self-fulfilling prophecy because each company must keep up with its competitors. Moreover that scaling can`t go on forever because transistors cannot be sized smaller than atoms. Den nard scaling has already begun to slow. By the 45 nm generation, designers are have to make trade-offs between improving power and improving delay. Although the cost of printing each transistor goes down, the one-time design costs are increasing exponentially, relegating state-of-the-art processes to chips that will sell in huge quantities or that have cutting-edge performance requirements. However, many predictions of scaling have already proven wrong. In early 1990s, experts agreed that scaling would continue for at least a decade but beyond that point future was dark.

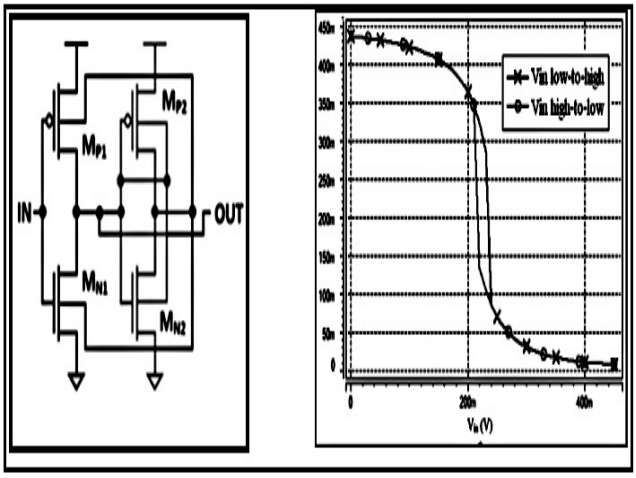
II. EXISTING SCHMITT TRIGGER(6T)

This circuit exhibits different threshold voltages V_{thl} and V_{tlh}i.e when input is switching from high-to-low and low-to-high transition in an inverting configuration



Proposed Low Power Schmitt trigger:

Hence it is proposed that a novel 4T Low power Schmitt trigger with dynamic body biasing (to operate ST in Near Threshold Region) as shown in below figure.

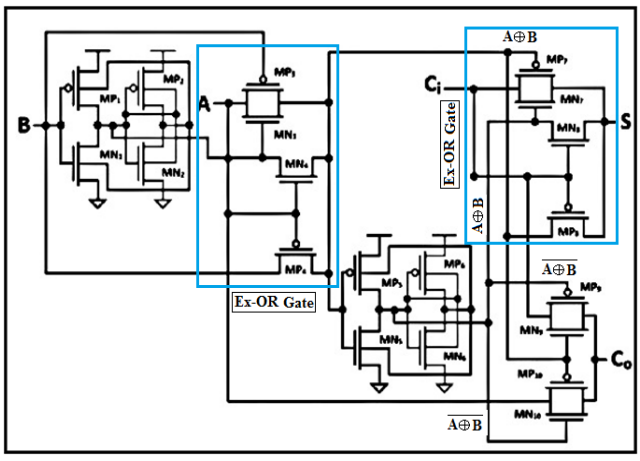


This Low Power Schmitt trigger is incorporated in the design of Full Adders of different topologies in place of inverter to mitigate effect of variability in the design metrics.

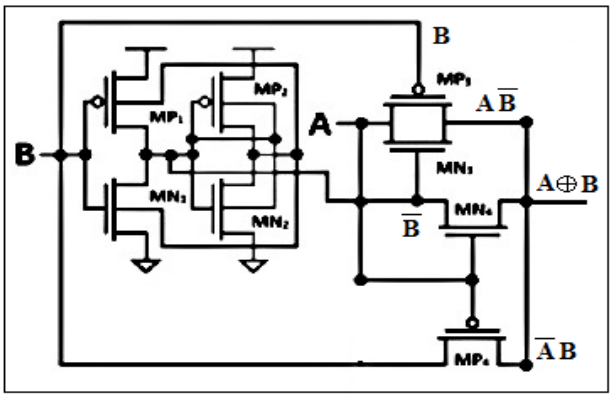
III. METHODOLOGY FOR PROPOSED FULL ADDERS

- Transmission Function Schmitt Trigger Full Adder (TFSTFA).
- Transmission Gate Schmitt Trigger Full Adder (TGSTFA).
- Transmission Gate drivcap Schmitt Trigger Full Adder (TG drivcap STFA).
- Hybrid Schmitt Trigger Full Adder(Hybrid STFA).

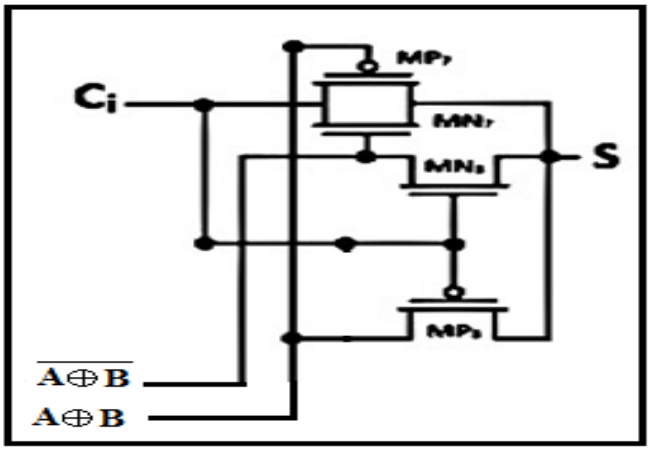
TFSTFA Circuit :



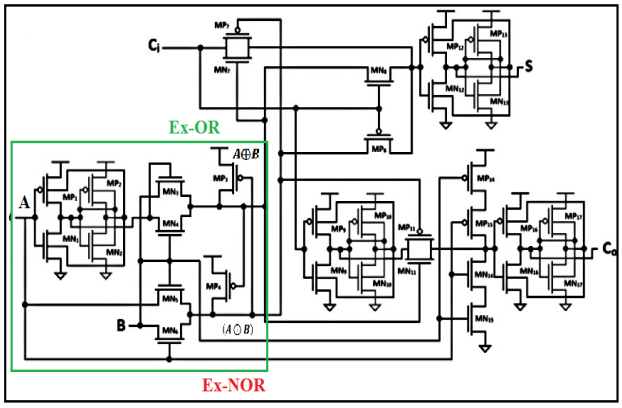
Basic Ex-OR Gate used :



Sum Generating Circuit :



Hybrid Schmitt Trigger Full Adder

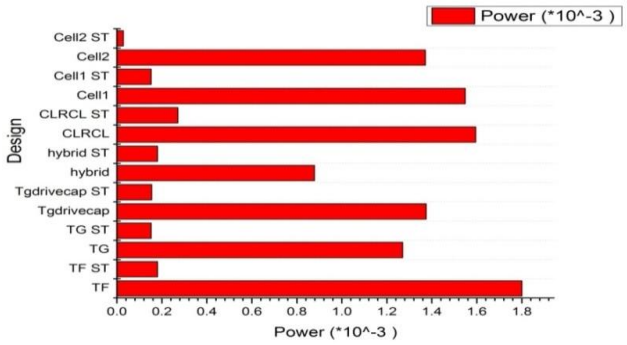


IV. RESULT

- To compare the performance of the original and proposed cells, for the three design metrics, power dissipation (P_{avg}), propagation delay (t_p) and PDP, by running Monte Carlo simulations for the above device

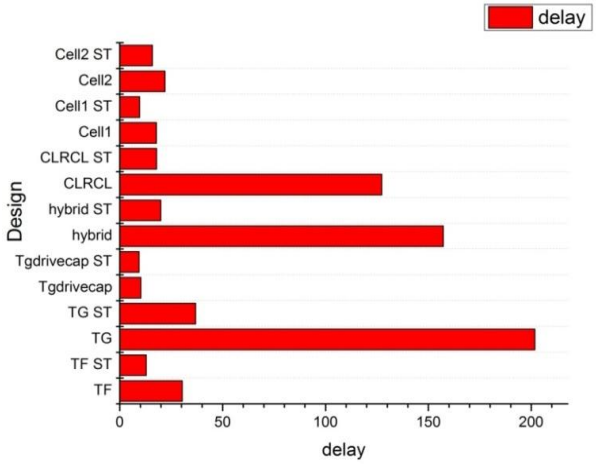
- Standard deviation (σ) is used the measure of dispersion in this design metrics.
- Variability is then defined as the ratio of the standard deviation (σ) to the mean value (μ) of specified design metrics.

Comparison bar chat graph for power of different FA design :



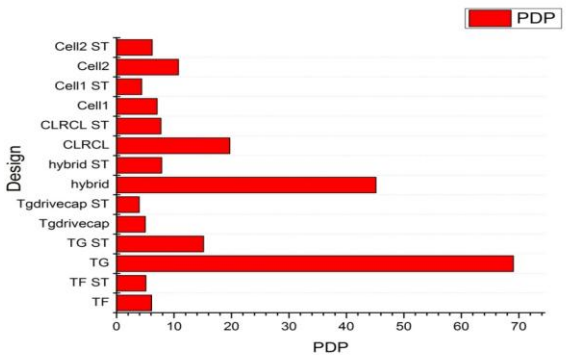
From the above bar chat it is observer that for all Full Adder topologies variability in Power can be minimized by replacing CMOS inverter with Low Power Schmitt Trigger.

Comparison bar chat graph for delay of different FA design



From the above bar chat it is observer that for all Full Adder topologies variability in delay can be minimized by replacing CMOS inverter with Low Power Schmitt Trigger.

Comparison bar chat graph for PDP of different Full Adders design



From the above bar chat it is observer that for all Full Adder topologies variability in PDP can be minimized by replacing CMOS inverter with Low Power Schmitt Trigger.

V. CONCLUSION

- Hence it can conclude that, the FA designed with low voltage Schmitt trigger sub-circuits, exhibits significantly improve over variability in power, delay and PDP and gives more robust circuits.
- Even though improvement is active in variability of design metrics, CMOS devices are preferred if area is considered as design metric.
- But if the cost of extra transistors are tolerable proposed design may achieves significant improvement in variability.

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