Efficient CNTFET-Based Ternary Full Adder Cells For Nanoelectronics

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Abstract- *This paper presents two new efficient ternary Full Adder cells for nano-electronics. These based on the unique characteristics of the CNTFET device, such as the capability of setting the desired threshold voltages by adopting proper diameters for the nano tubes as well as the same carrier mobilities for the N-type and P-type devices. These characteristics of CNTFETs make them very suitable for designing high-performance multiple- Vth structures. The proposed structures reduce the number of the transistors considerably and have very high driving capability. The presented ternary Full Adders are simulated using Synopsys HSPICE with 32 nm CNTFET technology to evaluate their performance and to confirm their correct operation.*

Keywords- CNTFET; Multiple-Valued logic; Ternary logic;Ternary Full Adder; Multiple- Vth design

I. INTRODUCTION

As the predominant technology, the complementary metal oxide semiconductor (CMOS) process offers the necessary size scaling for the implementation of high-performance, low-power, and high-density VLSI circuits and systems. However, because the dimensions of MOS transistors must be reduced to a lower nanoscale, this technology faces numerous significant obstacles and problems.In order to mitigate these challenges, a number of non-CMOS nanodevices, including Quantum-dot Cellular Automata (QCA), Carbon Nanotube Field Effect Transistor (CNTFET), Single Electron Transistor (SET), and Graphene Nano-ribbon Transistor (GNRT), have been suggested as potential substitutes for conventional bulk CMOS in the near future.

Transistors and Technology Scaling: VLSI technology heavily relies on transistors since they are fundamental parts of electronic circuits. Technological advancements lead to technology scaling, or the gradual shrinkage of transistor size over time. This scaling allows for the integration of more transistors into a single chip, improving functionality and performance.

Levels of Design: VLSI design occurs at different levels of abstraction, including:
Level of Logic Gates: Transistors are combined at this level.

Transistor Level: This describes how individual transistors are made and how they are connected to one another.

Logic Gates Level: In this level, transistors are assembled to create logic gates and other fundamental digital building blocks.

Level of Functional Blocks: consists of creating larger functional blocks, such as adders, multiplexers, and memory units.

System Level: Assembles several functional parts to create a complete system.

Furthermore, there are similarities between the MOSFET and CNTFET devices' current-voltage (I-V) properties. Similar to MOSFET, CNTFET also has P-type and N-type devices. But in contrast to the MOSFET In contrast to binary logic, more than two logic levels are allowed in MVL systems, and more than two approved logic values may be used for arithmetic and logical operations. As a result, many arithmetic and logical operations might be performed faster and with fewer computing steps by utilising MVL. Pin-out and connector issues, which restrict the number of connections both inside and outside of the circuits, are the primary hurdles faced by binary logic designers when creating big, dense chips.

APPLICATIONS:

1.High-Performance Computing (HPC):CNTFETs have the potential to revolutionize HPC systems by enabling faster and more energy-efficient processors. Their superior electrical properties allow for faster switching speeds and lower power consumption, making them ideal candidates for next-generation CPUs and GPUs.

2.Flexible Electronics: CNTFETs can be integrated into flexible substrates, enabling the development of bendable and stretchable electronic devices. This opens up possibilities for applications such as flexible displays, wearable electronics, and conformable sensors.

3.Biomedical Devices:CNTFETs can be used in biomedical applications such as biosensors and neural interfaces. Their high sensitivity and low noise characteristics make them suitable for detecting biomolecules and interfacing with biological systems, leading to advancements in healthcare diagnostics and neural prosthetics.

4.Energy Harvesting and Storage:CNTFETs can be utilized in energy harvesting and storage devices such as solar cells, thermoelectric generators, and supercapacitors. Their high carrier mobility and low energy consumption make them well-suited for converting and storing energy from various sources efficiently.

5.Internet of Things (IoT) Devices:CNTFETs can play a crucial role in IoT devices by enabling low-power, high-performance electronics. Their ability to operate at low voltages and consume minimal power makes them ideal for sensors, actuators, and other IoT components deployed in energy-constrained environments.

II. EXISTING METHODS

The acronym for complementary metal-oxide-semiconductor, or CMOS, refers to technology. This kind of technology is employed in the production of memory chips, CPUs for computers, and other electronic gadgets. With the employment of metal, oxide, and semiconductor materials, CMOS technology produces incredibly dependable and low-power electronic circuits.

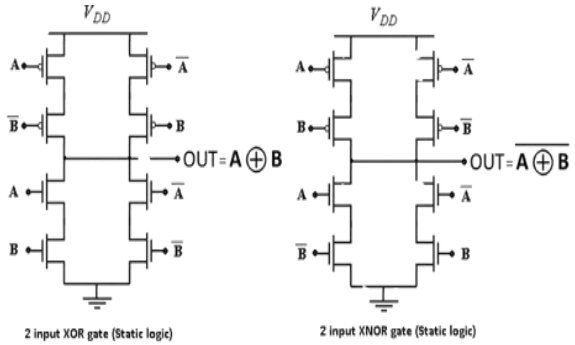


Fig.3: The circuit diagram for 2-input NAND, NOR, XOR and XNOR gates in CMOS static logic.

Transmission gate: A transmission gate (TG) is an analogue gate that works similarly to a relay. It can conduct in both directions and can be stopped by a control signal at almost any voltage potential. The CMOS technology used in this switch allows NMOS to pass a strong 0 but a weak 1 and PMOS to pass a strong 1 but a poor 0. NMOS and PMOS function simultaneously. Essentially, two field-effect transistors (FETs) with the substrate terminal in between make up a transmission gate.

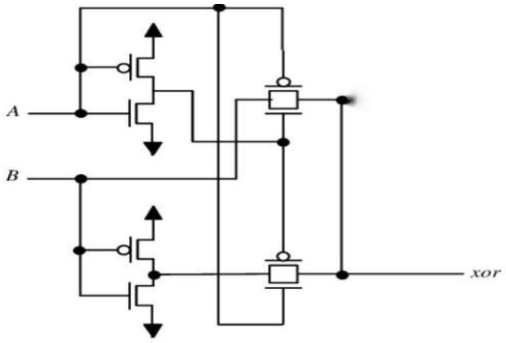


Fig 3: XOR circuit using transmission gates

Complementary Pass-transistor Logic (CPTL): A distinct circuit technique called Complementary Pass-transistor Logic (CPTL) can greatly lower the complexity of full-CMOS pass-gate logic circuits. substituting a nMOS pass-transistor network for a CMOS for the logic operations. The core idea of CPL is the TG network. All input signals need to be provided, along with their inverse. Moreover, the circuit produces complementary outputs that are used by subsequent CPL stages. Every feedback is used in a complimentary manner. Thus, the fundamental parts of the CPL circuit consist of complementary inputs, a nMOS pass transistor logic network to generate complementary outputs, and CMOS output inverters to restore the output signals.

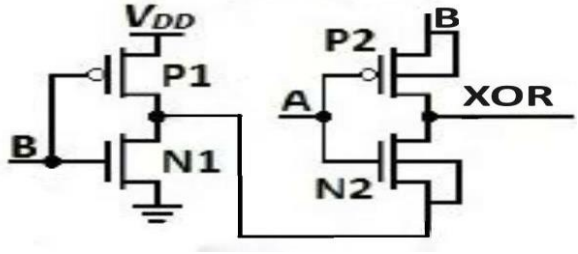


Fig 4,5: The XNOR and XOR circuits using complementary pass transistor logic.

TERNARY LOGIC:

Ternary logic, also known as three-valued logic, is a system of logic that extends traditional binary logic (which has two possible values: 0 and 1) to include a third value. In ternary logic, there are three possible logical states: true (T), false (F), and an additional third state, often represented as unknown, undefined, or indeterminate (U).

The inclusion of this third logical state allows for more nuanced and flexible reasoning and computation. Ternary logic finds applications in various fields, including computer science, electronics, and artificial intelligence. Some potential advantages of ternary logic include:

- Increased Information Density: Ternary logic allows for the representation of more information per digit compared to binary logic. This can lead to more efficient data storage and processing in certain applications.
- Improved Fault Tolerance: The additional logical state in ternary logic can enhance fault tolerance in digital systems by providing a mechanism to represent and handle uncertain or ambiguous information.
- Reduced Complexity: In certain cases, ternary logic can lead to simpler and more compact circuit designs compared to equivalent binary logic implementations. This can result in reduced hardware complexity and improved efficiency.
- Enhanced Computational Power: Ternary logic can enable the development of computational systems with increased expressive power and computational efficiency, particularly in tasks that involve handling uncertain or probabilistic information.

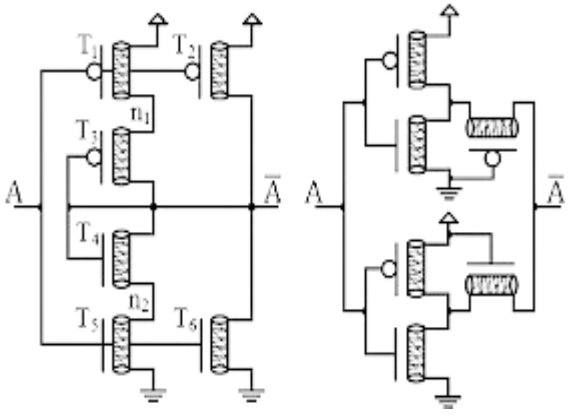


Fig6:ternary logic basic cell

III. PROPOSED TECHNOLOGY

CNTFET: A carbon nanotube field-effect transistor (CNTFET) employs a single carbon nanotube (CNT) or an array of carbon nanotubes as the channel material as opposed to bulk silicon, as in the traditional MOSFET architecture. Considerable progress has been made since the first demonstration of CNTFETs in 1998. The different work functions of the metal and the CNT result in the Schottky barrier at the source and drain of CNT–metal contacts, which are made up of metals like silver, titanium, palladium, and aluminium. Though, as with Schottky barrier diodes, the barriers would have restricted this FET to conveying a single kind of carrier, quantum mechanical tunnelling through the barrier dominates the carrier transport over the metal-CNT interface.

Based on the stated advantages and disadvantages of the various types of CNTFETs and also due to the more similarities between MOSFET-like CNTFETs and MOSFETs in terms of inherent characteristics and operation, this type of CNTFET is utilized fo rdesigning the proposed ternary Full Adder cells.

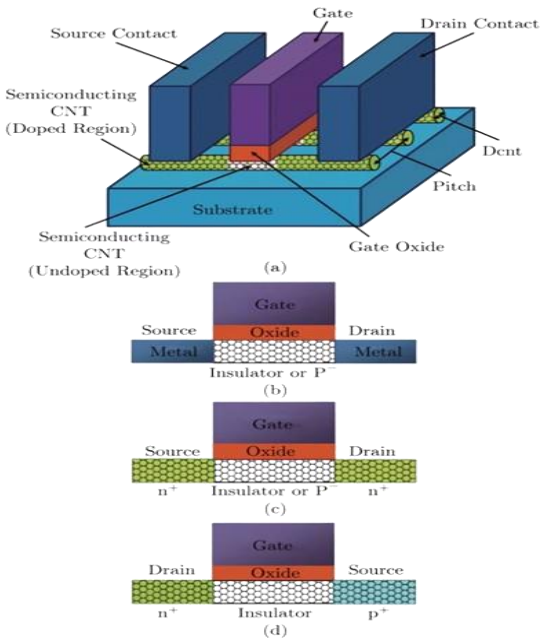


Fig7:(a)A typical CNTFET device; Different types of CNTFET device ,(b) SB-CNTFET © MOSFET-like CNT FET (d) T-CNTFET.

The Proposed Ternary Full Adder Cells:

One kind of MVL is ternary logic, which has three important logic values. These logical values are similar when represented as "0," "1," and "2." to voltage values of VDD, 1/2VDD, and 0. The 1-trit ternary Full Adder cell is the most fundamental ternary arithmetic circuit. A 1-trit ternary Full Adder cell's truth table with inputs A, B, Cin (input carry), Sum, and Cout

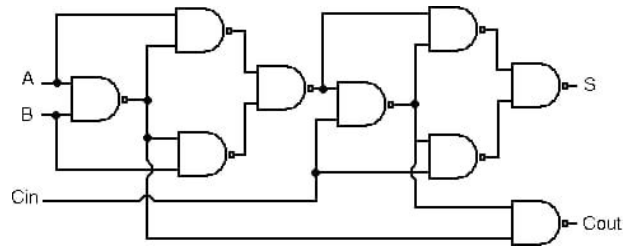


Fig8(A):Ternary NAND gate(Gate Level)

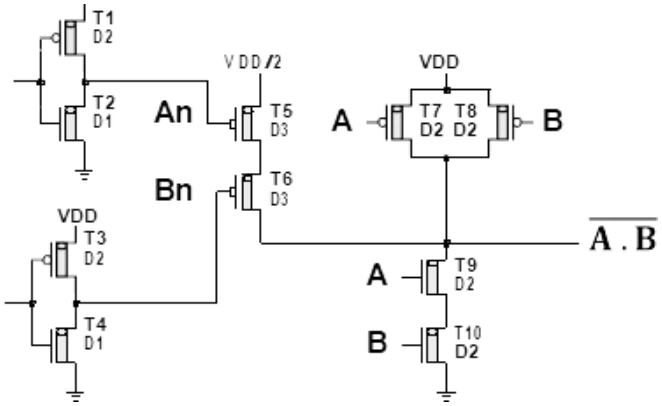


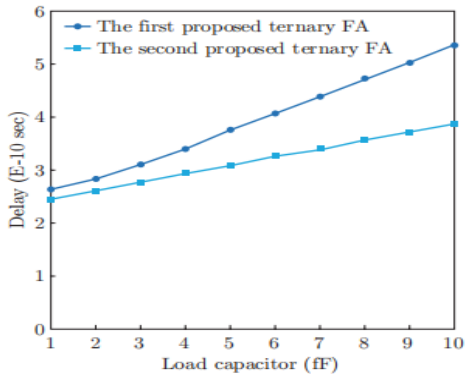
Fig8(B):Ternary NAND Transistor Level Diagram

PARAMETER	CMOS	TRANSMISSION GATE	CPTL	CNTFET
DELAY	4.996 e^{-10}	2.039e^{-12}	4.997 e^{-08}	2.6978e^{-05}
AV.POWER	5.022 e^{-04}	6.432e^{-04}	3.395 e^{-5}	1.610e^{-08}

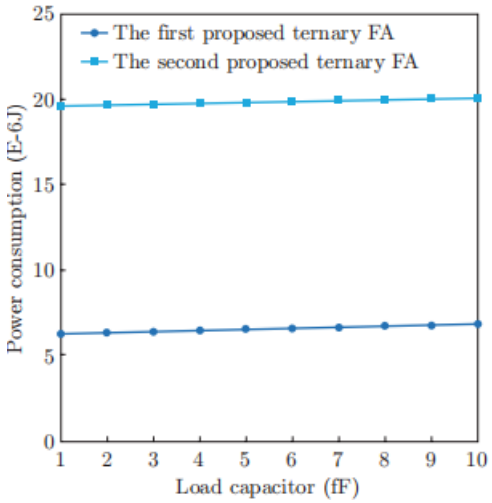
TABLE 1

NOTE:

To show how the Ternary Full Adder in transistor level will look, will be difficult here ,because it needs nearly 90+ CNTFET's to complete one full adder in that level.That's why we representation it in the form of T-NAND gate because the total full adder is created or designed by using NAND with CNTFET.



Delay of the designs versus load capacitors



Power consumption of the designs versus load capacitors.

IV. CONCLUSION

Innovative and effective ternary Complete On the basis of CNTFET devices, adder cells for nanotechnology have been proposed. The ternary Full Adder. A novel approach based on multi-Vth nanodevices has been used to develop adders, which have profited from the special qualities of CNTFET. The presented structures significantly reduce the number of transistors while having very good driving capabilities. These novel designs can be used as the foundation for larger, more intricate ternary arithmetic circuits. Using Synopsys HSPICE and 32nm CNTFET technology, the proposed ternary Full Adder cells have been simulated, validating their proper operation.

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