

Design and development of FPGA based Temperature and Light Intensity Measurement system using UART Protocol

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Abstract- In this, develop an efficient FPGA based temperature and Light intensity measurement system to reads the temperature and light intensity values through XADC using UART protocol and displays it on LCD updated to every second time period. The LM35 and LDR sensors are used as a temperature and light intensity sensors and are interfaced with the FPGA (ARTIX-7) manufactured by Xilinx. The output that is produced by the sensors is connected to the signal conditioning circuit, which convert the output into quantized voltage levels in order to send it as an input to an ADC. The necessary code is written in the hardware description language VHDL. Xilinx VIVADO suite is used for software development which is one of the EDA (Electronic Design Automation) tool offered by the Xilinx Company. The purpose of this project is to lower the power usage and continuously update the temperature and light intensity using a 28nm FPGA device.

Keywords- FPGA (ARTIX-7), ADC, UART serial communication protocol, LM35 and LDR sensors, LCD Display, VHDL language, Xilinx VIVADO

I. INTRODUCTION

Semiconductor devices known as Field Programmable Gate Arrays (FPGAs) are built around a matrix of customizable logic blocks (CLBs) coupled by programmable interconnects. FPGAs can be reprogrammed after production to satisfy certain feature or application requirements. FPGAs and Application Specific Integrated Circuits (ASICs), which are specially made circuits for particular design requirements, are differentiated by this property. While there are OTP FPGAs available, SRAM-based FPGAs are more common and can be reprogrammed as the design changes. FPGA, which stands for Field-Programmable Gate Array, is another way we may put it. This kind of integrated circuit (IC) allows for post-manufacturing configuration by the user or designer. In contrast to conventional application-specific integrated circuits (ASICs), which are created throughout the manufacturing process with a specific goal in mind.

Programmable read-only memory (PROMs) and programmable logic devices (PLDs) are two of the older devices that gave rise to the FPGA. These devices could be programmed in the field or at the factory, but once programmed, they could not be modified because they used fuse technology—Thus, the expression "burning a PROM." on contrast, the configuration data of an FPGA is stored on a reprogrammable medium such as static RAM (SRAM) or flash memory. Intel, Lattice Semiconductor, Microchip Technology, and Microsemi are among the companies that manufacture FPGAs.

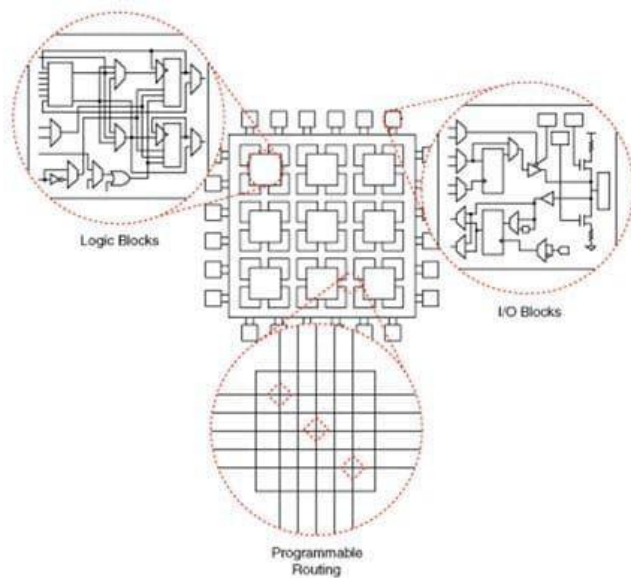
➤ Principle of FPGA:

An FPGA is essentially a passive component that may be designed to function as almost any type of digital circuit. Nothing physical changes in this situation, which is magical. The FPGA only has to have a configuration loaded for it to begin functioning like the desired circuit. No bother, no soldering, no jumper wires.

FPGA Architecture:

Configurable logic blocks (CLBs) are the building blocks of a basic FPGA design (Figure 1), which is made up of thousands of CLBs and a fabric—a system of programmable interconnects—that routes signals between CLBs. Interface blocks for input/output (I/O) allow the FPGA to communicate with external devices.

The CLB may alternatively be known as a logic block (LB), logic element (LE), or logic cell (LC), depending on the manufacturer.



FPGA: Basic Overview

A device with a matrix of reconfigurable gate array logic circuits is called an FPGA. An FPGA's internal circuitry is connected in such a way that it produces a hardware implementation of the software program when it is setup. FPGAs do not have an operating system and instead process logic using specialized hardware, unlike processors.

Because FPGAs are really parallel devices, several processing processes do not have to compete with one another for the same resources.

Uncommitted wires are used to route signals and a variety of logic modules form the foundation of FPGAs. The mask design used in the production of gate arrays connects these wires. As opposed to FPGAs, where the user connects these wires, these wires in FPGAs must be connected via an electronic device. The three most popular ways to accomplish this are through direct connects using antifuses, flash or EEPROM cells to carry the signal, or pass transistors operated by SRAM cells. The benefits and drawbacks of every one of these connectable devices vary. The design, architecture, and performance of the FPGA are significantly impacted by this. Here is a description of how FPGAs are categorized using user-programmable switches.

Anti-fuse Based: At first, every contact is open. Selected areas are converted to conduct through programming. This procedure can be programmed only once (OTP). Moreover, this technology does not utilize the conventional CMOS process and is non-volatile in nature.

➤ Logic Cells:

“Logic Cell” refers to the combination of a LUT and a storage component. A slice's capacity is increased by its extra characteristics, which include broad multiplexers, arithmetic gates, and logic. The whole slice is equal to 2.25 simple logic cells, according to benchmarks.

➤ Input/output Block (IOB):

A programmable, unidirectional or bidirectional interface between a package pin and the internal logic of the FPGA is provided by the input/output block (IOB), which supports a large range of standard interfaces. With dedicated double data rate (DDR) registers for computational or registered inputs and outputs, programmable input delays, on-chip termination, and hot-swap capability, this feature-rich set is highly reliable. The output path, input path, and 3-state path are the three primary signal paths found in the IOB.

FPGA (Field-Programmable Gate Arrays) and ASIC (Application-Specific Integrated Circuits) are the two methods used in chip development. ASICs can be very efficient in terms of design area, power, and speed, but they can also be quite resource- and time-intensive. Making a customized chip from the ground up could be costly and time-consuming. Therefore, if the targeted product was not needed in huge quantities, FPGAs would usually be a superior choice.

The EDGE Artix 7 FPGA Development board is an enhanced version of the EDGE Spartan 6. It was made just for the most recent version of the vivado Design Suite. The EDGE Artix 7 board is built around the Xilinx Artix 7 XC7A35T FPGA IC. A camera, TFT, switches, buttons, LED interface, Micro SD, HDMI Out, external memory, SDRAM, WIFI, Bluetooth, ADC, DAC, LCD, and seven segments are among the features. It is easy to construct the Micro Blaze softcore CPU design with SDRAM using the Vividado SDK.

Data Flow Procedure:

- The temperature sensor (LM5) will continuously reads the temperature of It's surroundings and transfer the signals to ADC.
- Similarly, intensity of light sensor (LDR) will continuously reads the light intensity of Its surroundings and transfer the signals to the ADC.
- ADC is the Analog to Digital Converter, this will convert the analog signals of LM5 & LDR sensors in to the digital signal.
- Then, the digital signal will be transferred to the FPGA board using the UART protocol.
- Here, UART protocol is used for the transmitting and receiving of the signals.

- Now, FPGA board will send /transmit the signal to display on LCD using UART protocol

II. LITERATURE SURVEY

Before employing FPGA-based solutions, various traditional methods and microcontroller-based systems were commonly used to measure temperature and light intensity. Here are some existing models that predate the utilization of FPGA kits for such applications:

- Microcontroller-Based Systems
- Standalone Sensor Circuits
- PC-Based Systems
- Data Loggers
- Analog Signal Processing
- Wireless Sensor Networks

From this Literature Survey we can observe that the methods they used to measure temperature and light intensity are not power efficient & they are unable to reconfigure or modify. And mainly these methods are unable to monitor the temperature and light intensity readings continuously.

III. PROPOSED MODEL

The proposed model for the design and development of an FPGA-based temperature and light intensity measurement system using the UART protocol builds upon the lessons learned from existing models. Here are key components and improvements in the proposed model:

- FPGA Board Selection
- Sensor Integration
- UART Communication Enhancement
- Testing and Validation

This proposed model will continuously monitor the temperature and light intensity. For this continuous monitoring we used UART protocol which is used for continuous seamless data transmission and receiving. Also, we used FPGA board instead of micro controllers, Since FPGA can be reconfigurable and power efficient used for testing and validation.

IV. RESULT & DISCUSSION

- We can observe the continuous monitoring of the temperature & light intensity at different conditions as shown in below images.

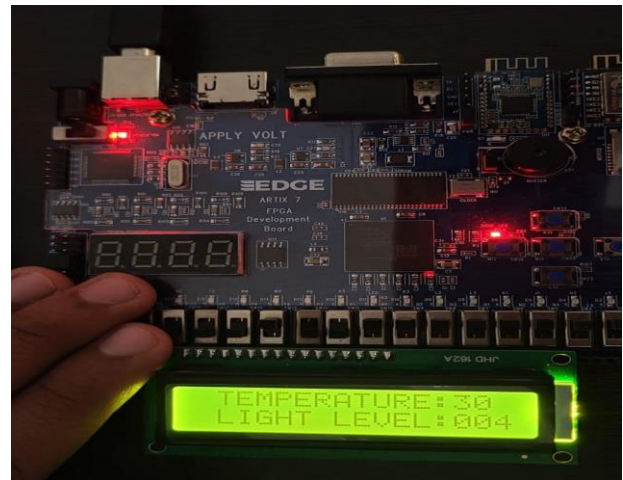


fig.1: This figure shows the readings of temperature & light intensity in the dark place.

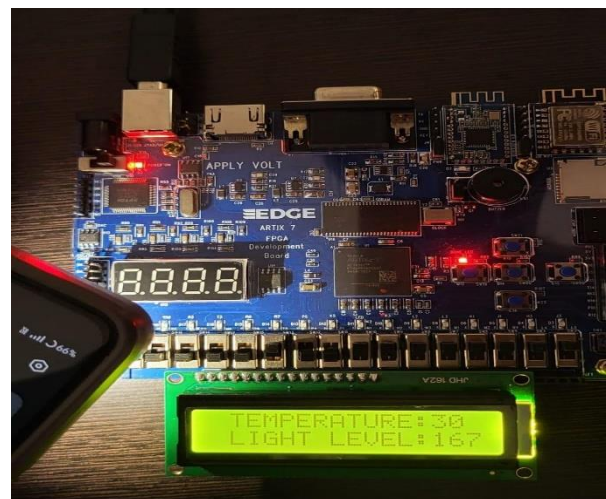


Fig.2: This figure shows the readings of temperature & light intensity in the bright place

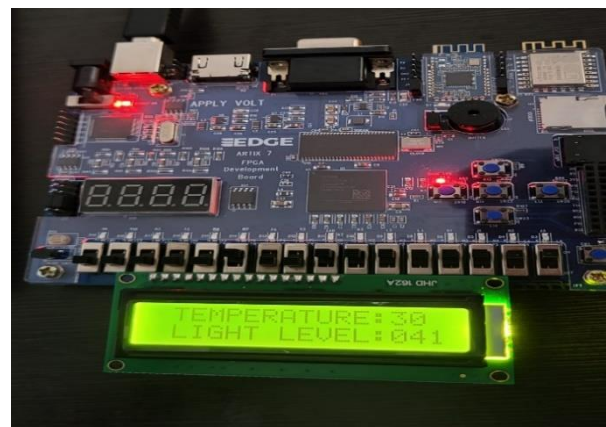


Fig.3: This figure shows the readings of temperature & light intensity of its surroundings.

V. CONCLUSION

- In conclusion, developing an FPGA-based temperature and light intensity measurement system using UART protocol offers significant advantages & disadvantages with continuous monitoring of temperature and light intensity. We used FPGA kit because it is a standard and verified kit. We can also rewrite/modify the program according to the user requirement. We get continuous readings of temperature and light intensity since we are using UART protocol. It transfers the data bits through baud rate. The standard baud rate is 9600bps which is sufficient for low-speed operations and it can reach speeds of up to 115200bps.

REFERENCES

- [1] W. Huang, M. Stan, K. Skadron, K. Sankaranarayanan and S. Ghosh. Compact Thermal Modelling for Temperature-Aware Design. In Proc. of DAC, June 2004.
- [2] XilinxFPGAEditor
<http://toolbox.xilinx.com/docsan/xilinx6/books/manuals.pdf>
- [3] Xilinx XPower
<http://www.xilinx.com/xpower>.
- [4] S. Velusamy, W. Huang, J. Lach, M. Stan and K. Skadron. Monitoring Temperature in FPGA based SoCs. University of Virginia Technical Report, CS-2004-39.
- [5] K. Skadron, M. R. Stan, W. Huang, S. Velusamy, K. Sankaranarayanan, and D. Tarjan. Temperature-aware microarchitecture. In Proc. ISCA-30, June 2003.
- [6] Pan, W.; Gong, G.; Li, J. A 20-ps time-to-digital converter (TDC) implemented in field-programmable gate array (FPGA) with automatic temperature correction. IEEE Trans. Nucl. Sci. 2014, 61, 1468–1473.
- [7] Song, Z.; Zhao, Z.; Yu, H.; Yang, J.; Zhang, X.; Sui, T.; Xu, J.; Xie, S.; Huang, Q.; Peng, Q. An 8.8 PS RMS resolution time-to-digital converter implemented in a 60 nm FPGA with real-time temperature correct