Sequential Circuits Synthesis For Rapid Single Flux Quantum Logic Based On Finite State Machine Decomposition

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Abstract- *Rapid Single Flux Quantum (RSFQ) logic is a obligation technology to over through Complementary metal-oxide semiconductor (CMOS) logic in some specialized areas due to providing ultra-fast and energy-efficient circuits. To realize a large scale integration design, electronic design automation (EDA) tools specialized for RSFQ logic are required due to the divergences in logic type, timing constraints, and circuit structure compared with CMOS logic. Logic synthesis is crucial in converting behavioral circuit description into a circuit net list, typically combining combinational and sequential circuit synthesis. For the RSFQ logic, the sequential circuit synthesis is challenging, especially for non-linear sequential blocks with feedback loops. Thus, this paper presents a sequential circuit synthesis algorithm based on finite state machine (FSM) decomposition, which ensures design functionality, lowers costs, and improves the RSFQ circuit performance. Additionally, we present the synthesis processes of the feedback logic and the Fredkin Gate and Feynman Double Gateto demonstrate how the proposed algorithm operates, and benchmark circuits reveal our method's ability to synthesize largescale sequential circuits using Xilinx tool.*

Keywords- RSFQ, FSM, Feynman Double Gate, Fredkin Gate.

I. INTRODUCTION

1.1. VERY LARGE SCALE INTEGRATION

Very large scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC makers add all of these into one chip.

Challenges

As microprocessors become more complex due to technology scaling, microprocessor designers have encountered several challenges which force them to think beyond the design plane, and look ahead to post-silicon:

Process Variation: As photolithography techniques tend closer to the fundamental laws of optics, achieving high accuracy in doping concentrations and etched wires is becoming more difficult and prone to errors due to variation. Designers now must simulate across multiple fabrication process corners before a chip is certified ready for production. Theoverhead for custom design is now reaching a tipping point, with many design houses opting to switch to electronic design automation (EDA) tools to automate their design process.

Timing/ design closure: As clock frequencies tend to scale up, designers are finding it more difficult to distribute and maintain low clock skew between these high frequency clocks across the entire chip. This has led to a rising interest in multicore and multiprocessor architectures, since an overall speedup can be obtained by lowering the clock frequency and distributing processing.2

First-pass success: As die sizes shrink (due to scaling), and wafer sizes go up (due to lower manufacturing costs), the number of dies per wafer increases, and the complexity of making suitable photo masks goes up rapidly. A mask set for a modern technology can cost several million dollars. This nonrecurring expense deters the old iterative philosophy involving several "spin cycles" to find errors in silicon, and encourages first-pass silicon success.Several design philosophies have been developed to aid this new design flow, including design for manufacturing (DFM), design for test (DFT).

Owing to technology improvements reaching the nanometer scale, manufactured chips arefaced with higher defect rates and increased susceptibility to soft errors. Soft

errors are mainly causedby cosmic-ray neutrons or alpha particles in device packaging. Soft error can hit either in the combinational logic or flip flops (FFs) of a sequential circuit. A single event transient (SET) occurs when a charged particle hits the combinational logic resulting in a transient current pulse. If this transient has enough width and magnitude, it could result in an error flipping the value of a gate. An SE upset (SEU) occurs if a charged particle is a memory element causing its value to flip. Soft errors grow in direct proportion to the number of cells in the design and with reduction in voltage. The demonstrated that soft errors will increase with technology improvements and that SET rates will be comparable with SEU rates.Fault tolerance in systems can be enhanced by adding redundancy. Redundancy can be added at module level, gate level, transistor level or software level. To enhance fault tolerance in sequential circuits, several techniques have been proposed in the literature. Triple modular redundancy (TMR) is one of the well-known techniques for soft errortolerance. In TMR, a module istriplicated and the three modules feed a voter that selects the correct value. TMR guarantees tolerance of soft errors causing an erroneous value at the output of a single module. In, a generalized MR scheme has been proposed which provides protection for a module with multiple outputs protecting only output combinations which have high probability of occurrence. In, a double MR fault tolerance scheme that utilizes self-voting circuits has been proposed.

Fault collapsing

There are two main ways for collapsing fault sets into smaller sets. These faults are called equivalent faults. Any single fault from the set of equivalent faults can represent the whole set. In this case, much less than k×n fault tests are required for a circuit with n signal line. Removing equivalent faults from entire set of faults is called fault collapsing. Fault F is called dominant to F' if all tests of F' detects F.

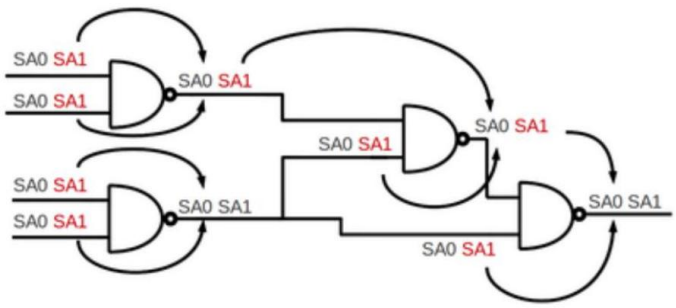


Figure1: fault equivalence in digital circuits

It is possible that two or more faults produce same faulty behavior for all input patterns. These faults are called equivalent faults. Any single fault from the set of equivalent faults can represent the whole set. In this case, much less than k×nfault tests are required for a circuit with n signal line. Removing equivalent faults from entire set of faults is called fault collapsing. Fault collapsing significantly decreases the number of faults to check. In the example diagram, red faults are equivalent to the faults that being pointed to with the arrows, so those red faults can be removed from the circuit. In this case, the fault collapse ratio is 12/20.

II. LITERATUREREVIEW

2.1 Self-Voting Dual-Modular-Redundancy Circuits for Single Event-Transient Mitigation

Dual-modular-redundancy (DMR) architectures use duplication and self-voting asynchronous circuits to mitigate single event transients (SETs). The area and performance of DMR circuitry is evaluated against conventional triple-modular-redundancy (TMR) logic. Benchmark ASIC circuits designed with DMR logic show a 10–24% area improvement for flip-flop designs, and a 33% improvement for latch designs.

2.2 Error Mitigation Using Approximate Logic Circuits: A Comparison of Probabilistic and Evolutionary Approaches

Technology scaling poses an increasing challenge to the reliability of digital circuits. Hardware redundancy solutions, such as triple modular redundancy (TMR), produce very high area overhead, so partial redundancy is often used to reduce the overheads. Approximate logic circuits provide a general framework for optimized mitigation of errors arising from a broad class of failure mechanisms, including transient, intermittent, and permanent failures. However, generating an optimal redundant logic circuit thatis able to mask the faults with the highest probability while minimizing the area overheads is a challenging problem. In this study,we propose and compare two new approaches to generate approximate logic circuits to be used in a TMR schema. The probabilistic approach approximates a circuit in a greedy manner based on a probabilistic estimation of the error. The evolutionary approachcan provide radically different solutions that are hard to reach by other methods. By combining these two approaches, the solution space can be explored in depth. Experimental resultdemonstrate that the evolutionary approach can produce better solutions, but the probabilistic approach is close. On the other hand, these approaches provide much better scalability than other existing partial redundancy techniques.

III. METHODOLOGY

SEQUENTIAL LOGIC

The proposed technique may be easily extended to sequential logic, by extending the methodproposed in for CED in FSMs based on parity check codes. To make the circuit fault tolerant,Theoriginal area-optimized FSM implementation and an output comparator are added to detect faults in the next state and output logic, as illustrated in figure 4. The parity checker and the comparator produce the same control signals of the previous section to diagnose and correct a fault.

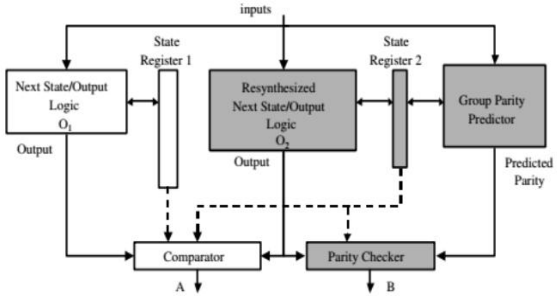


Figure 2:Methodology for Sequential Circuits

The parity check bits are stored in bi-stable elements to also detect faults in the state register in however; this is not possible in a fault tolerant implementation as the check is performed a cycle later, while the next state logic is evaluating the next state using an erroneous present state. Moreover, although the fault is detected it may not be corrected without performing is computation thatwill slow down the circuit operation.

3.1 FEYNMAN DOUBLE GATE:

Input vector (Iv) and output vector (Ov) for 3 × 3 reversible Feynman double gate (F 2G) is defined as follows : Iv = (a, b, c) and Ov = (a, a ⊕ b, a ⊕ c). Block diagram of F 2G is shown in Figure 3. Fig. represent the quantum equivalent realization of F 2G.From Fig. 1(b) we find that it is realized with two 2×2 Ex-OR ate, thus its quantum cost is two. According toour design procedure, twelve transistors are required to realize F2G reversibly as shown in Fig. 3.

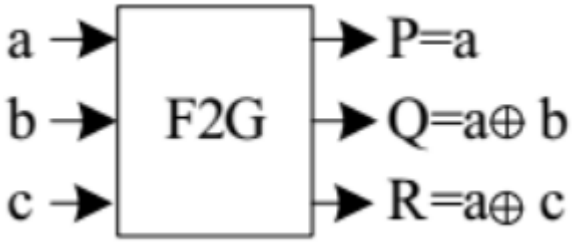


Figure 3: Block diagram of Reversible Feynman double gate

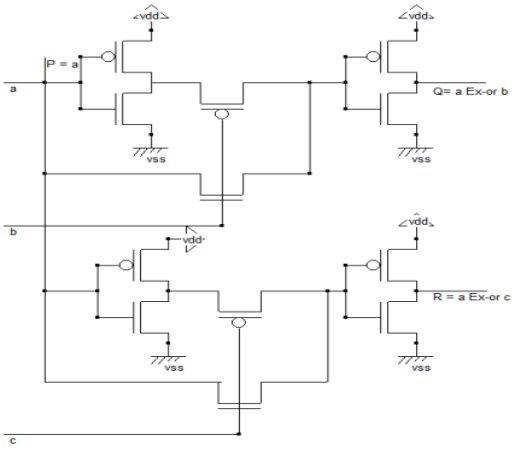


Figure 4: Stucture Reversible Feynman double gate

3.2 Fredkin Gate:

The input and output vectors for 3 × 3 Fredkin gate (FRG) are defined as follows:

Iv = (a, b, c)andOv = (a, ab⊕ ac, ac ⊕ab). Block diagram of FRG is shown in Fig. 5. Fig. 6 srepresentsthe quantum realizationof FRG. In Fig., each rectangle is equivalent to a 2 × 2 quantum primitives, therefore its quantum cost is considered as one. Thus total quantum cost of FRG is five. To realize the FRG, four transistors are needed as shown in Fig.

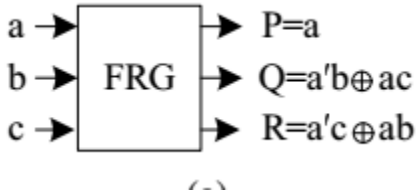


Figure 5: Block diagram of Fredkin gate

3.3 Reversible 4:2 Encoder:

The proposed 4:2 Reversible Encoder is shown in figure. It uses three Feynman gates(FG) and one Fredkin gate(FRG).It has four inputs A,B,C,D and two outputs Y1&Y2 and also hastwo garbage outputs g1&g2.The operation of circuit is given in Table. This proposed 4:2 Encoder has Quantum cost of 8. Reversible logic gates are very interesting topic for research due to less heat dissipation and low power consumption. Reversible logic gates are used in various applications such as CMOS design, Quantum computing, Nanotechnology, Cryptography,Optical computing, DNA computing, Digital signal processing (DSP), Communication computer graphics. Quantum computing is not realized withoutimplementation of reversible logic .Main purposes of designing of reversible logic gates are to decrease quantum cost, garbage output, no. of gates. In this paper we present a proposed design of Encoder using Feynman and

Fredkin reversible logic gates. Reversibility in computing implies that information about the computational states should never be lost. The information can be recovered for any earlier stage by computing backwards or un computing the results. This is termed as "logically reversibility". Physical reversibility is a process that dissipates no heat in terms of wastage of energy. Power dissipation of reversible circuit, under ideal physical circumstances, is zero. The loss of information is associated with laws of physics describing that one bit of information lost dissipates kTln2 of energy, where k is Boltzmann' constant and T is the temperature of the system. Reversible computing will also lead to improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits. To increase the portability of devices again, reversible computing is required. Reversible are circuits or gates that have one to one mapping between vectors of inputs and outputs, thus the vector of input states can be always reconstructed from the vector of output states. In reversible logic gates the number of output bits always equals the number of input bits. The fan out of every signal including primary inputs in a reversible gate must be one.

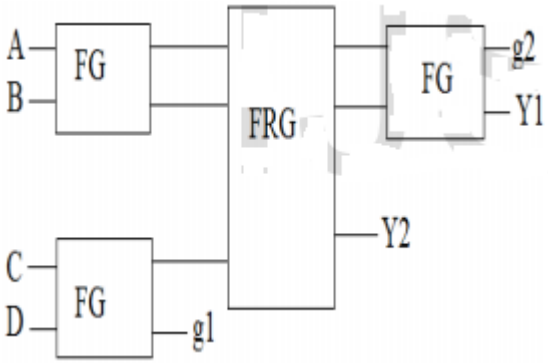


Figure 6: Reversible 4:2 Encoder

3.4 Reversible 2:4 Decoder:

Decoders are the collection of logic gates fixed up in a specific way such that, for an input combination, all outputs terms are low except one. These terms are the min-terms. Thus, whenan input combination changes, two outputs will change. Let, there are n inputs, so number of outputs will be 2n. There are several designs of reversible decoders in the literature. To the best of outknowledge, the designs from is the only reversible design that preserve parity too.This demonstrates the reversible logic synthesis for the n-to-2n decoder, where n is the number of data bits. The circuits are designed using only reversible fault tolerant Fredkin and Feynman double gates. Thus, the entire scheme inherently becomes fault tolerant. Algorithm for designing the generalized decoder has been presented. In addition, several lower bounds on the number of constant inputs, garbage outputs and quantum cost of the reversible fault tolerant decoder have been proposed. 2-to-4 reversible fault tolerant decoder can be realized with at least 12 quantum cost. A 2-to-4 decoder has 4 different 2×2 logical AND operations. A reversible fault tolerant AND2 operation requires at least 3 quantum cost. So, 2-to-4 reversible fault tolerant decoder is realized with at least 12 quantum cost.

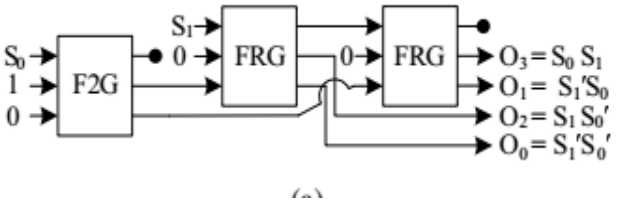
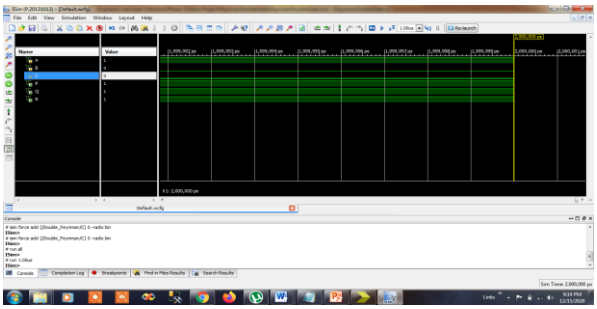


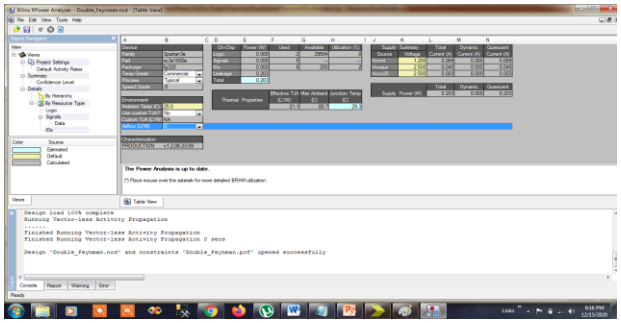
Figure 7: Reversible 2:4 Decoder

IV. SIMULATION RESULTS

4.1 TIMING DIAGRAM XILINUX TOOL



4.2 POWER ANALYSIS XILINUX TOOL



V. CONCLUSION

This paper presents a novel algorithm for synthesizing sequential circuits for RSFQ logic. The developed algorithm employs the FSM decomposition method from the RSFQ perspective, accomplishing the sequential circuit synthesis using the FSM of the RSFQ gates to build a large FSM system. Besides, state encoding, sub-FSM mapping, and super gates utilization are also introduced to complete the algorithm. Our method significantly reduces the

number of junctions in each circuit compared with the traditional methods after synthesis, with the maximum frequency reaching up to the limitation of our PDK. Furthermore, the simulation results on a verify our method's functionality. By employing the FSM decomposition method, the RSFQ sequential synthesis problem could be solved and the circuit performance including clock frequency, area and power consumption could be improved.

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