Implementation of Low Power Thermometer Code To Digital Converter Using Wallace Tree Encoder

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Abstract- *VLSI architecture for a high performance Low power thermometer code to digital converter using Wallace tree encoder is proposed in this research. When transforming code of thermometer type to binary type, WTE is utilized (analog to digital conversion). This is a type of flash ADC with an encoder, group of resistors and a comparator circuit, and it is a high speed application. To obtain binary code from the comparator's output, an approximate encoder is necessary. The encoder's energy consumption is a crucial problem when constructing alow-power flash type of ADC. Wallace tree encoders decrease mistakes caused by the presence of zeroes in a succession of ones presence to a sequence of zeroes at a comparator output, but they consume excess power. A low-power WTE is fabricated using a CLA full adder to overcome the issue of excessive power consumption. The proposed device uses only 616.4nW of electricity and has a 57.13-second delay. Xilinux14.2 tool is used to design the circuit and simulated using test bech.*

Keywords- CLA Full adder, ADC, Encoder.

I. INTRODUCTION

Viterbi is firstly introduces by Andrew J. Viterbi in 1967, considering the VA is efficient method for encoding convolutional code. The objective of this work is to explore the design of a Viterbi encoder for wireless applications. Synchronous and Asynchronous are the two design styles existing for the realization of digital communication systems. Synchronous systems work with global clock and so has higher switching activity than asynchronous system. As switching activity is more in case of synchronous system power consumption is higher. Asynchronous systems are controlled by local clock or by dividing global clock resulting low switching activity. Since switching activity is low, speed of the system increases at the same time power consumption is reduced. Numerous advantages can be obtain from asynchronous designs with the use of a global clock. Switching activity is related only when system performing useful work. This is the important trait for battery operated systems. Worst case path delay can be used o determine the speed of synchronous systems which determines the maximum clock frequency. Asynchronous systems run on the average path delay of all their components. With the increasing demand of wireless multimedia business, it is necessary to call for strict criterion on speed & power consumption of portable devices. With increasing of the transistor count & difficulty to propagate clock signals through an entire circuit VLSI designer suffers big problem. To tackle such a problem designers resort more &more to Globally Asynchronous Locally Synchronous (GALS) or totally asynchronous solutions.Asynchronous circuits can be design using two different methods. First is bundle data (BD)which relies on delay lines. Second approach is delay insensitive (DI) relies on dual rail scheme, can be categories into several subcategories as pure delay insensitive (DI), Quasi Delay Insensitive (QDI) and Speed independent circuits (SI). To reduce area & switching activity bundle data approach uses handshaking, but it faces technology related problem. Extra care with the computation of timing constraints between data & controlsignals is required. QDI approach can be classified into several templates according to design technique. This yield high performance circuits but they are much larger than their synchronous counterparts. One of the most adopted templates is Delay-Insensitive Minterm Synthesis (DIMS) for implementing QDI logic but it requires more space and logic2elements with correspondingly high cost. Hard decision and soft decision are the two encoding techniques can be used for design of Viterbi encoder. Hard decision technique can identify any number of errors which are less than orequal to the correction capacity of the code. Soft decision technique decodes correctly any corrupted sequence with one or two errors independently of the quantification levels attributed to the symbols of a given received sequence.

II. LITERATURE REVIEW

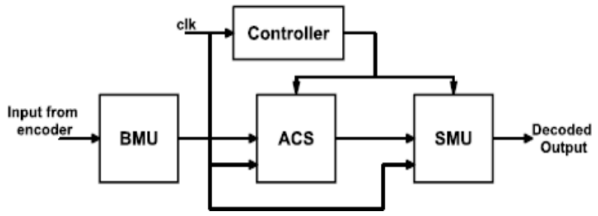

Figure 2: Synchronous Viterbi Encoder Using HREM

In the Viterbi encoder; the register-exchange method is used to finish the survivor path storage and encoding. Frequent switching is the main disadvantage of register exchange method and long constraint length. The new proposed method designed for encoding data bits is known as hybrid register exchange method (HREM). Using this method switching activity can be reduced. Initial state can be first traced through an m cycle, and then transfer the content of initial state to the current state and the next m bits of the register is the m bits of current state itself.

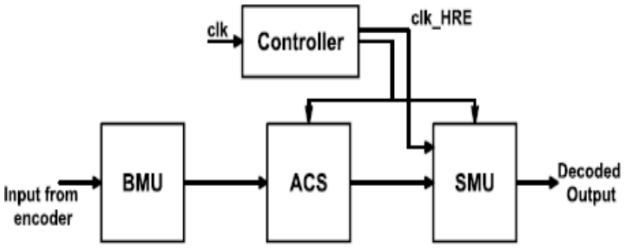

Figure 3: Proposed Asynchronous Viterbi Encoder Using HREM

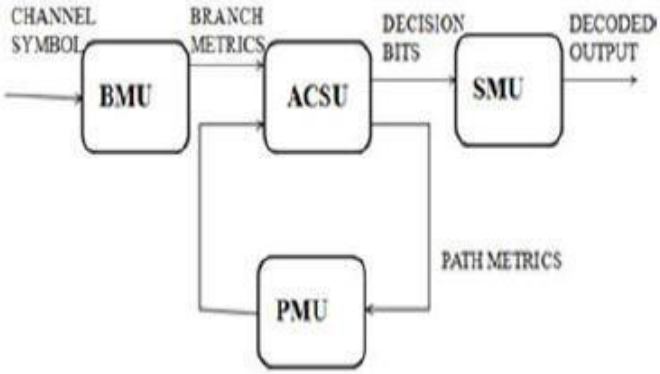

Figure 4: Block Diagram of Viterbi Encoder

In general, a ROM encoder will require 1 out of N codes as input, whichnecessitates the usage of two input XOR gates. The “Wallace Tree encoder” does not require these kinds of modifications because it receives the thermometer code as input directly. The ROM encoder will address at least three lines if the comparator output has even a single bit defect, resulting in an error-free code. However, inaccuracy is much decreased with the Wallace Tree encoder shown in Fig.2sBecause the majority of the world's critical signals are analogue in nature. They are challenging to store and hard to process. As a result, they must be converted to digital pattern. An ADC converts analogue signals into digital data, allowing for more precise and dependable storage and processing.

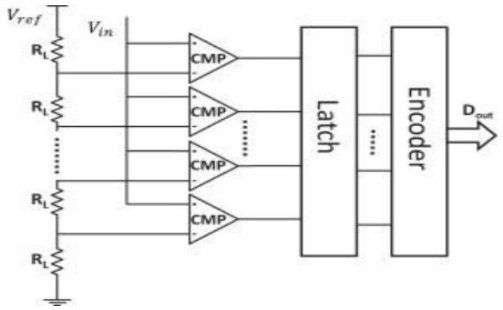

Figure 5:Block diagram of flash type ADC

1V. SIMULATION RESULTS

4.1 TOP LEVEL ARCHITECTURE

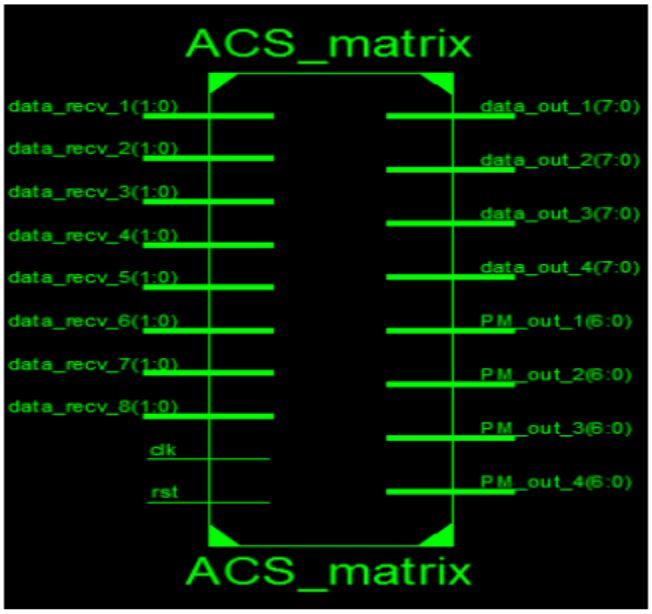

Figure 6: ACS MATRIX

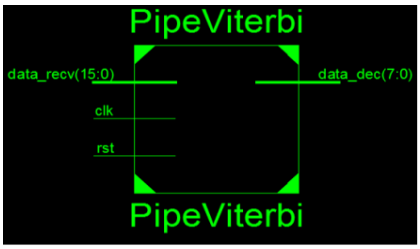

Figure 7: Pipeviterbi

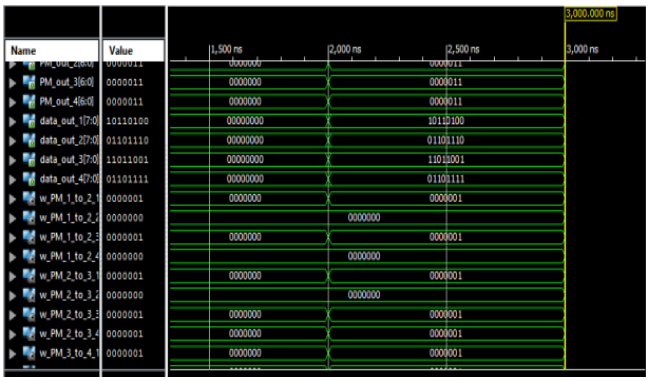

Figure 8: ACS Matrix Output

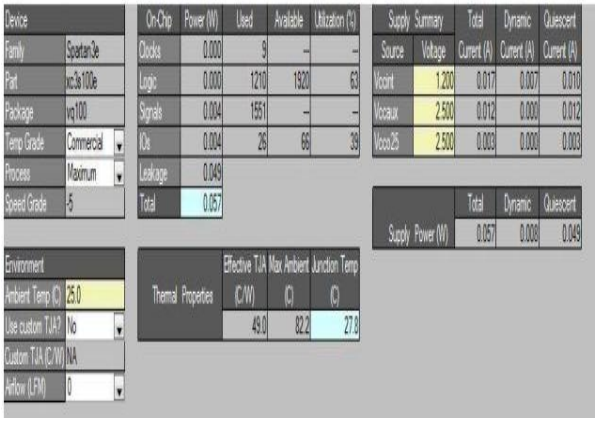

Figure 9: Power Analysis of Viterbi encoder

V. CONCLUSION

Viterbi encoder is designed using synchronous and asynchronous register exchange and hybrid register exchange method. The output waveform of the synchronous and asynchronous VD using HREM is shown in below respectively. VD is designed in Verilog using Xilinx 14.2. The dynamic power calculated for synchronous and asynchronous design is given .Asynchronous hybrid register exchange outperforms over synchronous and asynchronous register exchange & synchronous HREM. Both register exchange and hybrid register exchange module have been designed in synchronous and asynchronous technique. Asynchronous Hybrid register exchange method gives the 13.04 % reduction in dynamic power consumed when compared with its synchronous counterpart with much better increase in maximum frequency.

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