A low voltage variation for 1uA load current using 90 nm technology

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Abstract- *The problem encountered in some papers is of low slew rate, power supply rejection ratio, line and load regulations, high quiescent current, settling time, and load current. Generally, due to these parameters LDO suffers with low battery life. A capacitor less LDO is presented, which improves these parameters and reduce the power consumption by reducing the quiescent current and drop out voltage. Tremendous reduction is achieved in voltage variation of less than 1mV for 1 uA.*

Keywords:- low drop out voltage(LDO) regulator, PSRR, SR.

I. INTRODUCTION

Here are two types of LDOs based on capacitor as

1.1) Low Drop Out Regulators with Capacitor

Reduces output noise, the output voltage variation and improves PSRR. But it also has some disadvantages
That use of capacitor increases the chip area, affects the stability of LDO regulator, affects on a large load transient response, affect during shut-down, there is also low start-up issue.

1.2) LDO without capacitor

Present research in LDOs is focused on removing this external capacitor while maintaining stability, good transient response and high power supply rejection performance. Capacitor free low drop-out regulators have several advantages over the low drop-out regulators with capacitance on the basis of small size and portability

II. LITERATURE SURVEY

A stable LDO voltage regulator with a novel Double Recycling Error Amplifier structure is presented which enhance the slew rate [1] but with increased quiescent current. Few authors reduces the value of quiescent current by designing LDO with push pull composite power transistor [2] which is having low PSR that indicate low output supply voltage irrespective of supply voltage.High PSR of -95dB at 5MHz have been achieved by paper [3] which is integrated with medical body area network (MBAN) transceiver having drop of 300mV. Since minimum dropout is the requirement of many applications, so drop out of 200 mV has been shown by paper [4] having low values of load and line regulations. Better line and load regulations of 3.2 mV/V and 12 mV/A is presented in paper [5]. In this paper the settling time is more which is reduced by paper [6] because settling time is also one of the important parameter while considering LDO.

III. INTRODUCTION OF LOW DROPOUT LINEAR REGULATOR

Figure1 illustrates the functional block diagram of a typical low dropout linear regulator (LDO). It consists of four main sections, (A) a reference voltage, (B) an error amplifier, (C) a series pass element and (D) a feedback network. The reference voltage aims at generating a stable, accurate and temperature-tolerant reference voltage. Then the error amplifier detects the difference between the feedback voltage and the reference voltage (V_{REF}) .

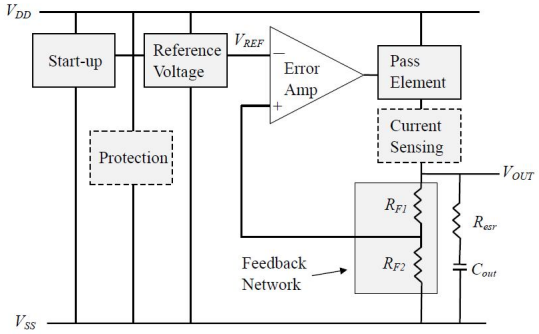


Fig.1 Functional blocks of a typical LDO voltage regulator

IV. SYSTEM MODEL

For error amplifier design folded cascode topology(Figure 2) have been used because it

- Control of the frequency behavior.
- Can get more gain by increasing the output resistance of a stage.
- PSRR of the two-stage op amp is high which make better option for many applications.
- A two-stage op amp can become unstable for large load capacitors (if nulling resistor is not used).

- The cascode op amp leads to wider ICMR and/or smaller power supply requirements.

Specifications:

1. Input Voltage = 1 V
2. Reference Voltage = 500 mV
3. Technology = 90 nm

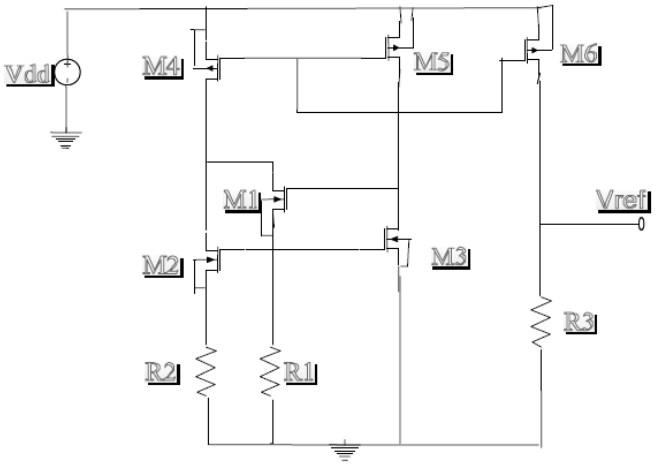


Fig.2 Circuit diagram of voltage reference circuit

V. PROPOSED METHODOLOGY

To achieve our objectives, we will device a method to get our required parameters. So, I will connect another error amplifier to the substrate of pass element using 90nm technology. Fig. shows the block diagram of proposed LDO voltage regulator.

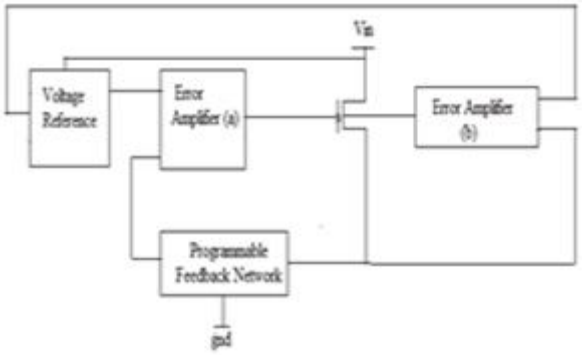
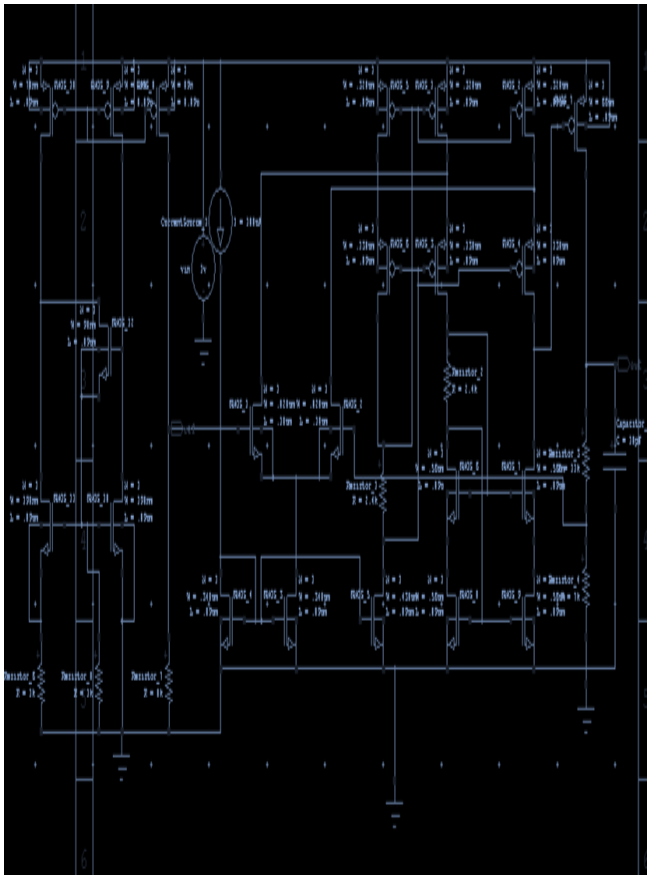


Fig.3 Block diagram of proposed LDO voltage regulator

Error Amplifier

Error amplifier is just an operational amplifier which is made up of folded cascade type because this amplifier provides high slew rate and power supply rejection ratio. It also solves the problem of limited bandwidth of conventional LDO. The LDO consist of two error amplifier: one is connected to the gate of pass transistor and another to the body of pass transistor.

VI. RESULT



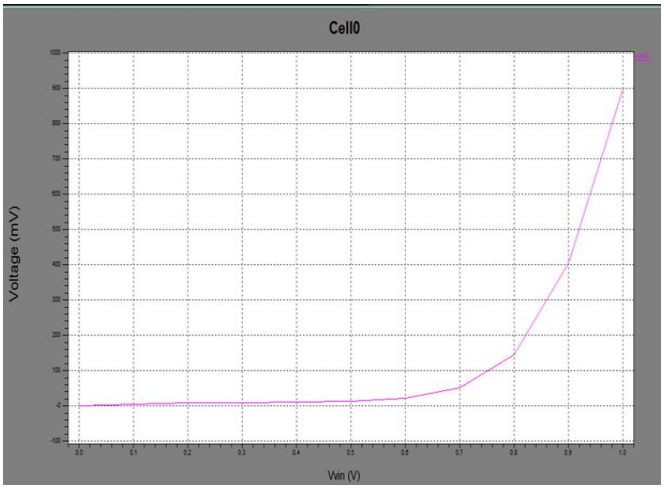


Fig.4 Result

The simulation result illustrates that the output voltage variation is 100mV when the input voltage changes from 0V to 4.1V with the drop-out voltage higher than 900mV, resulting in the line regulation of 0.9V/V.

VII. CONCLUSION

A low drop out voltage regulator has been designed on 90 nm and simulated in Tanner EDA software. To improve the performance of LDO voltage regulator, folded cascade opamp topology is used for designing error amplifier , which regulates the output voltage at 0.9 V from 1 V supply with minimum drop-out voltage of 100 mV .Within the scope of power management system ,low quiescent current consumption is required which is 100 µA and ΔV_{out} is less than 1 mV.for 1uA load current.

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