Study and Performance Analysis of Junctionless FinFET

Camy Joshya Y[1], Dr.P.Karthigaikumar[2], Vimala A[3]
[1, 2, 3] Department of Electronics and Telecommunication Engineering
[1, 2, 3] Karpagam College of Engineering, Coimbatore, Tamil Nadu, India

Abstract- *Junctionless transistor is a uniformly doped transistor without junctions. All existing transistors are based on the use of semiconductor junctions which is formed by adding dopant atoms into the semiconductor material. When the distance between junctions in devices falls below 10nm, then high doping concentration gradients become indispensable. In this paper, Junctionless Fin Field-Effect Transistor (FinFET) was analysed for sub-32-nm technology node using Technology Computer Aided Design (TCAD) simulations. Impact on drive current is predicted. The short channel effects can be reduced effectively.*

Keywords- Fin field-effect transistor (FinFET), junctionless, random dopant fluctuation (RDF), variability, TCAD.

I. INTRODUCTION

A conventional Metal Oxide Field Effect Transistor (MOSFET) contains two p-n junctions at the source and drain regions. When the devices are scaled down, the formation of such junctions need large doping concentration gradient and careful fabrication. These severe demands thrust the scaling of MOSFETs to their deep limits. Hereby a new device which is called junctionless (JL) transistor [1], [2] has been proposed to assuage these problems. Its structure is analogous to a conventional MOSFET; however, with homogeneous doping polarity and a uniform doping concentration across the channel, source, and drain, the device requires no junctions, e.g., n+ source–n+ channel–n+ drain for an N-channel Metal Oxide semiconductor field-effect transistor (NMOS) and p+ source–p+ channel–p+ drain for an P-channel Metal Oxide semiconductor field-effect transistor (PMOS). Hence, there will not be any diffusion, because the gradient of the doping concentration between the Source/Drain and the channel is zero, which eliminates a resultant annealing process and allows the device to be fabricated with even shorter channels.

In the junctionless transistor, the silicon channel can be a form of silicon nanowire (SiNW), which is thin and narrow as possible. Therefore, when the device is turned off, the SiNW can be entirely pinched off. In addition, the SiNW needs to be heavily doped to allow for a reasonably high current when the device is turned on. The main conduction mechanism in a junctionless field-effect transistor (JLFET) relies not on the surface but on the bulk current. It turns off by making the channel fully depleted [3], [4], [5]. They have near-ideal sub threshold slope, tremendously low leakage currents, and fewer degradation of mobility than classical transistors.

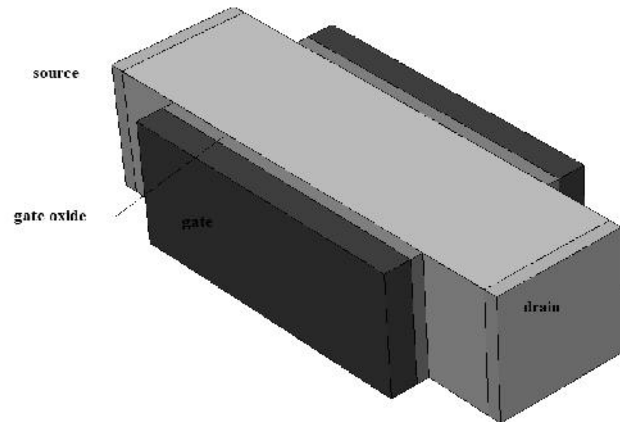

Fig. 1: Structure of Junctionless FinFET.

Utilizing a single gate, it is quite difficult to fully deplete the channel, and also, it is difficult to obtain the acceptable threshold voltages in such a condition [6], [7]. Hence, a double-gate FinFET is an alternative device for JLFETs due to its superior electrostatic control of the channel. The V_T fluctuation caused by the Wsi variation of junctionless a transistor is drastically larger than inversion-mode transistors with nearly intrinsic channel. This is because, in junctionless transistors, the channel doping concentration cannot be reduced in order to maintain their inherent advantages [8], [9]. Junctionless devices are vulnerable to process-induced variability including line edge/width roughness (LER/LWR), random dopant fluctuation (RDF), oxide thickness, work function variation, etc. While line edge roughness (LER) [10] and random dopant fluctuation (RDF) [11] induced variability were already shown to be significant for junctionless FinFETs (JL-FinFETs). In this work, we used TCAD simulations to investigate the characteristics for numerous JL-FinFET technology generations, which intended to congregate ITRS targets for the near future.

II. METHODOLOGY

Three-dimensional n-type double gate JL-FinFETs for 32nm technology node shown in Fig. 1 were drawn using Sentaurus TCAD [12].The JL-FinFETs are intended to meet

the 2009 ITRS targets [13] for 32-, 21-, and 15-nm high-performance logic devices, and detailed design parameters are given in Table 1. In our JL-FinFETs, devices with a uniform doping concentration $N_D = 9 \times 10^{19}$ cm^{-3} had their local doping profiles randomized according to the Sano method, wherein a number of discrete dopants following a Poisson distribution are assigned to random locations within the device. Hence smaller JL-FinFETs having fewer total dopants exhibit larger relative doping fluctuations, i.e., larger RDF.

Table 1: Nominal parameters for simulated JL FinFET

Quantity	Technology node 32 –nm	Description
L_g (nm)	22	Physical gate length
EOT(nm)	0.90	Oxide thickness
N_D(cm^{-3})	9×10^{19}	Fin/body doping
T_{fin}(nm)	9.6	Fin thickness
Ψ_m(eV)	5.25	Gate work function
T_g (nm)	2.0	Gate thickness

HfO_2 with high K dielectric is used as the oxide material in order to reduce the gate leakage. Heavily doped N-channel junctionless transistors usually need a gate material with high work function, such as p+ polycrystalline silicon or platinum, in order to attain a appropriate V_T value. Accordingly, a gate work function of 5.25 eV was used for the junctionless FinFET in this simulation. On the other hand, a mid-gap gate material (work function of 4.6 eV) can be used in the simulation to keep the V_T value between 0.2 and 0.3 V at the nearly intrinsic channel for the inversion-mode transistors.

III. SHORT CHANNEL EFFECT

Short-channel effects are studied to be less important [6] in junctionless devices as it is investigated that drain-induced barrier lowering (defined measuring the reduction of the energy barrier when it is applied the same V_D used to define the I_{on} current) is lower than in equivalent inversion-mode devices, especially for the shortest devices. In MOSFET with junctions, part of the reduction of the threshold short-channel effects is due to the presence of a space-charge region associated with the junctions and part of it is due to the growth of the drain space-charge region with drain voltage.

In a MOSFET with physical gate length L, the effective gate length is L_{on}, when the device is on, and the effective gate length is L_{off} when the device is off. Note that $L_{off}<L_{on}$, which means that the “effective” channel length when the device is off is shorter than when it is on. In the junctionless transistor, the doping concentration is constant across the device. The electrostatic squeezing of the channel in the off device propagates into the source and drain; as a result, $L_{off}>L$ when the device is off. When the device is on, the squeezing effect is removed, such that $L_{on}=L$. As a result, effective gate length is larger on the off state than in the on state i.e., $L_{off}>L_{on}$, which improves short channel effects.

IV. ELECTRIC FIELD

The electric field perpendicular to the current flow is studied to be notably lower in junctionless transistors than regular inversion-mode or accumulation-mode field-effect transistors. As inversion channel mobility in Metal Oxide semiconductor transistor is reduced by this electric field, the squat field in junctionless transistor may bestow them an advantage in terms of current drive for complementary metal oxide semiconductor applications. This observation still applies when quantum confinement is present. The major carriers in channel region for a Junction transistor create itself a barrier to carrier scattering, whereas, the Junctionless transistor does not have this problem, leading to get a high current drive. The advantage linked to the JL transistors is simple device fabrication due to the elimination of junction implantation and annealing; hence, a simple process outcomes in a reduced cost. But these advantages are difficult to be achieved for junction transistors. That is why excluding the so-called short-channel effects (SCEs) the conventional CMOS devices face lots of critical issues for achieving low cost mass production.

V. RESULT AND DISCUSSION

The I_D–V_G characteristics at V_D = 0.50V for junctionless FinFET of 32nm device is shown in Fig. 2.Also the I_D–V_D characteristics is shown in Fig. 3.It is found that the threshold voltage decreases, when there is increase in the doping concentration. At the gate voltage (V_G) below threshold ($V_G< V_{TH}$) the channel region is depleted of electrons .It keeps the device in off condition till further increase in gate voltage. At threshold voltage ($V_G = V_{TH}$) a string-shaped channel of neutral n-type silicon connects source and drain. Above threshold voltage ($V_G >V_{TH}$) the channel of neutral n-type silicon expands in width and thickness. When a flat energy bands situation is reached ($V_G =V_{FB}>> V_{TH}$) the channel region has become a simple resistor.

It is noted that at zero gate voltage, the device is in its on state when it is biased by a nonzero drain source voltage. A adequate negative bias which applied to the lateral gates deplete the region under the gates and cause an off state. The

current characteristic curves also show that the device has on off ratio of 10^5 for the simulated device. In the case of accumulation MOSFETs (AMOSFETs) and JLTs (gated resistors), the depletion of the channel region is in the off state at V_G=0V, caused by the work function difference between the gate material and the highly doped channel .As a result, in all fabricated devices a gate bias voltage equal to the work function difference between channel and the gate is required to achieve a flat band condition. It is worth noting that the JLT is mainly a gated resistor that is generally an on device at $V_G = 0$ V. When zero gate bias is applied to JL FinFET, the entire channel region is neutral (i.e., not depleted), and the device is in a flat band condition. The similar and high doping concentration of the channel and the gates eliminates the cause of a work function difference between the channel and the gates, which provides the flat band condition at zero gate voltage.

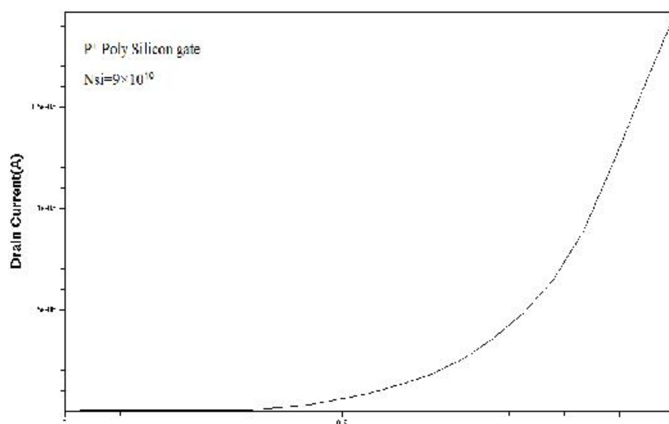

Fig. 2: Drain current versus gate voltage of a JL FinFET

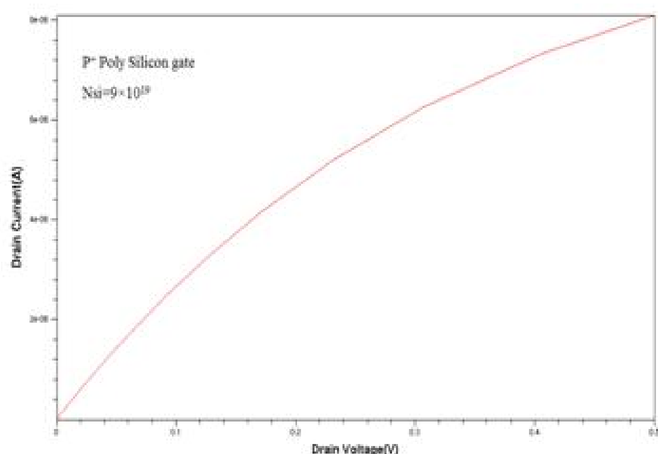

Fig. 3: Drain current versus drain voltage of a JL FinFET

VI. CONCLUSION

This paper presents the study of junctionless FinFET and the characteristics of junctionless FinFET are analysed using TCAD simulation. Improvement in drive current is achieved for junctionless FinFET. As we know all the existing transistors are based on the use of semiconductor junctions created by introducing dopant atoms into the semiconductor material. According to moor's law the junctionless transistor is most excellent to reduce the size of the transistor with tremendous behavior which makes the chip makers work easy. Junctionless fabrication process is greatly simplified, compared to standard CMOS, since there are no doping concentration gradients in the device.

REFERENCES

[1] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. Dehdashti Akhavan, R. Yan,I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher,B. McCarthy, and R. Murphy, "Nanowire transistors without junctions,"Nat. Nanotechnol., vol. 5, no. 3, pp. 225–229, Mar. 2010.

[2] A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi,and J.-P. Colinge, "Junctionless nanowire transistor (JNT): Properties and design guidelines," in Proc. ESSDERC, Sep. 14–16, 2010, pp. 357–360.

[3] R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-Orabi, and K. Kuhn, "Comparison of junctionless and conventional trigate transistors with Lg down to 26 nm," IEEE Electron Device Lett., vol. 32, no. 9, pp. 1170–1172, Sep. 2011.

[4] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, "Bulk planar junctionless transistor (BPJLT): An attractive device alternative for scaling,"IEEE Electron Device Lett., vol. 32, no. 3, pp. 261–263, Mar. 2011.

[5] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," IEEE J. Solid-State Circuits, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.

[6] C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "Performance estimation of junctionless multigate transistors," Solid-State Electron., vol. 54, no. 2, pp. 97–103, Feb. 2010.

[7] S. Yu, Y. Zhao, Y. Song, G. Du, J. Kang, R. Han, and X. Liu, "3-D simulation of geometrical variations impact on nanoscale FinFETs," in Proc. ICSICT, 2008, pp. 408–411.

[8] S-J. Choi, D-I. Moon, S. Kim, J. P. Duarte, and Y-K. Choi, "Sensitivity of threshold voltage to nanowire width

variation in junctionless transistors," IEEE Electron Device Lett., vol. 32, no. 2, pp. 125–127, Feb. 2011.

[9] R. Trevisoli, R. Doria, M. de Souza, and M. Pavanello, "Threshold voltage in junctionless nanowire transistors," Semicond. Sci. Technol., vol. 26,no. 10, p. 105 009, Oct. 2011.

[10] G. Leung and C. O. Chui, "Variability of inversion-mode and junctionless FinFETs due to line edge roughness," IEEE Electron Device Lett., vol. 32, no. 11, pp. 1489–1491, Nov. 2011.

[11] Greg Leung and Chi On Chui, "Variability Impact of Random Dopant Fluctuation on Nanoscale Junctionless FinFETs," IEEE Electron Device Lett., vol. 33, no. 6, pp. 767–769, June. 2012.

[12] Sentaurus TCAD User Manual, Synopsys, Inc., Mountain View, CA, Version F-2011.09.

[13] International Technology Roadmap for Semiconductors, Semicond. Ind. Assoc., San Jose, CA, 2009.