Performance Analysis of Resonant Converter Using LLC Topologies

Deepalaxmi. R[1], Desigan. V[2], Dineshkumar. S[3], Ishwarya. V[4], Jayabharathi. K[5]
[1, 2, 3, 4, 5] Department of Electrical and Electronics Engineering
[1, 2, 3, 4, 5] SSN College of Engineering

Abstract- *In conventional converters with PWM switching, the switching devices are made to turn on and turn off the entire load current at high di/dt. The devices handling with high di /dt also experience high-voltage stress across them. Due to these two effects, there are increased power losses in the switching devices. In case the size and weight of the converter is to be reduced, switching frequencies are increased. At these high frequencies, switching losses and high voltage stresses are further aggravated. The shortcomings enunciated above can be minimized if each switch in converter is turned on and off when the voltage across it is zero at the instant of switching. ZVS technique along with LLC resonant circuit to turn on and turn off the active switches (MOSFET) has been used. The aim of the project is to simulate and analyze different topologies of LLC resonant converter, to identify the efficient topology using MATLAB simulink and to construct a proto type model of the efficient topology.*

Keywords- Resonant converter, Soft switching, Zero voltage switching, LLC topology

I. INTRODUCTION

Hard switching occurs during the overlap between voltages and current which takes place when MOSFET is switched on and off. The overlap in the switching losses can be minimized either by increasing the rate of change of current (di/dt) or voltage (dv/dt) in the switching waveform. On the contrary, if the switch is turned ON or OFF only when the voltage across it is zero. Then this switching is defined as Zero Voltage Switching (ZVS). In the resonant converters, the resonant capacitor provides a zero-voltage condition for the switch to turn on and off while the voltage across the device made zero. In general, ZVS is preferred over ZCS at high switching frequencies, primarily due to internal capacitances associated with the switch. ZVS eliminates the capacitive turn-on loss. It is suitable for high-frequency operation. The use of the soft-switching ZVS topology enables high-frequency operation that maximizes efficiency by minimizing the significant switching losses.

A basic resonant (AC-DC) converter consists of a diode bridge rectifier followed by a bulk capacitor and a high frequency resonant converter. This kind of converter inevitably introduces highly distorted input current, resulting in serious harmonic distortion and a low power factor. In order to comply with the more stringent regulations on current harmonics and improve the power factor, an additional stage of Power Factor Correction (PFC) is cascaded in front of the converter. In spite of its good performance, such two stage construction results in high cost and low efficiency.

II. PROPOSED METHOD

LLC topology has been used sparingly in high-end applications that require the very high efficiency. However with increased efficiency, LLC topology is attractive throughout product categories and power levels. Two variants of the LLC converter are the series resonant converter and the parallel resonant converter. The LLC converter is series resonant when C_r is in series with the magnetizing inductance L_{r1}/L_{r2} of the transformer and a parallel resonant converter when C_r is in parallel with the magnetizing inductance L_{r2}. All primary side MOSFETs turn on resonantly to obtain ZVS thus resulting in full recycling of the energy contained in the MOSFETs' parasitic output capacitance. Resonant operation of all switching devices in the LLC converter results in minimized dynamic loss and thus increased overall efficiency, particularly at higher operating frequencies in the hundreds of kilo Hz to Mega Hz range. The figure 1 shows block diagram of the proposed converter.

A full bridge inverter converts the input DC voltage into high frequency AC voltage, which is applied to the resonating network. In this block diagram, the resonant converter includes both the switching circuit and the resonant circuit. The isolation transformer is provided between output of converter and output circuit to provide isolation, since the output of the converter is a high frequency AC. At the output side, a diode bridge rectifier and a capacitor type filter have been used. The capacitor filter of high range is used for efficient filtering operation. The topology is capable of filtering out the DC voltage, which may occur due to the switching period mismatch of the switching devices. Finally the rectified output voltage is given to the load.

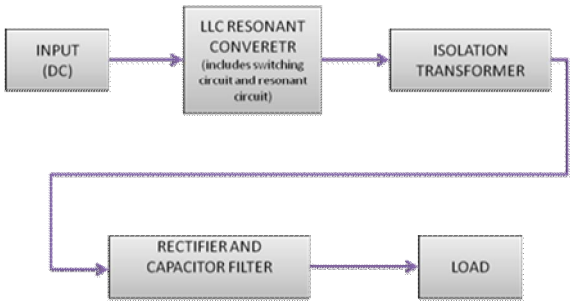

Figure 1. Block diagram of the proposed converter

The figure 2 depicts the circuit diagram of proposed LLC resonant converter.

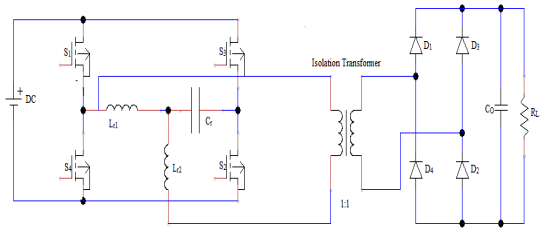

Figure 2. Proposed LLC resonant converter

The switching occurs when the voltage across the MOSFET made zero and resonance is allowed to occur just before and during the turn-on and turn-off processes so as to create ZVS.

2.1 SWITCHING CIRCUIT:

The circuit consists of four switches of MOSFET (capable of operating at high frequency) named as S_1, S_2, S_3 and S_4.The circuit forms a full bridge. This configuration improves efficiency, reduces harmonics. The MOSFET turns on only when GATE pulse is applied to it. The ARDUINO circuit is operated by 5V supply which is capable of generating GATE pulse. The generated GATE pulse is given to the gate terminal of the MOSFET through opto-coupler. Opto-coupler is supplied by 15V supply; also it provides isolation between switching circuit and ARDUINO control circuit.

2.2 RESONANT CIRCUIT AND TRANSFORMER

The resonant circuit is connected between two legs of the MOSFET bridge circuit. The objective of this type of switch is to shape the switch voltage waveform during conduction time in order to create a zero-voltage condition for the switch to turn off. The full-bridge AC-DC resonant converter is formed with S_1, S_2, S_3 and S_4 and a load resonant circuit, which consists of L_{r1} , L_{r2} and C_r in series with an isolation transformer. The transformer is introduced to produce isolation between switching circuit and load circuit. In case if any fault occurs in load circuit it won't affect the switching circuit and vice-versa.

2.3 RECTIFIER AND FILTER

Diodes D_1, D_2, D_3 and D_4 constitute the output rectifier circuit. The voltage that gets from the secondary of the isolation transformer is given to the bridge rectifier. The bridge rectifier rectifies it and supplies it to the load.

III. MODES OF OPERATION OF THE PROPOSED CONVERTER

The figure 3 depicts the circuits for various modes of operation.

MODE 0

From t_0 to t_1,diodes D_1 and D_2 conducts during the –ve half cycle of the resonant capacitor voltage, is clamped to zero by the anti-parallel diode of the switch. At this mode the switches is in off position.

V_{cr} - increases from –ve to 0
i_{Lr1} - increases from 0 to +ve
i_{Lr2} - increases from –ve to 0

MODE 1

From t_1 to t_2, i_{Lr1} and i_{Lr2} transfers from D_1 to T_1 and D_2 to T_2. Thus, T_1 is switched on with zero current and zero voltage. At t_1, T_1 is switched off with finite voltage and current, resulting in turn-off switching loss.

V_{cr} - increases from 0 to +ve
i_{Lr1} - decreases from +ve to 0
i_{Lr2} - increases from 0 to +ve

MODE 2

From t_2 to t_3, D_3 and D_4 conducts during the discharging period of resonant capacitor.

V_{cr} - decreases from +ve to 0
i_{Lr1} - increases from 0 to –ve
i_{Lr2} - decreases from +ve to 0

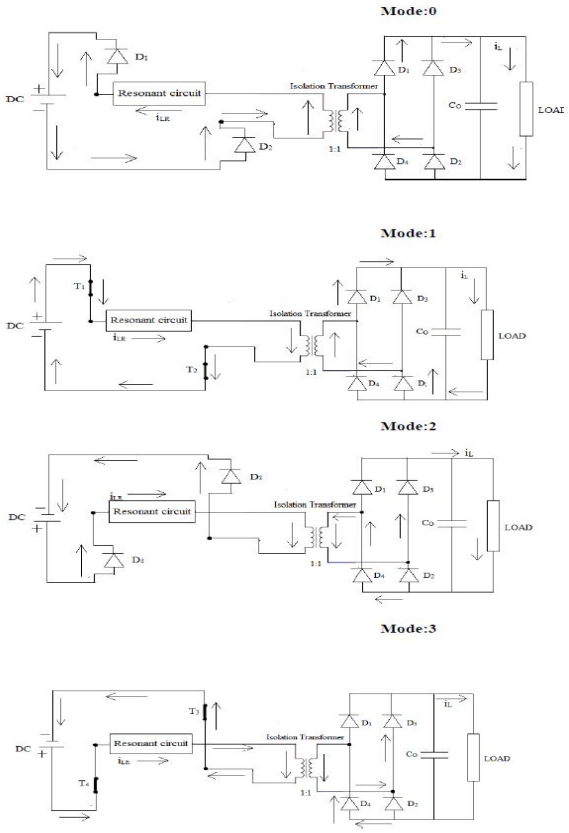

Figure 3. Circuits for various modes of operation

MODE 3

From t_3 to t_4, switches T_3 and T_4 are switched on with zero current and zero voltage. At t_4, T_3 and T_4 is switched off and i_{Lr1} and i_{Lr2} transfers from T_3 and T_4 to D_1 and D_2. As the switches are turned on with ZVS, lossless snubber capacitors can be added across the switches.

V_{cr} - increases from 0 to –ve
i_{Lr1} - increases from –ve to 0
i_{Lr2} - increases from 0 to –ve

IV. PROPOSED LLC CONVERTER TOPOLOGIES

The figure 4 shows the different topologies of LLC resonant circuit.

Topology 1- LLC circuit on primary

Topology 2- LLC circuit on secondary

Topology 3- LLC resonant circuit with L on primary and LC on secondary

Topology 4- LLC resonant circuit with LL on primary and C on secondary

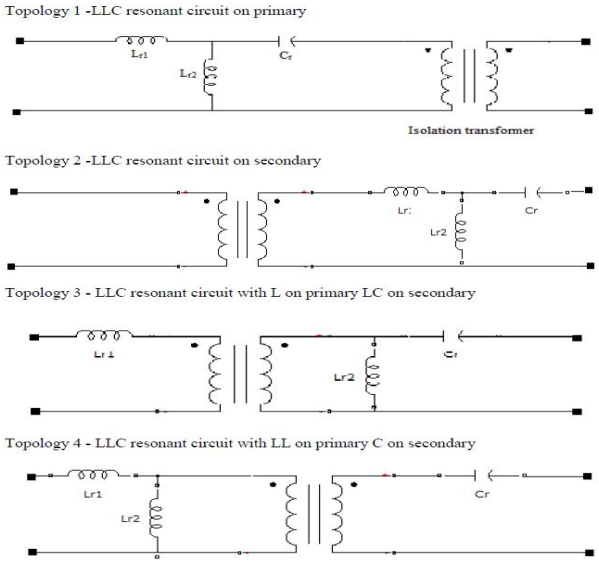

Figure 4. Different topologies of LLC resonant circuit

V. DESIGN OF LLC RESONANT CONVERTER:

The converter components are to be designed for the rated condition. The converter operates very close to the resonant frequency at the rated load. The converter elements are considered ideal with no parasitic. Only E_{in} and E_o are DC, all other symbols for voltages and currents expressed in uppercase letters, indicates AC quantities.

$$v = E_{in} \quad \text{for} \quad 0 < \omega t \leq \pi$$
$$= -E_{in} \quad \text{for} \quad \pi < \omega t \leq 2\pi$$

STEP 1:

The Converter AC voltage gain may be expressed as,

$$\mathbf{M=V_o} / V_{in}$$

With reference to the simplified AC equivalent network, the input AC voltage applied to the LLC network(V_{in}) and the input AC voltage applied to the diode bridge (V_o) may be expressed as,

$$Vin = 2\sqrt{2}/\pi(Ein - 2Vsw)$$
$$V_o = 2\sqrt{2}/\pi(Eo + 2Vd)$$

Although ideally the converter characteristic may be made load-independent at a definite M (i.e. for specified E_o and E_{in}) with corresponding operating frequency but in cases where input voltage undergoes variation (+ΔV), the converter should be designed for the highest M (corresponding to the input voltage E_{in}-ΔV), and the change in the input voltage during operation may be compensated by adjusting the frequency and Pulse Width.

STEP 2:

$$L_{r1} = 8Rfl/\pi^2 \beta\omega$$

$\omega = 2\pi fs$; where, ω corresponds to the operating frequency

Lower magnitude of no-load current improves efficiency at lower load, however makes the converter size bigger. Hence a compromise is necessary.

$R_{fl} = Eo^2 / Po(fl)$; where, R_{fl} corresponds to full load resistance.

Only corresponding to this load resistance the converter is supposed to operate at resonance and for all other load resistances, higher than this, the converter will automatically operate in the lagging power factor mode.

A design parameter "β" is defined as follows to account for the efficiency, instead of calculating the same for a particular device specifications,

$$\beta = \frac{I_{NL}}{I_{FL}}$$

where, I_{FL} is the current through $\mathbf{L_{r2}}$ and $\mathbf{R_{ac}}$ at rated load.

It is obvious that a lower β offers better part-load efficiency. At no-load the expression of the converter input current (i.e. the current through C_r and L_r) becomes,

$$I_{NL} = V_{IN}\pi^2 M\left(\sqrt{M(M-1)}\right)/8R$$

STEP 3: $C_r = M/\omega^2 L_1(M-1)$

STEP 4: $L_{r2} = (M-1)L_1$

STEP 5: $f_r = 1\backslash 2\pi\sqrt{LC}$;

Where, f_r is a resonant frequency of the resonant converter

VI. SIMULATION CIRCUITS AND WAVEFORMS

6.1 TOPOLOGY 1: RESONANT CIRCUIT ON PRIMARY

Figure 5 shows the simulink model of the resonant converter topology I which consists of 4 active switches (S_1,S_2,S_3 and S_4), NOT gate function block, two resonant inductors L_{r1} and L_{r2}, resonant capacitor C_r, isolation transformer, a bridge rectifier and filter capacitor (C_f) and load resistor. Switches S_1 and S_2 are controlled by GATE pulse generated from pulse generator. The operation of this converter is based on the zero voltage switching technique. The performance of the converter depends on the circuit parameters like duty cycle (D), operating frequency (f_s), resonant frequency (f_r), MOSFET tail characteristics. The figures 6 and 7 depict the input waveforms and resonant waveforms of topology I respectively. Also the figures 8 and 9 depict the waveforms across the switch and output waveforms of topology I respectively.

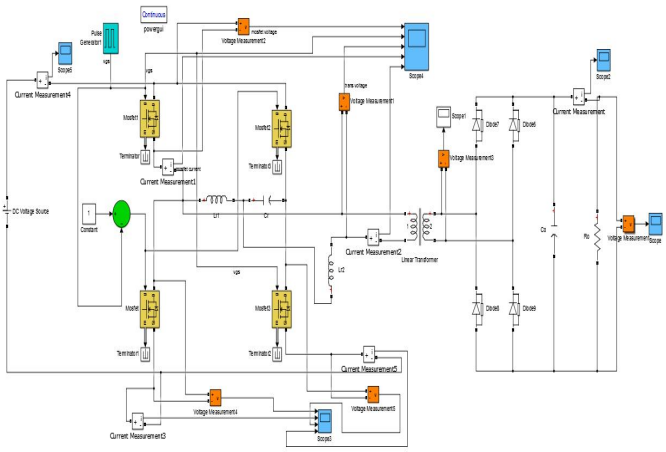

Figure 5. Simulink model of the resonant converter topology I

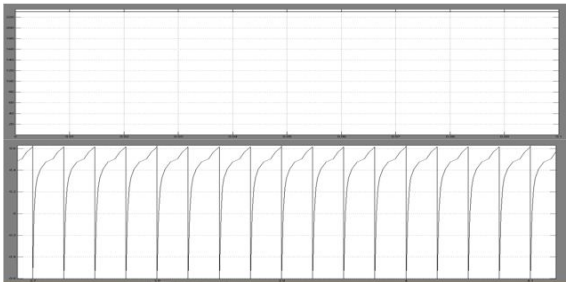

Figure 6.Input wave forms of topology 1 (a) Input voltage and (b) Input current

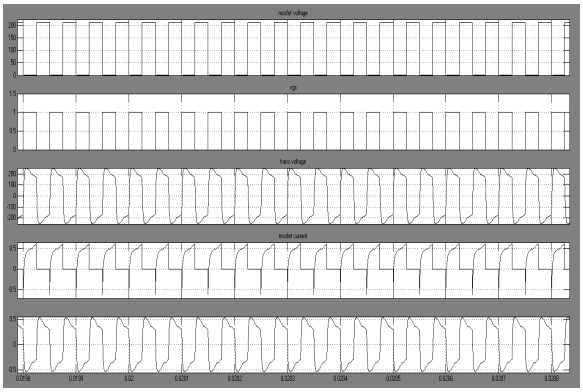

Figure 7. Resonant wave forms of topology 1 (a)Voltage across MOSFET (b) Gate pulse 1 (c) Resonant voltage (d) Current through MOSFET 1 and (e) Resonant current

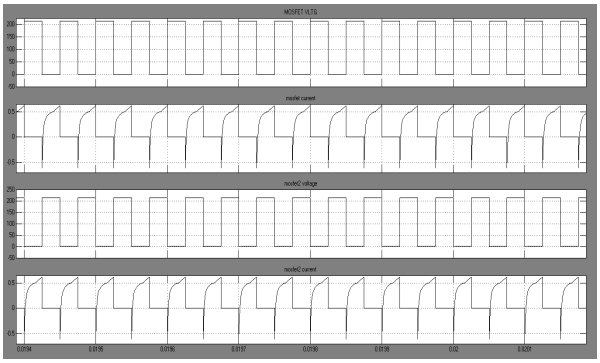

Figure 8. Wave forms across the switch of topology 1 (a) Voltage across the switch 2 (b) Current in switch 2 (c) Voltage across the switch 4 (d) Current in the switch 4

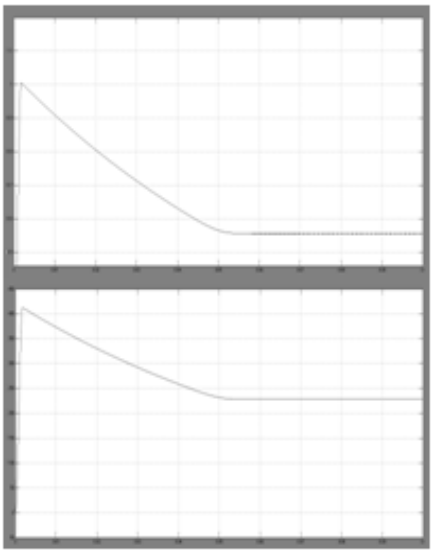

Figure 9.Output wave forms of topology 1 (a) Output voltage and (b) Output current

From the waveforms it's inferred that for a given 230V as input, the ouput peak voltage is VP =415 V and it settles at 248V. The peak voltage occurs due to the switching circuit. From the magnitude and output voltage waveform of topology I it infers that, the topology is efficient among other topologies and reduced ripples.

Thus from the output voltage and current waveform it's clear that the topology II is close to topology I ,but with little lower magnitude. The drop occurs due to the separation of switching and resonant circuit.

6.2 OBSERVATIONS FROM SIMULATION RESULTS

The table 1 gives the details about comparison of different topologies which shows input voltage, input current , output voltage and output current of four different topologies of resonant converter.

Table 1 Comparison of different topologies

Topology	Input Voltage Vi (Volts)	Primary Voltage= Secondary voltage (Volts)	Output Current (Amps)	Output (load) Voltage (Volts)
I (LLC on primary)	230	255	0.539	248
II (LLC on secondary	230	255	0.6	247.5
III (L on primary)	230	15	0.35	14.5
IV (LL on primary)	230	15	0.363	14

Table 2 Comparison of efficiency and switching losses of the resonant converter topologies

Input power (P_{in}) (Watts)	Output Power (P_o) (Watts)	Efficiency (Ⴖ) in %	Switching Losses of MOSFET (Watts)
138	150	98.7	1.12
128.06	148	98	1.48
50.3	5.1	10.4	1.03
71.3	5.5	13.09	1.028

From the tables, it is inferred that the topology I is efficient and switching losses are less, topology II is second efficient circuit. The topologies III and IV are less efficient due to the poor conversion between primary and secondary. It is inferred from the simulation results that the output voltage of topology 1 and topology 2 are higher than the remaining two topologies. Hence the topology 1 has been chosen to build a proto type.

VII. PERFORMANCE ANALYSIS OF RESONANT CONVERTER

The performance of topologies I and II are analyzed in terms of variation in efficiency and switching losses for different values of duty cycle.

7.1 FORMULAE:

1. Efficiency(Ⴖ) = Output power(P_o) / Input power(P_i)
2. Switching losses

$$[((t_{on} . V_{off} . I_{on} . f_s)/2) + ((t_{off} . V_{off} . I_{on} . f_s)/2)]$$

where, t_{on} – Turn-on time of MOSFET;

t_{off} – Turn-off time of MOSFET

V_{off} – Drain to Source voltage when switch is off

I_{on} – Drain current when switch is on

f_s - Switching frequency

7.2 Efficiency and switching loss curves of Topology I and Topology II

The fig 10 (a) and 10 (b) show the efficiency and switching loss Vs duty cycle curves of topology I

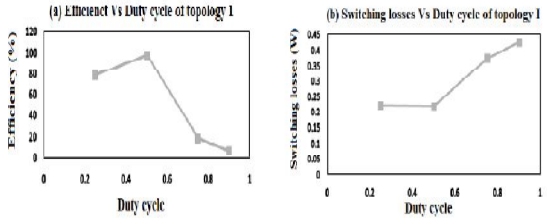

Figure 10 (a) Efficiency Vs duty cycle and 14 (b) Switching loss Vs duty cycle curves of topology I

The fig 11 (a) and 11 (b) show the efficiency and switching loss Vs duty cycle curves of topology I

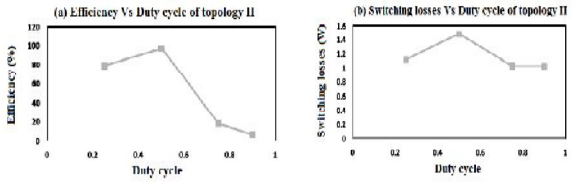

Figure 11 (a) Efficiency Vs duty cycle and 11 (b) Switching loss Vs duty cycle curves of topology II

The performance analysis is done based on the data of comparison table which is shown above. Thus from the above curves it is inferred that at 50% of duty cycle the topology I works satisfactorily.

VIII. HARDWARE IMPLEMENTATION

This section describes the practical implementation of the Topology I of LLC resonant converter that has shown in figure.2 .The input (V_{in}) and output voltages (V_o) and the voltage stress across switches S1,S2,S3 and S_4 were measured using multi-meter. The GATE pulses are observed using CRO.

8.1 HARDWARE SETUP:

The hardware setup of the AC-DC resonant converter is shown in Fig.12. The gating pulse from ARDUINO is given to the MOSFET switches through the opto-coupler. The opto-coupler is supplied by 12V to drive the circuit. The input to the converter is taken from a 230/24V step-down transformer. Opto-coupler circuit provides isolation between switching circuit and control circuit. Opto-coupler circuit consists of four IC's of TLP250. The circuit works when 15V regulated supply is given to it. The supply is given through the step-down transformer.

From the secondary of the transformer the voltage is given to the diode bridge rectifier, to converter the input AC to DC to supply the converter circuit . The rectified voltage is given to resonance circuit. The output of the resonance circuit is AC which is given load circuit through the bridge rectifier and filter. The output of rectified voltage is given to the MOSFET drain terminal.

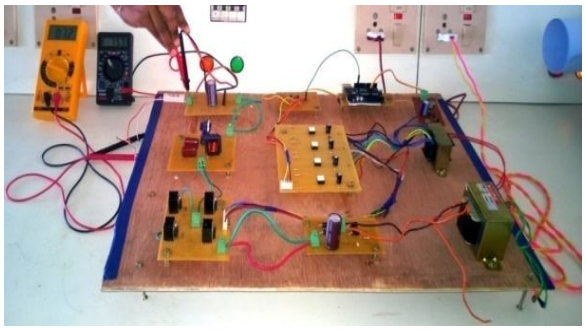

Fig.12 Hardware set up of the proposed Topology I

8.2 PULSE GENERATION CIRCUIT

The figure 13 depict the output pulse waveform observed through CRO. The pulse generation circuit is used to give the GATE pulse to turn the MOSFET ON. The GATE pulses are supplied from ARDUINO circuit . The output of the ARUDINO is taken from pin no:13(PWM output). Pins 1 and 7 are connected to the supply voltage +5V. Pins 8 and 22 are connected to GROUND. A NOT gate function is included in the circuit to NOT the input GATE signal for 2 MOSFET's. When output of the circuit is 1, it enables the MOSFET's 1 and 2 at that time not function works and inverts the signal to other two MOSFET's.

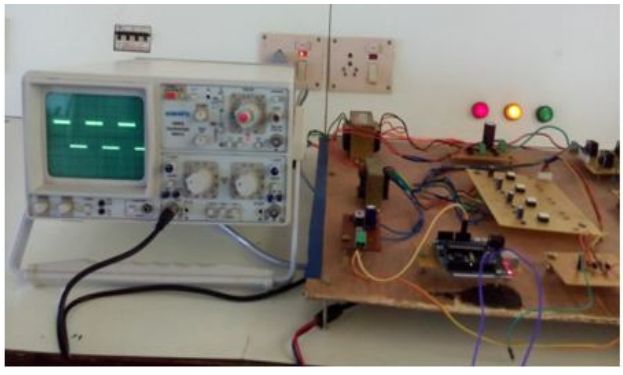

Fig.13 output pulse waveform

IX. CONCLUSION

The performance analysis of LLC resonant converter using ZVS technique is presented. The proposed circuit is derived based on the integration of a diode bridge rectifier, full bridge MOSFET switching circuit with LLC resonant converter. The active power switches are designed to operate at ZVS to ensure high efficiency. The proposed converter has intrinsic benefit of low switching losses and high efficiency. The circuit operation of AC-DC resonant converter is studied and analyzed through the MATLAB simulation. The prototype of resonant converter of Topology I (LLC resonant circuit on primary) is implemented in order to verify the simulation results. Zero current switching (ZCS) technique could be used instead of ZVS. Also CCL resonant converter circuit can be used instead of LLC resonant converter.

REFERENCES

[1] Chandan Chakraborty, Muneaki Ishida and Takamasa Hori, "Performance, Design and Pulse Width Control of a CLL Resonant DC/DC Converter Operating at Constant Frequency in the Lagging Power Factor Mode" , IEEE 1999 International Conference on Power Electronics and Drive Systems, PEDS'99, July 1999.

[2] Fred Lee, Kwang-Hwa Liu, "Zero Voltage Switching Techniques in DC/DC Converter" IEEE Transactions on Power Electronics, Vol 5, July 1990.

[3] S.K.Parimala., M.S. Aspalli and Laxmi Deshpande, "High frequency DC-DC converter design using Zero Voltage Switching" , International Journal of Science, Environment ISSN 2278-3687 (O) and Technology, Vol. 3, No 2, pp.621 – 629, 2014.

[4] P. Sudhrasana Rao, C. Nagakotareddy, "An Enhanced ZVS & ZCS Full Bridge Converter With Resonance Circuit In The Secondary Winding For High Power Applications", International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 3, Issue 4, pp.1996-2001, July-August 2013.