DESIGN OF LOW POWER FLIP-FLOP USING ADJUSTABLE VOLTAGE CIRCUIT TECHNIQUE

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Abstract- *The proposed system describes the power reduction in flip-flop. The system uses a technique called adjustable voltage circuit (AV circuit). The power reduction is achieved by combining the AV circuit with the D-Flip Flop. Adjustable voltage circuit can be applied to any load circuit. D Flip Flop is the load circuit in this project. Supply voltage Vdd is connected to adjustable voltage circuit. The AV circuit supplies a maximum DC voltage to an active load or decrease the dc voltage supplied to the load circuit in standby mode. Furthermore this AV circuit can be applied in Memories and Registers. This paper investigates the effectiveness of flip flop with this technique. The power reduction has been achieved upto 12%. The flip flop design has been carried out using 180 Nano scale technology. The circuit has been simulated by using the Tanner EDA tool.*

Key words—*Flip-flops, low-power, VLSI.*

I. INTRODUCTION

The mobile market keeps on expanding. In addition to the conventional mobile phone, digital camera, and tablet PC, development of various kinds of wearable information equipment or healthcare associated equipment has newly prospered in recent years. Today's technologies make possible powerful computing devices with multi-media capabilities. Consumer's attitudes are gearing towards better accessibility and mobility. Their desire has caused a demand for an ever-increasing number of portable applications requiring low-power and high throughput. For example, notebook and handheld computers are now made with competitive computational capabilities as those found in desktop machines. It is important that these high computational capabilities are placed in a low-power, portable environment. The weight and size of these portable devices is determined by the amount of power required. The battery lifetime for such products is crucial , hence, a well planned low-energy design strategy must be in place. In order to meet the demand in high computational applications, the clock rate is steadily increasing, with clock jitter and clock skew being an increasingly significant part of the clock cycle. The energy consumed by low-skew clock distribution networks is perpetually growing. In addition, the number of logic gate delays in a clock period is reduced by 25% per generation, and is approaching a value of 10 or smaller beyond 0.13 μm technology generation. As a result, latency of flip-flops or latches is becoming a larger portion of the cycle time. In order to achieve a design that is both high performance and power efficient , careful attention must be paid to the design of the flip-flop and latches.

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II. CONCEPT OF EXSISTING SYSTEM

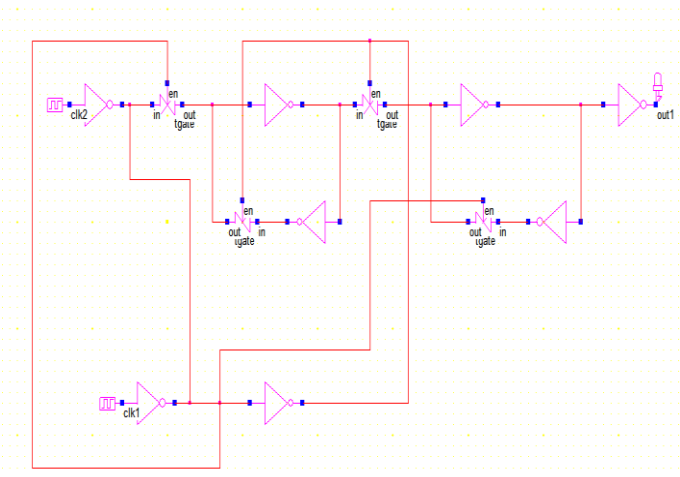

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Fig. 1. Conventional transmission-gate flip-flop (TGFF).

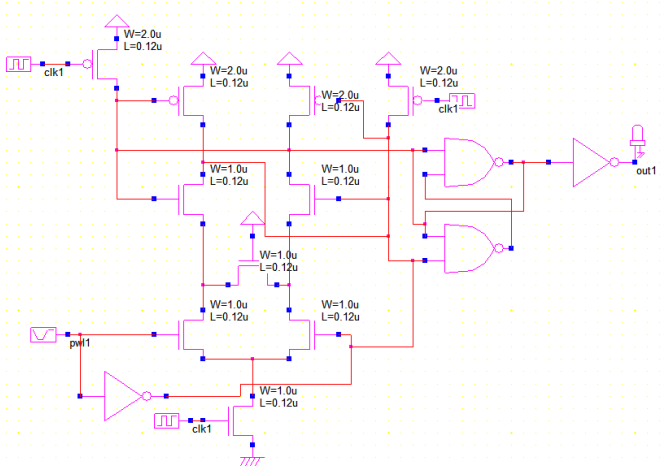

Fig. 2. Differential sense-amplifier flip-flop (DiffFF).

Here we analyze problems on previously designed typical low power flip-flops with comparison to a conventional flip-flop as in Fig.1. The Fig. 2 shows a typical circuit of differential sense- amplifier type FF (DiffFF). This circuit is very effective to amplify small-swing signals and so it can be used in output part of memory circuits. In this type of flip-flop , the effect of power reduction degrades if the data activity is low, because these kind of circuits have pre-charge operation in every clock-low state. Eventhough if we use reduced clock swing, then it requires a customized clock generator and an extra bias circuit.

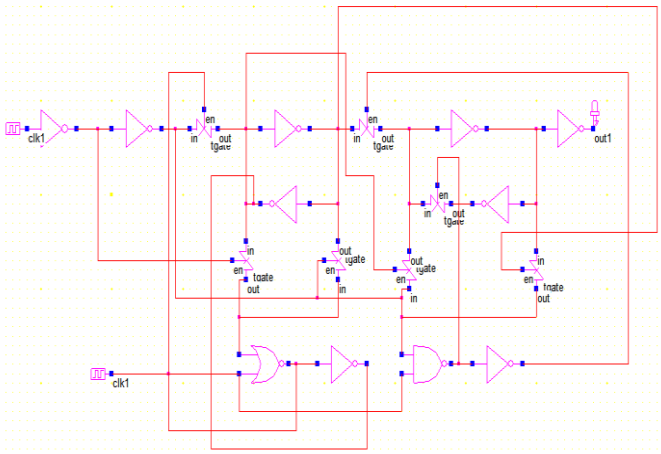

Fig. 3. Conditional-clocking flip-flop (CCFF).

Figure 3 shows a circuit of conditional- clocking type flip-flop (CCFF). This circuit monitors the change in input data at each and every clock cycle. If the input data are not changed then the circuit disables the operation of internal clock. By this operation, the power can be reduced when the input data are not changed. But the drawback is that the cell area doubles that of the conventional circuit shown in fig.1. and mainly due to this size issue , it becomes hard to use if the logic area is relatively large in the chip.

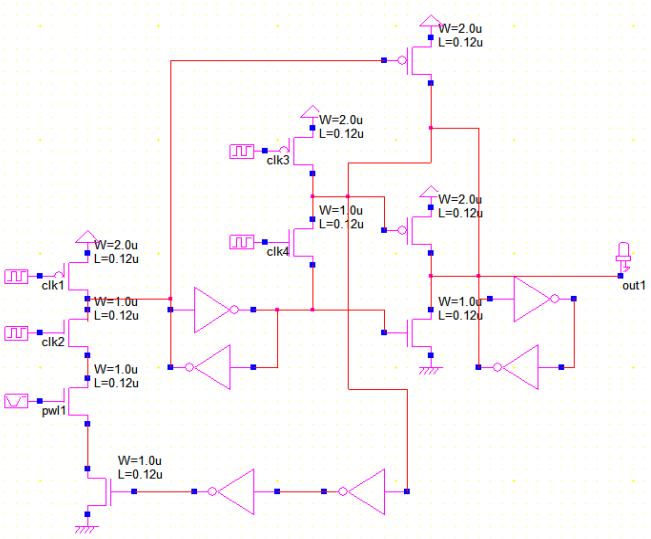

Fig. 4. Cross-charge control flip-flop (XCFF).

Fig. 4 shows the circuit of cross-charge control FF (XCFF) [7]. The feature of this circuit is to drive output transistors separately in order to reduce charging and discharging of gate capacitance. However during actual operation, some of the internal nodes are pre-set with clock signal if the data is high, and this operation dissipates extra power to charge and discharge internal nodes. As a result, the effect of power reduction will decrease.

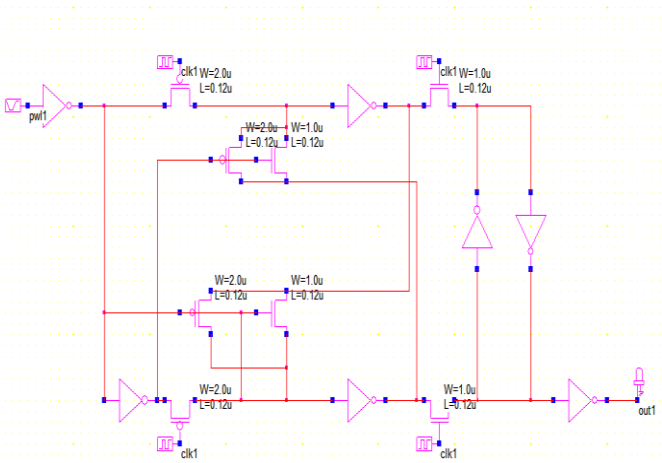

Fig. 5. Adaptive-coupling flip-flop (ACFF).

The figure5 shows the adaptive coupling type flip-flop which is based on a 6 transistor memory cell. In this flip-flop, the double channel transmission gate is replaced by a single-channel transmission gate with additional dynamic circuit which has been used for the data line in order to reduce the clock related transistors. But here the delay gets affected easily by input clock slew variation because different types of single channel transmission gate are used with the common data line and clock signal. Moreover , characteristics of single channel transmission gate circuits and dynamic circuits are strongly affected by process variation. Therefore, their optimization is very difficult, and performance degradation across various process occurs.

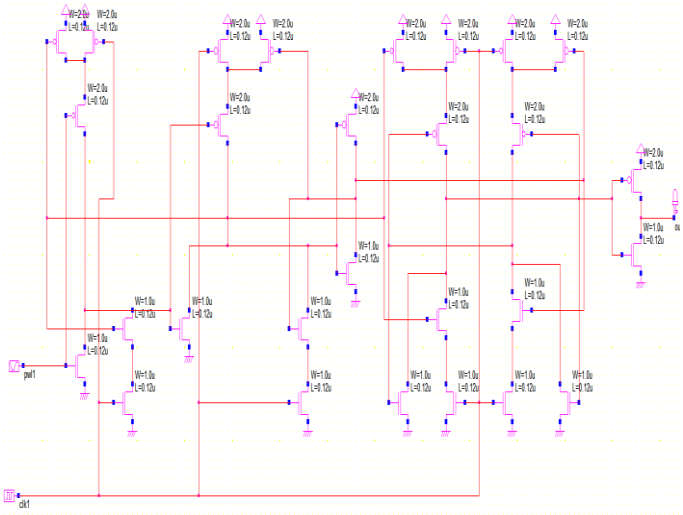

Fig. 7. Transistor level schematic of Fig. 6

The power of the FF is mostly dissipated in the operation of clock-related transistors, and reduction of transistor count is effective to avoid cell area increase and to reduce load capacitance in internal nodes. In the conventional FF shown in 12 transistors are 12 clocked transistors. It is quite difficult to reduce the clock-related transistor directly from this circuit. One reason is because transmission-gates need a 2-phase clock signal, thus the clock cannot be eliminated. Another reason is that transmission-gates is constructed by both PMOS and NMOS to avoid degradation of data transfer characteristics caused by single-channel MOS usage. There-fore, instead of transmission-gate type circuit, we consider a combinational type circuit as shown in Fig. 6. To reduce the transistor-count we consider a method consisting of the following two steps. The first step is to have a circuit with two or more logically equivalent AND or OR logic parts which have the same input signal combination, especially including clock signal as the input signals. Then, merge those parts in transistor level as the second step.

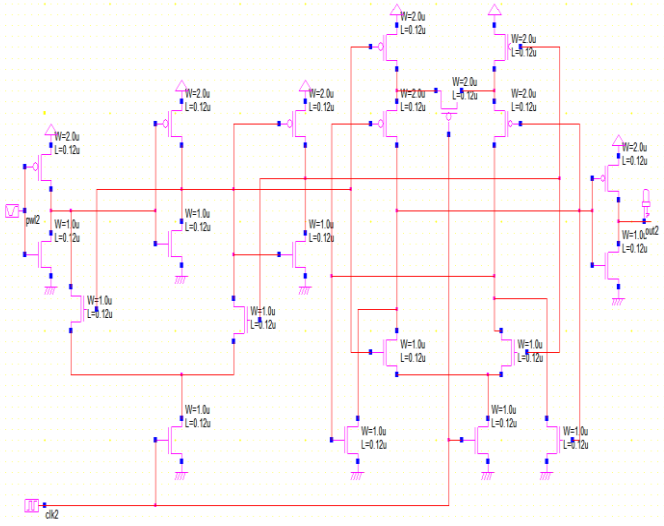

Fig.6. Transistor level schematic of topologically-compressed flip-flop (TCFF).

IV . CONCEPT OF PROPOSED FLIP-FLOP

4.1 ADJUSTABLE VOLTAGE CIRCUIT

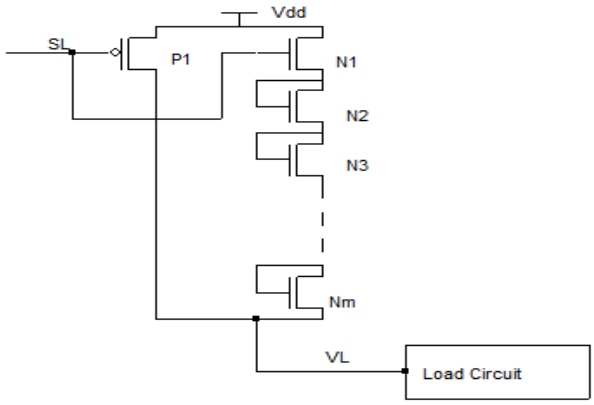

Fig 7 Adjustable voltage circuit

Adjustable voltage circuit that consist of parallel connection of PMOS transistor and NMOS transistors. Nmos transistors are connected in series. The ‘m ‘ number of NMOS transistors can be connected in this series connections. As the number of NMOS transistor increased the drain to source voltage of the OFF NMOS transistor

decreased. There by the supply voltage reduces and in turn power consumption reduces.

4.2 DESIGN APPROACH

In order to reduce the power of the FF while keeping competitive performance and similar cell area, we tried to reduce the transistor count , without introducing any dynamic or pre-charge circuit. The two master and two slave configuration flip-flop is replaced by one master one slave. Circuit contains four clocked transistors. During ON and OFF of the clock pulse the each transistor node get charged and discharged respectively. Unwanted charging and discharging of the transistors leads to increase the power consumption. To reduce this effect clocked transistors are considerably reduced.

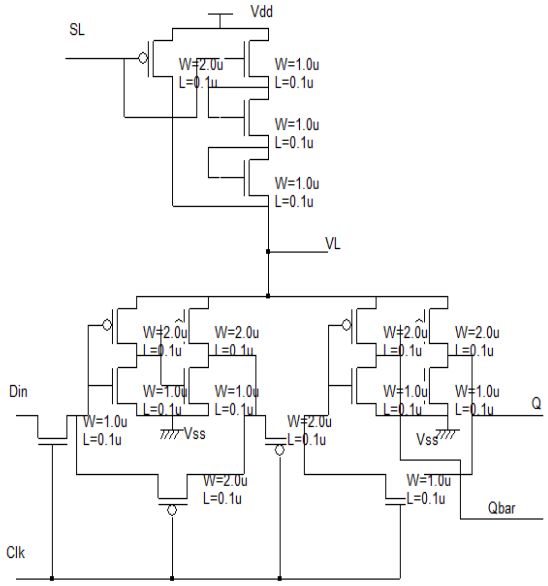

Fig 8 Flip-flop with adjustable voltage circuit

The master and slave part of the flip-flop circuit separated by a pmos transistor. This flip flop circuit is connected as a load circuit to the adjustable voltage circuit. Any circuit can be used as a load for adjustable voltage circuit. The power of the FF is mostly dissipated in the operation of clock-related transistors, and reduction of transistor count is effective to avoid cell area increase and to reduce load capacitance in internal nodes. In the conventional FF, there are 12 clock-related transistors. To reduce clock-related transistor counts directly from this circuit is quite difficult. One reason is because transmission-gates need a 2-phase clock signal, thus the clock driver cannot be eliminated. Another reason is that transmission-gates should be constructed by both PMOS and NMOS to avoid degradation of data transfer characteristics caused by single-channel MOS usage.

V. SIMULATION RESULTS

a)CIRCUIT OPERATION:

Adjustable voltage circuit in which VDD is the supply voltage and VL is the output voltage of this circuit and it can be applied to any load circuit. During the active mode (when SL=0) , this circuit supplies maximum supply voltage to the load circuit through the ON pmos transistor P1 so the load circuit can operate quickly. During the standby mode (when SL=1) , it provides slightly lower supply voltage to the load circuit through the weakly ON nmos transistors (N1,N2,…Nm). Voltage applied to the load circuit is given by

$$VL=VDD-Vn$$

Where Vn is the voltage drop of m weakly ON NMOS transistors.

b)EXISTING METHOD

The simulation output of Transmission gate flip-flop is shown below

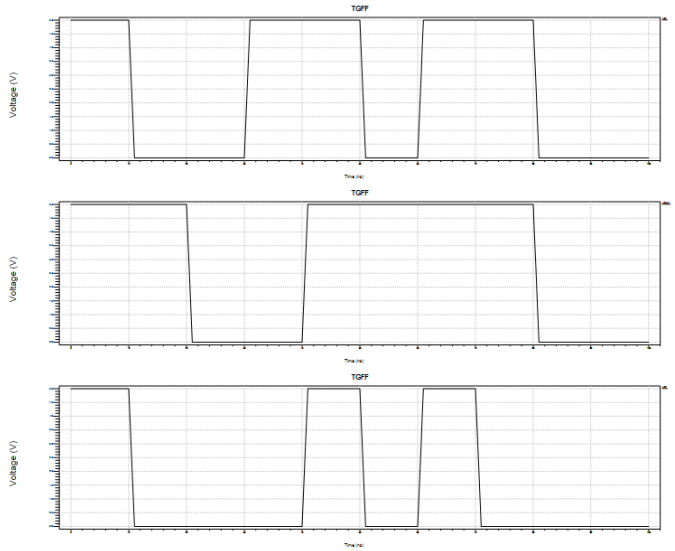

Figure 9 Output of Transmission Gate flip-flop

The simulation output of Differential flip-flop is shown below

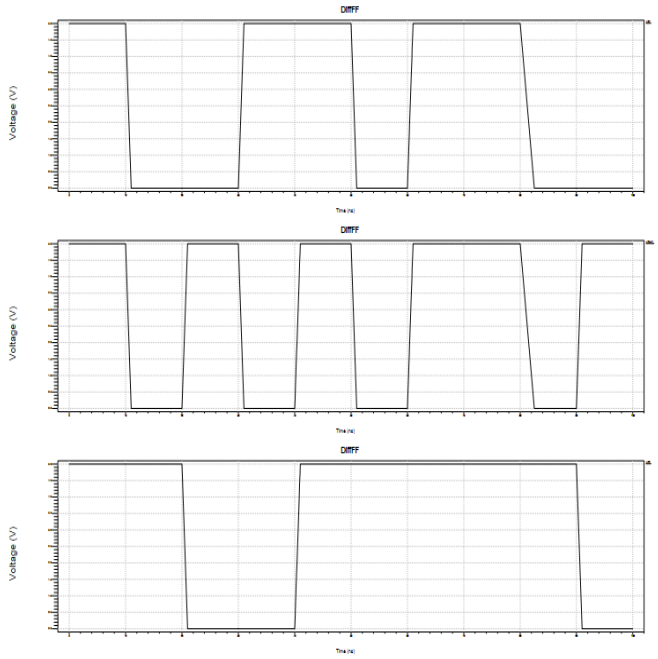

Figure 10 Output of Differential flip-flop

The simulation Output of Conditional Clocking Flip-flop is shown below

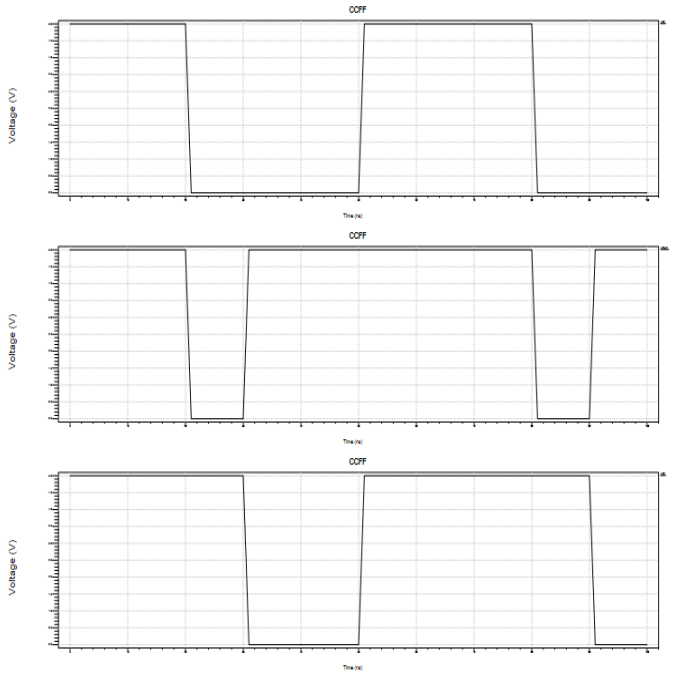

Figure12 Output of Conditional Clocking flip-flop

The Simulation output of Cross Charge Control Flip-flop is shown below

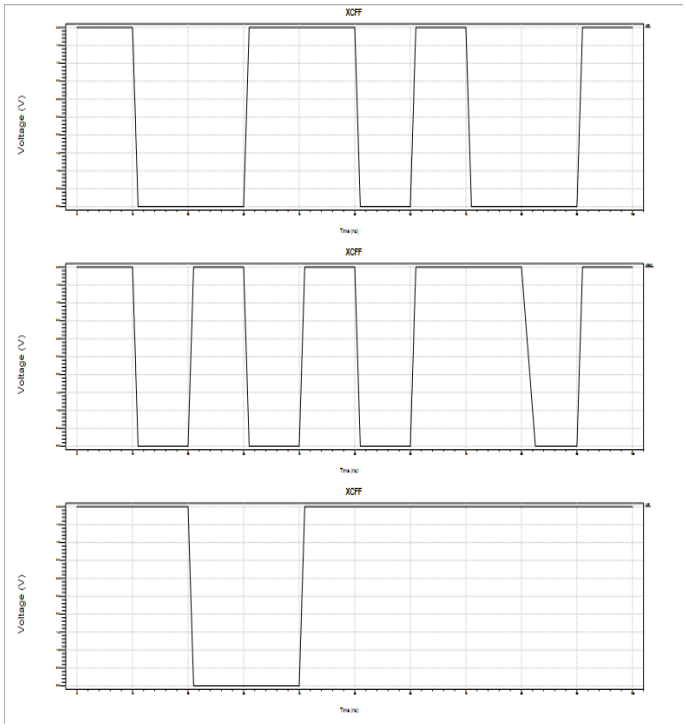

Figure 11 Output of Cross Charge Control flip-flop

The Simulation output of Adaptive Coupling Flip-flop is shown below

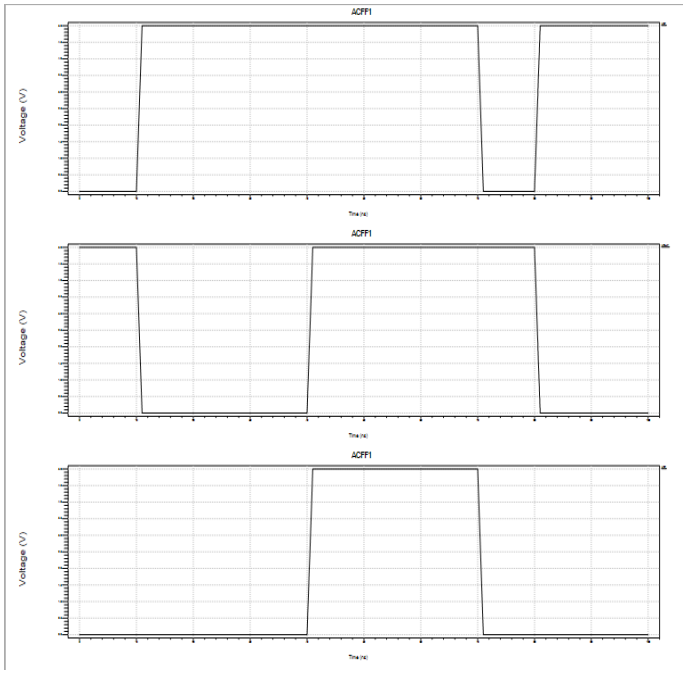

Figure 13 Output of Adaptive Coupling flip-flop

c)PROPOSED METHOD

The simulation Output of 28Transistor flip-flop is shown below

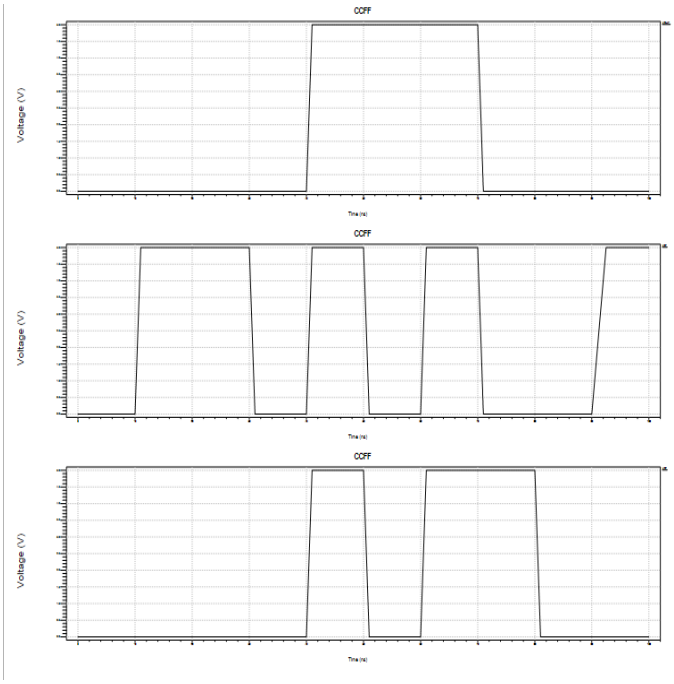

Figure 14 Output of 28Transistor flip-flop

The simulation output of Topologically Compressed Flip-flop is shown below

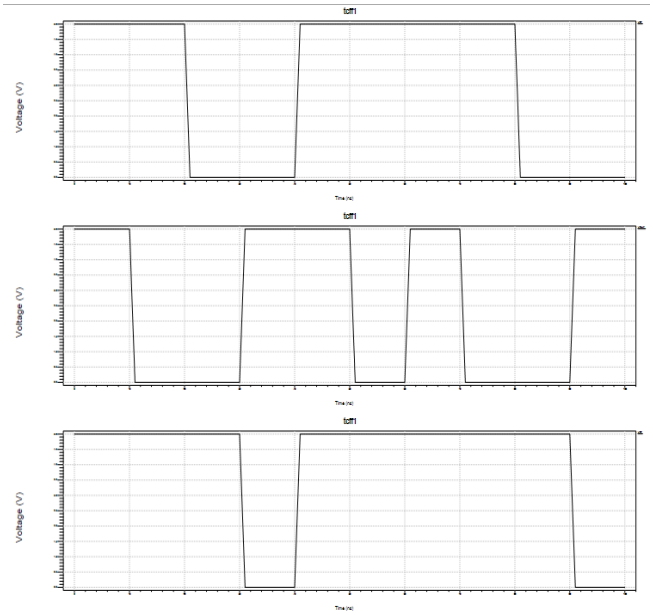

Figure 15 Output of Topologically Compressed flip-flop

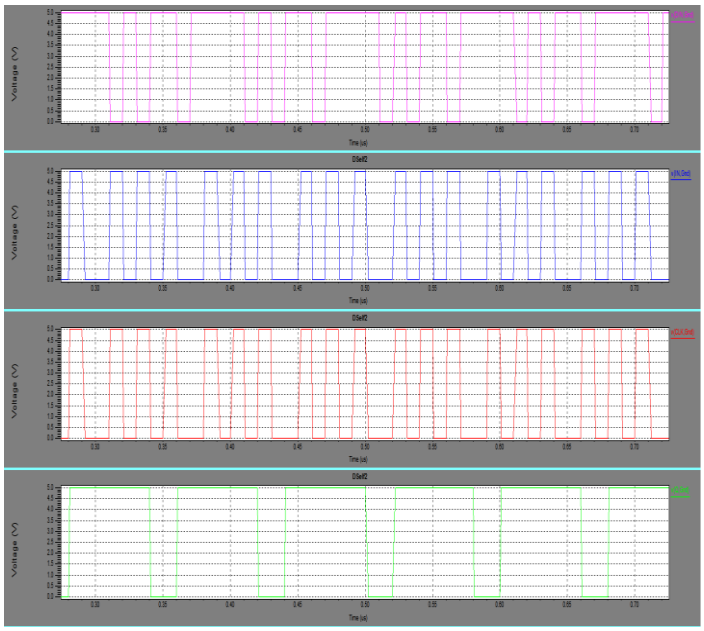

Figure 16 Output of flip-flop with adjustable voltage circuit

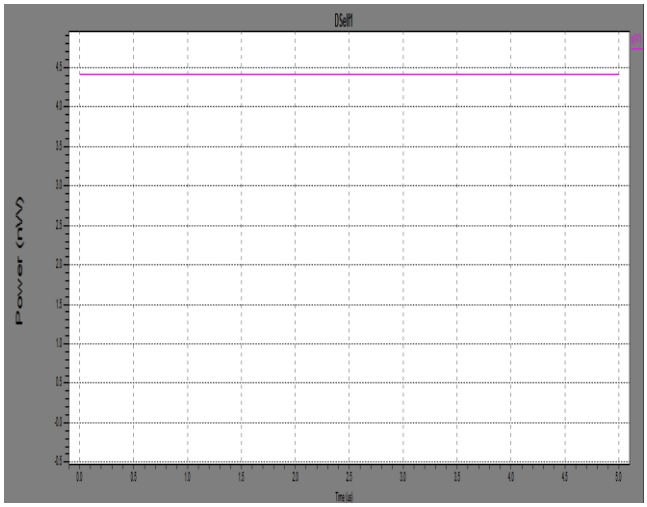

Figure 17 Power output

6.3 POWER COMPARISON BETWEEN FLIP-FLOPS

Parameters	Existing method	Proposed method
No. of transistors	21	16
Power consumption	3.58mW	4.5nW

Table 6.10 Comparison of flip-flops

6.4 LAYOUT FOR THE PROPOSED FLIP-FLOP

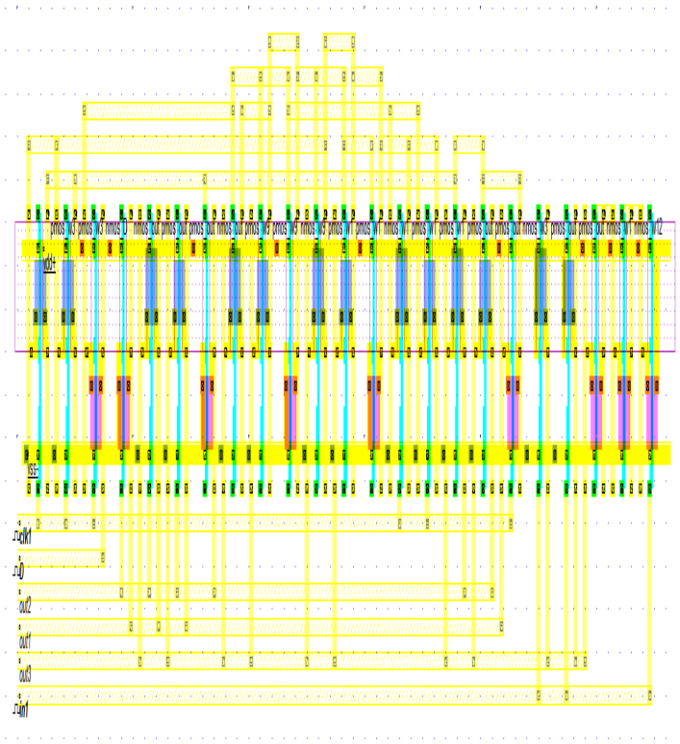

Fig 18 Layout of the flip-flop with adjustable voltage

6.5 DELAY ANALYSIS

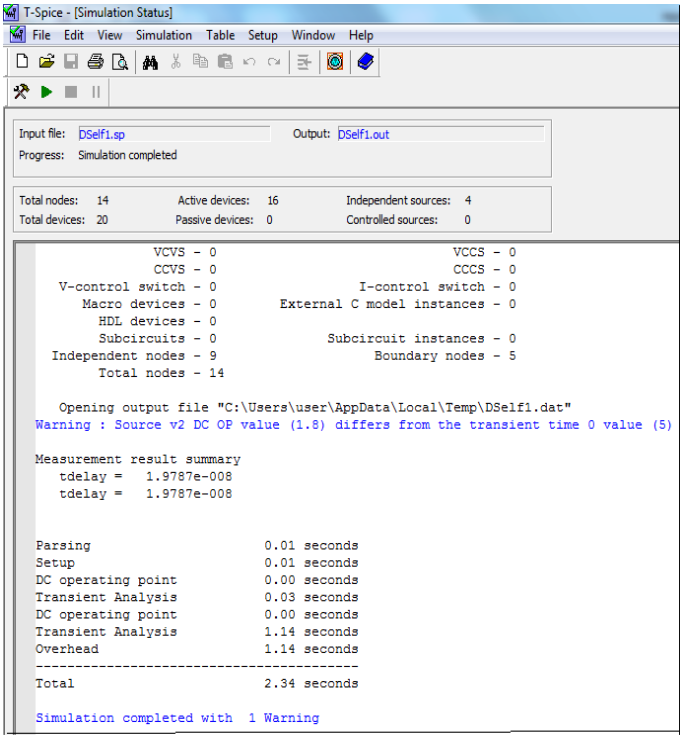

Figure 19 Delay analysis

VII. CONCLUSION

The low power flip-flop is compatible with the conventional process is proposed to save upto 12% of the total power consumption. compression design methodology. The delay value has been obtained for this flip flop is 1.9787e-008s. Power value that has been calculated by the software tool is 4.5nW. The topology of adjustable voltage circuit is easily expandable to various kinds of FFs without performance penalty. In summary, this flip flop can be applied to various speed systems, and it can reduce whole chip power more effectively. In future we can add some other leakage reduction techniques and the power can be further reduced. Furthermore the work can reduce the power consumption by using low swing voltage approach.

VIII. REFERENCES

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