Study on Capacitor-Less Low Drop Out Regulator Using 90-nm Technology

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Abstract- *The problem encountered in some papers is of low slew rate, power supply rejection ratio, line and load regulations, high quiescent current, settling time, and load current. Generally, due to these parameters LDO suffers with low battery life. A capacitor less programmable LDO is presented, which improves these parameters and reduce the power consumption by reducing the quiescent current and drop out voltage.*

Keywords- Capacitor-less LDO, low drop out voltage regulator, PSRR, SR.

I. INTRODUCTION

A low drop out regulator is a DC linear voltage regulator which can operate with a very small input output differencial voltage. The low drop-out regulators are the essential building block of portable electronic devices such as laptops, mobile phone, biomedical implantable devices such as pacemaker, ECG, EEG and EMG etc. A series low-drop-out regulator provides a specified and stable dc voltage, whose input to output voltage difference is low. The drop-out voltage is defined as the value of the input/output differential voltage where the LDO stops regulating. A Power transistor (pass device) is connected in series between the input and the output terminals of the regulator that's why it termed as series voltage regulator. Low drop-out (LDO) regulators can be divided as either low power or high power. Low power LDOs are typically those with a maximum output current of less than 1 A, exhibited by most portable applications. On the other hand, high power LDOs can yield currents that are equal to or greater than 1 A to the output, which are mainly demanded by many automotive and industrial applications. Conventional LDOs are typically implemented with at least one feedback loop which is stabilized using a huge external capacitor.

II. TYPES OF LDO

There are two types of LDOs based on capacitor as follows:

2.1) Low Drop Out Regulators with Capacitor

Reduces output noise, the output voltage variation and improves PSRR. But it also has some disadvantages that use of capacitor increases the chip area, affects the stability of LDO regulator, affects on a large load transient response, affect during shut-down, there is also low start-up issue.

2.2) LDO without capacitor

Present research in LDOs is focused on removing this external capacitor while maintaining stability, good transient response and high power supply rejection performance.Capacitor free low drop-out regulators have several advantages over the low drop-out regulators with capacitance on the basis of small size and portability.

III. PEER REVIEWED

A stable LDO voltage regulator with a novel Double Recycling Error Amplifier structure is presented which enhance the slew rate [1] but with increased quiescent current. Few authors reduces the value of quiescent current by designing LDO with push pull composite power transistor [2] which is having low PSR that indicate low output supply voltage irrespective of supply voltage. High PSR of -95dB at 5MHz have been achieved by paper [3] which is integrated with medical body area network (MBAN) transceiver having drop of 300mV. Since minimum dropout is the requirement of many applications, so drop out of 200 mV has been shown by paper [4] having low values of load and line regulations. Better line and load regulations of 3.2 mV/V and 12 mV/A is presented in paper [5]. In this paper the settling time is more which is reduced by paper [6] because settling time is also one of the important parameter while considering LDO. The driving capability of LDO is such that it should be able to drive the particular application like MCU, so the paper [7] shows authors. Area efficient capacitor less LDO is presented by paper [8].

IV. PROBLEM FORMULATION AND OBJECTIVE

The problem encountered in the performance of LDO is that the low power devices such as laptop, smart phones, medical devices, micro-controller units etc. consume large load current and during working as well as sleep mode, they have been leakaging large current which causes the low

battery life.The objective of our paper is to increase the values of slew rate, PSR, load and line regulations and also decrease drop out voltage, quiescent current, settling time, area, and load current by using 180 nm technology. Next objective will be to obtain the values of these parameters by adding the feature of programming and by using 90 nm technology.

V. PROPOSED METHODOLOGY

To achieve our objectives, we will device a method to get our required parameters. So, I will connect another error amplifier to the substrate of pass element using 180 nm technology. Fig.2 shows the block diagram of proposed LDO voltage regulator.

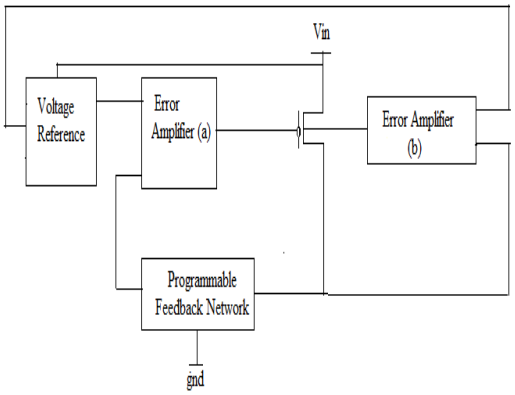

Fig 2 Block diagram of proposed LDO voltage regulator

Error Amplifier:

Error amplifier is just an operational amplifier which is made up of folded cascade type because this amplifier provides high slew rate and power supply rejection ratio. It also solves the problem of limited bandwidth of conventional LDO. The LDO consist of two error amplifier: one is connected to the gate of pass transistor and another to the body of pass transistor.

Programmable Feedback Network:

In our proposed method, we will use programmable feedback network in order to achieve the variable output voltages or required output. Feedback network is made programmable by adding extra resistors (R_3, R_4) with NMOS in parallel with R_2.

VI. CONCLUSION

In this paper a capacitor-less LDO voltage regulator is proposed by using an IBM 90-nm technology. In our proposed method PSRR and other performance parameters will be improved by using another error amplifier. This LDO will also reduce the quiescent current or ground current and dropout voltage which are the basic needs of any power management system.

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