Comparative Analysis of CMOS Low Noise Amplifiers in 45 nm VLSI technology

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Abstract- *The paper represents simulation and design of Low Noise Amplifier in a 45nm CMOS technology at 77 GHz frequency. Here we have proposed a comparative analysis of single ended and current reuse LNA. The LNA function is used to amplify signals without adding noise. It also preserve required signal to noise (SNR) ratio. Cadence design tool Virtuoso is used to simulate and design the circuit using transistors, resistors, inductors and capacitors. By usingsingle ended Low Noise amplifier, we can obtain forward gain (S21) having value of 2.34dB with noise figure and stability factor of 12.45dB and 2.47 respectively and it draw 2.1mW power from supply of 1.1V. The Current Reuse LNA gives a forward gain having value of 8.12dB with noise figure and stability factor having values 9.8dB and 3.99 respectivelyand it draw 1.5mW power from supply of 1.1V.*

Keywords- power dissipation; impedance matching; low noise amplifier; noise figure.

I. INTRODUCTION

Radio frequency is the frequency range defined in the electromagnetic frequency spectrum,mainly used for radio communications. It lies typically from 100 KHz to 100 GHz. However the frequencies which are below 1 GHz are considered as baseband frequencies and those which are greater considered as Radio frequencies (RF). The radio frequency (RF)signals received by receiver's antenna are weak. Thus, an amplifier with good noise performanceandhigh gain is required to amplify the signal so that it can be fed to the other parts of receiver for processing. Such amplifier is known as a Low Noise Amplifier (LNA) and forms an essential component of any RF integrated circuit receiver [3] [4]. Generally, the main goal of LNA design is to achieve simultaneous a low noise and high power gain for the given power dissipation and frequency condition. There are many fundamental low noise amplifier (LNA) topologies for single ended and narrow band design, such as resistive termination common source, common gate, shunt series feedback common source, inductive degeneration common source, cascade inductor source degeneration[5].

The design is based on a cascade configuration including feedback to the common source amplifier for simultaneous noise and input impedance matching. This paper describes theoperation and the simulation of s parameters, gain and minimum noise figure using 45nmCMOS technology.

II. LNA DESIGN

A. Low Noise Amplifier Topology

Out of the several topologies for narrow band single ended LNA design, an appropriate topology should be selected for low power and low voltage optimized LNA design. For common gate topology, the gain is lesser in very low power consumption. For shunt series feedback common source topology, it is difficult to trade off among noise figure, amplifier gain and good input-output matching in very low power consumption. Using resistor terminationtopology with common sourceintroduces noise to low noise amplifierdue to the thermal noise generated in resistors [5].Isolation is not enough as compared to cascade inductor degeneration topology, which can get the similar low noise amplifier performance in very low power consumption. Above all, the cascade inductor source degeneration topology is selected for this design.

B. Single-Ended LNA Design

The first topology chosen is a single-ended LNA. The circuit diagram is shown in Figure1. It employs inductive source degeneration (inductor connected to the source of transistor). This method has the advantage that one has a greater control over value of the real part of the input impedance through the choice of inductance [2]. Cascode transistor is used to minimize the tuned output interaction by tuning the input.

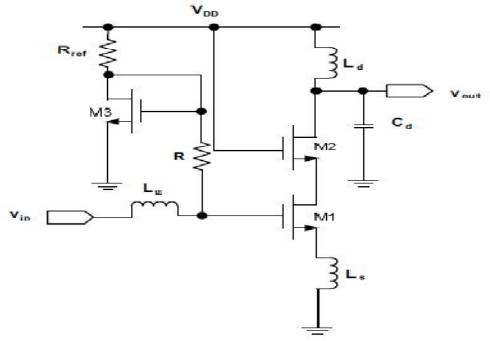

Figure 1: Single Ended LNA [2]

The RF input is coupled to the gate of the amplifier by the coupling capacitance. Transistor is the biasing transistor and forms a current mirror with transistor.

The width of is kept a small fraction of the width of to minimize the power overhead of the bias circuit. Output Inductor, resonates with output load to maximize output power transfer and gain at resonance frequency. The width of the cascoded transistor must be sized to trade-off common source gain reduction and increase of parasitic source capacitance of (both are consequences of a wider). Cascode transistor helps to reduce and reduceMiller effect. is large enough so that its equivalent current noise is small enough to be ignored. is used to set the resonant frequency.

III. SIMULATION OF SINGLE ENDED LNA

The schematic of fully single-ended LNA designed with 45nm technology is shown in Fig. 2. We have simulated our design using Cadence EDA tools-Virtuoso Schematic Editing and it is SimulatorSpectre.

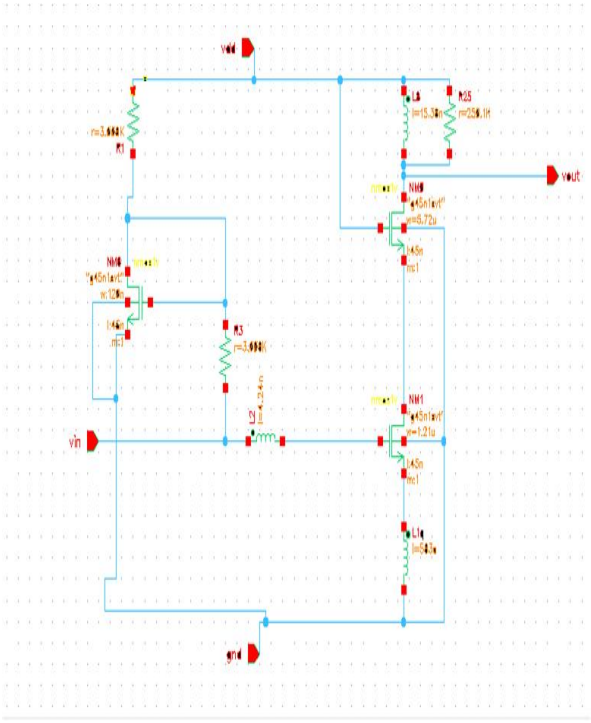

Figure 2: Schematic of Single-Ended LNA

A. Simulation results

Many simulation iterations are done on the proposed LNA circuit to meet design requirements. The simulation results of single-ended LNA achieved at the typical process are summarized in the Table 1.

Parameter	**Value**	**Unit**
Voltage Gain	10.09dB	dB
Input Port Voltage Reflection Coefficient,	-5.639	dB
Reverse Gain,	-37.13	dB
Forward Gain,	2.34	dB
Output Port Voltage Reflection Coefficient,	-0.623	dB
Stability Factor,	2.47	
Transducer Power Gain,	2.34	dB
Available Power Gain,	11.08	dB
Operated Power Gain	3.71	dB
Power dissipation	2.1	mW
	0.177	
Noise Figure	12.45	dB

Table 1: Performance parameters of the Single Ended LNA (RF frequency 76GHz)

B. Simulation Figures

After the simulation of the single-ended LNA at 76GHz frequency we obtained various results which are shown in the below figures.

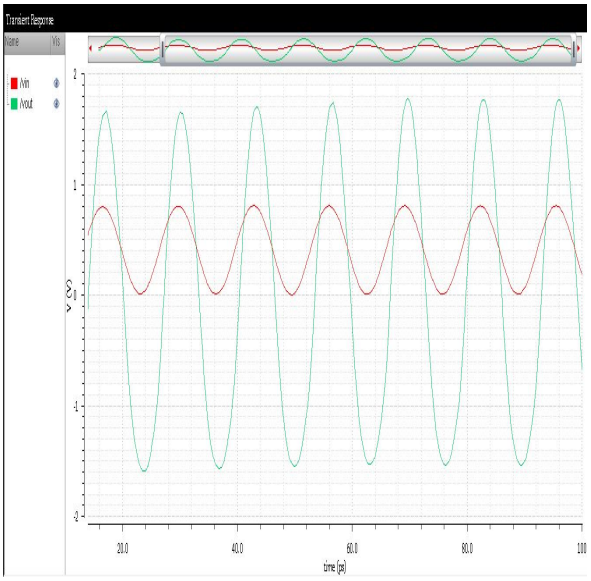

Figure 3: Transient Response of Single Ended Low Noise Amplifier

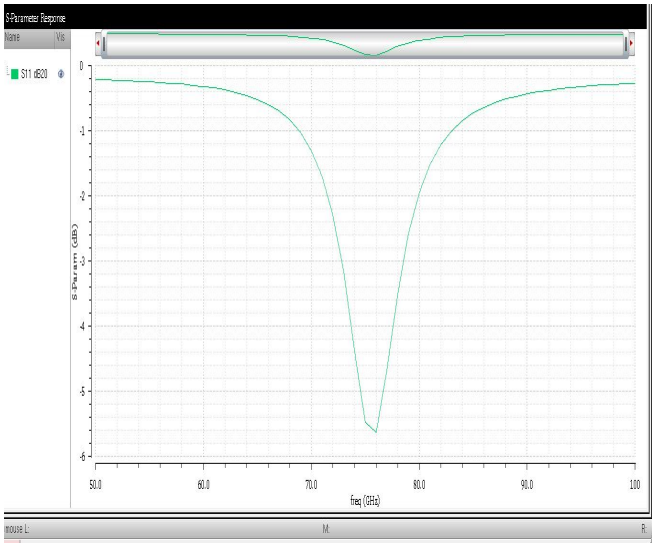

Figure 4(a): plot for single ended LNA

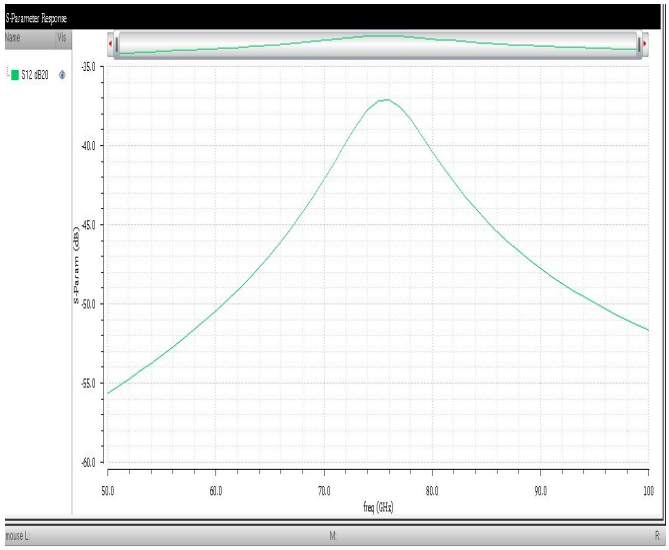

Figure 4(b): plot for single ended LNA

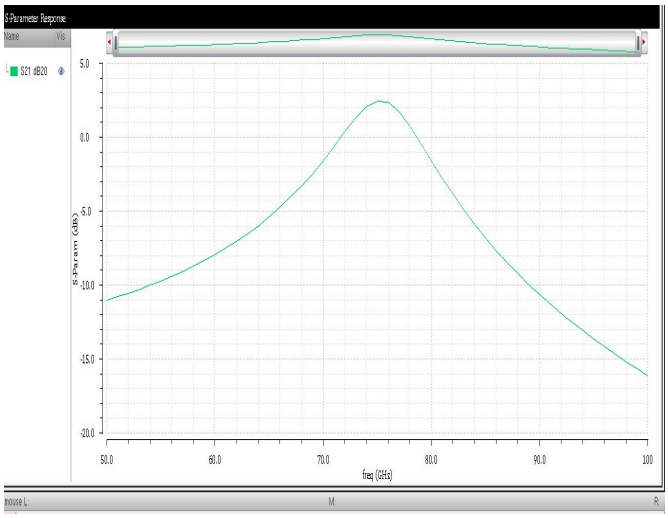

Figure4(c): plot for single ended LNA

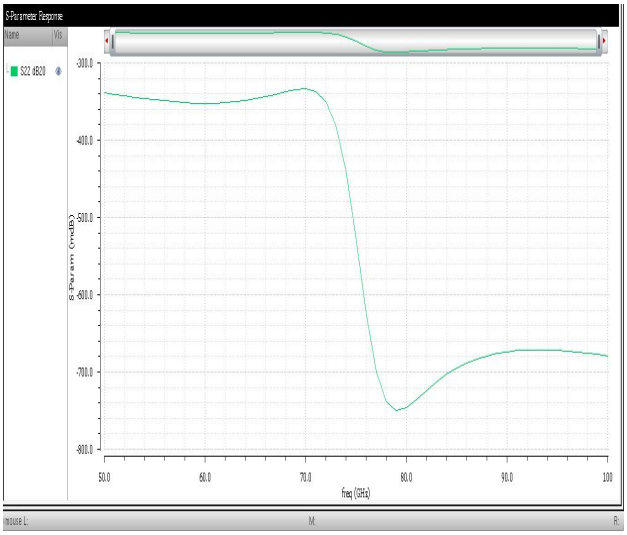

Figure 4(d): plot for single ended LNA

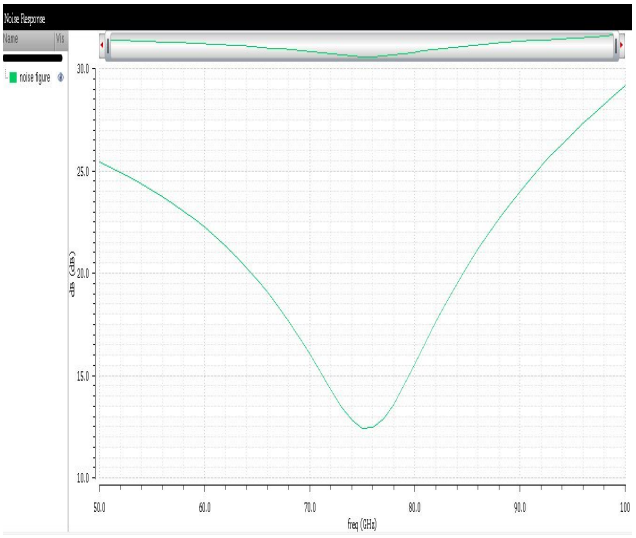

Figure 5: Noise figure plot for single ended LNA

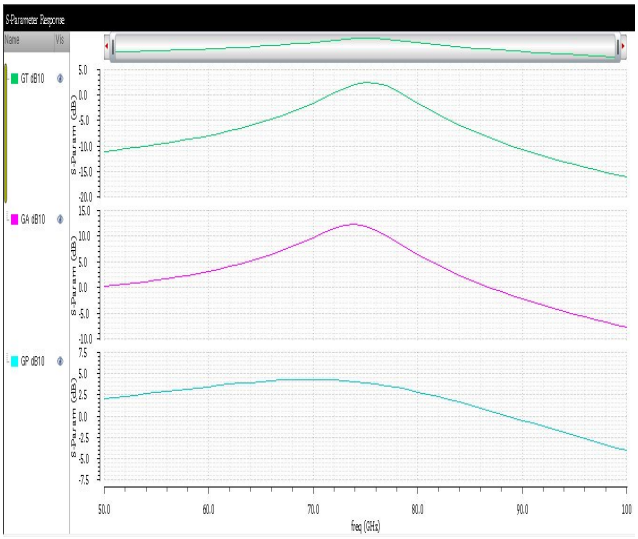

Figure 6: plot for single ended LNA

As is shown, Figure 3 and Figure 4(c) show the voltage gain and power gain at 76GHz frequency. The voltage gain is 10.09dB and power gain is 2.34dB obtained by simulation. Figure 5 gives us the Noise Figure parameter. The noise figure in our design is 12.45dB.

The input return loss value can be expressed in terms of the measured S parameter S11 is shown in Figure 6. The value of S11 obtained after the simulation is -5.639dB. Figure 6 shows the plots.At last, the power dissipation is calculated. After the simulation, so the power dissipation is 2.1mW.

IV. LNA DESIGN

A. Current Reuse LNA Design

CRLNA is mainly used for low power. The current reuse means to recycle the bias current so that it can be used by more than one stage. The basic issue with using a CMOS transistor for the LNA is its inherently low transconductance and hence low gain. However if the current reuse technique is employed, transconductance could be increased as much as two fold. The key point is that given the same bias current the effective transconductance is +, while it is simply in single ended topology [1].

With this approach, higher gain has been obtained without both, usage of the cascade configuration and increase in consumption as two amplifier stages have the same bias current (=). Since it is required for the LNA to have high gain and good circuit stability, cascode amplifier (and transistors) is the main contributor to the overall LNA gain. Besides high gain, the cascade amplifier provides high output impedance and good input to output isolation. As drain AC load of transistor in the cascode amplifier is approximately 1/ (input impedance of transistor, common gate CG amplifier), drain represents low impedance point. As transistor gate to drain gain is small, effect of Miller gate-drain overlap capacitance can be neglected. Additional amplifying stage (transistor) has common source topology in case capacitor, i =1, 2 is large. Resistor represents source output impedance (the most usual value is 50 Ω). For providing a good input matching the inductive source degeneration with inductor is used. Additional degree of freedom, while setting resonant frequency, is introduced with inductor. Bias circuit consists of transistor and resistor . The resistor is chosen large enough to represent high impedance to the carrier that prevents AC signal flow to the bias circuit, giving at the same time small contribution to the overall circuit noise. Voltage is transistor bias voltage. Large capacitor enables coupling of two amplifier stages by transmitting signal from transistor drain to transistor gate. Moreover, capacitor should have the highest possible value to provide the ideal AC ground for the second amplifier stage. Inductors, and represent loads of first and second amplifier stage. Capacitors and are input and outputblocking capacitors.

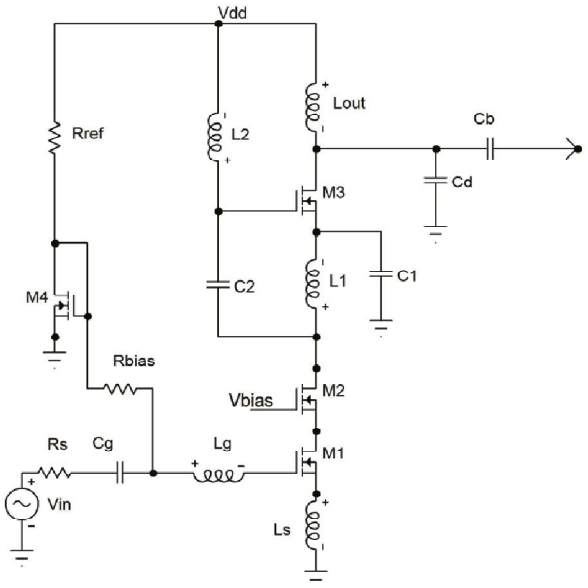

Figure 7: Current Reuse LNA [1]

V. SIMULATION

The schematic of current reuse LNA designed with 45nm technology is shown in Figure 8. We have simulated our design using Cadence EDA tools-Virtuoso Schematic Editing

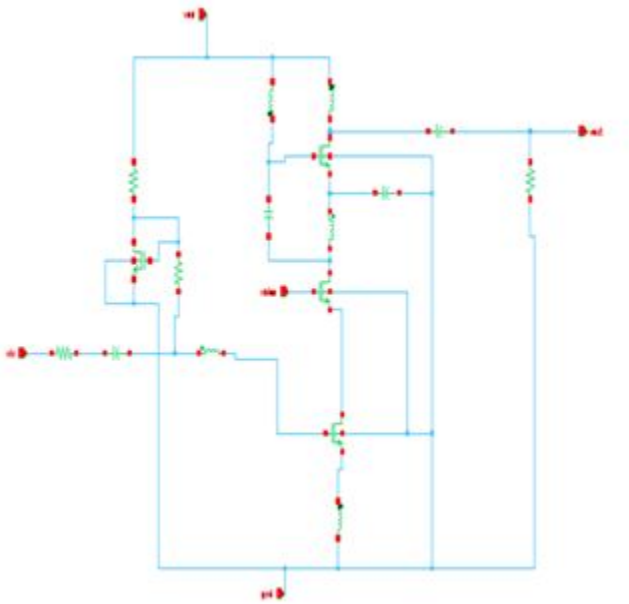

Figure 8: Schematic of current reuse LNA.

A. Simulation results

Many simulation iterations are done on the proposed LNA circuit to meet design requirements. The simulation

results of current reuse LNA achieved at the typical process are summarized in the Table 2.

Parameter	**Value**	**Unit**
Voltage Gain	11.79	dB
Input Port Voltage Reflection Coefficient,	-11.09	dB
Reverse Gain,	-26.731	dB
Forward Gain,	8.12	dB
Output Port Voltage Reflection Coefficient,	-0.408	dB
Stability Factor,	3.99	
Transducer Power Gain,	8.12	dB
Available Power Gain,	18.59	dB
Operated Power Gain	8.47	dB
Power dissipation	1.5	mW
	0.042	
Noise Figure	9.8	dB

Table 2: Performance parameters of the current-reuse LNA (RF frequency 76GHz)

B. Simulation Figures

After the simulation of the current reuse LNA at 76GHz frequency we obtained various results which are shown in the below figures.

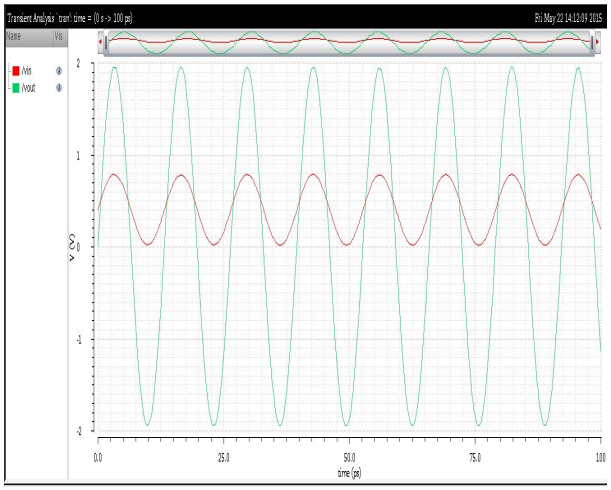

Figure 9: Transient Response of Current Reuse Low Noise Amplifier

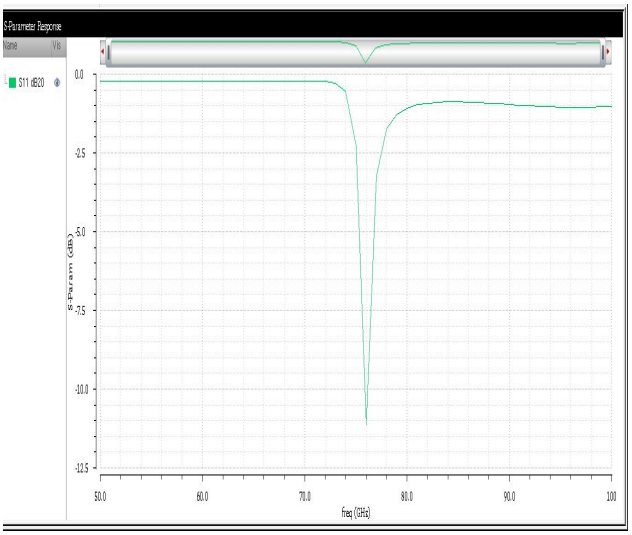

Figure 10(a): response of CRLNA

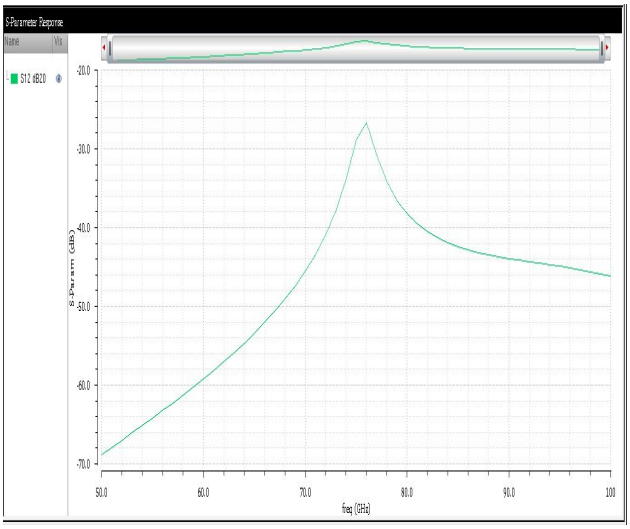

Figure 10(b): response ofCRLNA

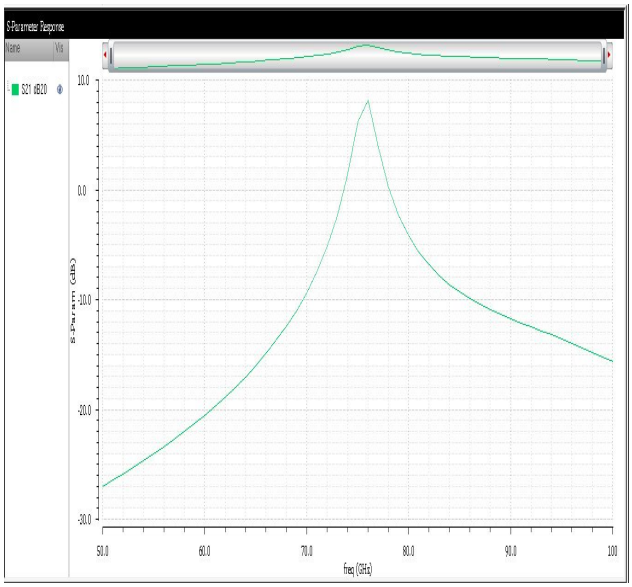

Figure 10(c): response of CRLNA

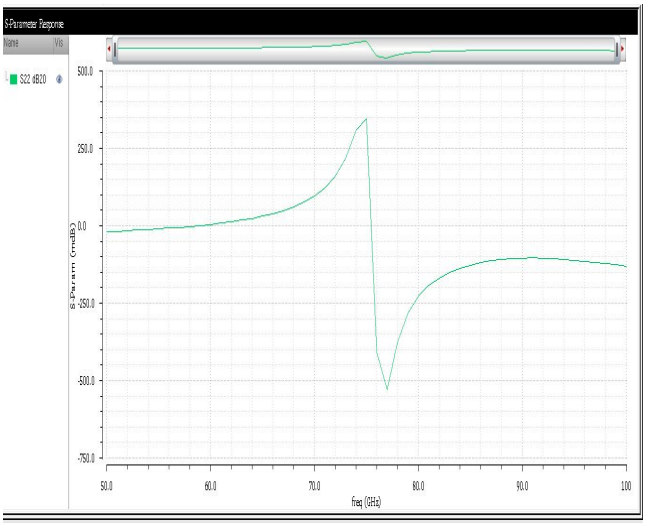

Figure 10(d): response of CRLNA

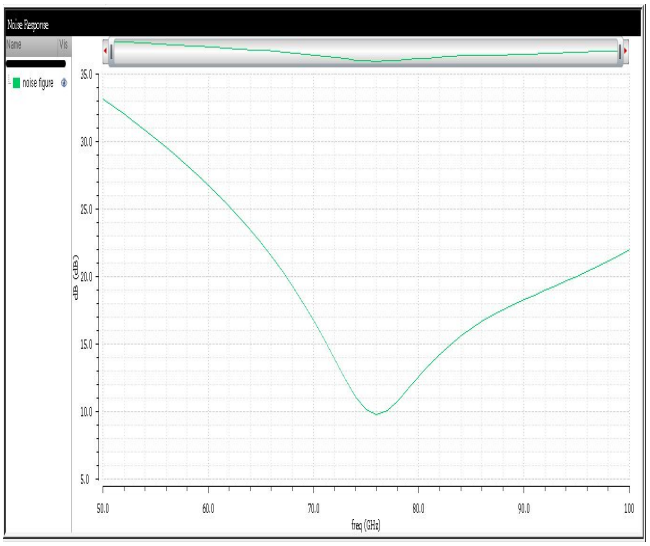

Figure 11: Noise Figure response of CRLNA

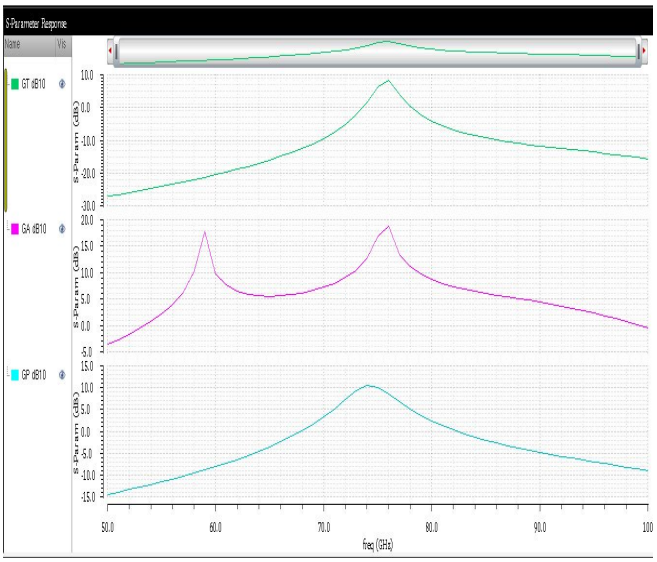

Figure 12: response of CRLNA

As is shown Figure 9 and Figure 10(c) show the voltage gain and power gain at 76GHz frequency. The voltage gain is 11.79dB and power gain is 8.12dB obtained by simulation. Figure 11 gives us the Noise Figure parameter. The noise figure in our design is 9.8dB.The input return loss value can be expressed in terms of the measured S parameter S11 is shown in Figure 10(a). The value of S11 obtained after the simulation is -11.09dB. At last, the power dissipation is calculated. So the power dissipation is 1.5mW.

VI. CONCLUSION

Several topologies of low noise amplifier have been investigated. Different parameters of two topologies of low noise amplifier i.e. single ended and current reuse are calculated and based on the information obtained the design is optimized. The transient and gain-phase response curves are also obtained of both the topologies of amplifier. deals with the designing of single ended amplifier and current reuse amplifier at high frequency of 76GHz and in 45nm CMOS technology, the comparison of designed topologies of amplifier are done in terms of performance parameters like power dissipation, gain, S parameter, stability and noise figure.

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