A novel Approach to Design of a low voltage, Low Drop-Out(LDO) 200mA Low Drop Out Regulator With Cascode Error Amplifier

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Abstract- *In this paper a low voltage, low drop-out (LDO) voltage regulator design procedure is proposed and implemented using TSMC0.18micron BiSIM V3.1CMOS process. It discusses a 1 to 1.5V, 5mA CMOS low drop-out linear voltage regulator with a single compensation capacitor of 1pF. The experimental results show that the maximum output load current is 0.64mA and minimum regulated output voltage is 1.11690µV.The regulator provides a full load transient response with less than 5mV overshoots and undershoots.*

Keywords:- low drop-out, low-voltage regulators, CMOS, linear regulator, power supply circuits, regulators. load regulation ,line regulation, PSSR. Phase Margin

I. INTRODUCTION

A Low-drop-out (LDO) regulator is a DC linear voltage regulator which can operate with a very small input-output differential voltage. The demand for the low-voltage, low drop out (LDO) regulators is increasing very rapidly because of the growing demand of portable electronics, i.e., smart watch, mobile phones, pagers, laptops, etc as well as industrial and automotive application [1]. Most recently this increasing demand for portable and battery operated products have forced these circuits to operate under low voltage conditions.

Furthermore high current efficiency has also become necessary to maximize the lifetime of battery.LDO design has become more challenging due to the increasing demand of high performance LDO's,of which low-voltage fast-transient LDO's are especially important [1]. Methods to improve the classical LDO structure have been proposed. However, structural limitation, which is the main obstacle in simultaneously achieving stability, high output-voltage accuracy and short response time, still cannot be overcome [2]. The structural limitation of the classical LDO's is mainly due to the associated single pole-zero cancellation schemes, in which an off-chip capacitor with a high equivalent series resistance (ESR) is required to achieve low-frequency pole-zero cancellation.

Therefore, to achieve good specifications, a novel LDO with a very simple circuit structure is employed. The structure has a double pole-zero cancellation scheme, and the design provides good performance but there is a trade off in settling time.

II. LOW – DROP OUT REGULATO STRUCTURE AND SCHEMATIC DESIGN

The Structure of the proposed LDO is shown in figure 1. It is composed of two stages. The 1st stage, as in the classical LDO, is the error amplifier use to provide error signal for voltage regulation. And the second stage is a common source amplifier which has a high output swing. Due to cascade architecture, the loop gain depends on the products of the voltage gains of the two gain stages. The high loop gain provides good line and load regulations [1].

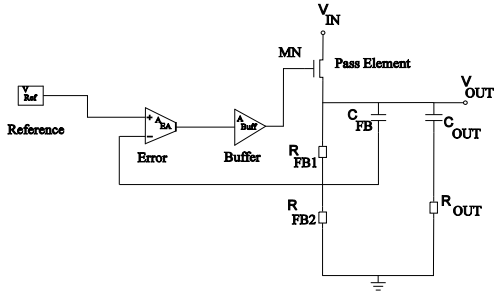


Fig. 1: circuit diagram of proposed LDO regulator

The circuit schematic in figure 2 shows that the error amplifier is a differential pair (M2 & M3) with active load (M4 & M5), while the second gain stage is a common source stage (M6) with a bias – current source (M7). The output swing of the second stage is much better than the source follower in turning on or off the power transistor, and therefore this configuration is suitable for low-voltage LDO designs. The current mirrors (M1, M7 & M8) provide current bias for both the stages.

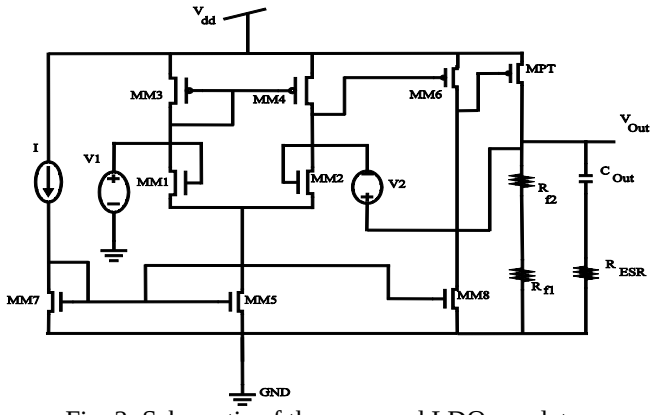


Fig. 2: Schematic of the proposed LDO regulator

The power transistor (MPT) is designed to operate in saturation region at drop out. Although the voltage gain of the power transistor is less than unity, the loop gain is not degraded due to the error amplifier and the second gain stage. A loop gain of more than 83dB can be easily achieved in the proposed design and is sufficient for good line and load regulations [1]. In the proposed design for the good transient response performance reason, the transistor size reaches millimeter or even centimeter orders, which generates a bigger gate capacitors. The slew rate at the gate of the power transistor and the frequency response of the LDO disadvantages for the proposed LDO.

Design of LDO can be subdivided into the design of power transistor (MPT) and design of two stage op-amp.

3.1. Design of error amplifier

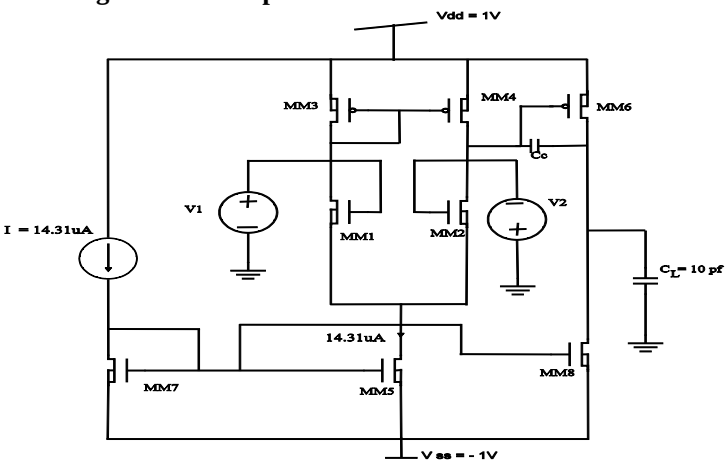


Fig. 3: Schematic of the error amplifier

In this section, a procedure is developed that will enable a first-cut design of the two-stage op-amp. The hand calculation approaches 70% of the design process. The two stage op-amp is designed for the following specs.

III. DESIGN OF LDO REGULATOR

Table 1: Modeling of proposed error op-amp

Sn	Parameter	Unit	Main Results
01	Compensation capacitor (Cc)	pF	2.9 ≈ 3 pF
02	Load capacitor (C_L)	pF	10 pF
03	Total Drain Current(I_{DD})	µA	14.31×10^{-6}A
04	Tail current (I_5)	µA	14.31µA
05	W/L ratio of first andsecondCMOS	µs	2.9 ≈ 3 µs
06	W/L ratio of first andsecondCMOS	µs	2.058 µs
07	Tranconductance (g_m)for MM1and MM2CMOS	µs	1.8455 µs
08	Saturationvoltage(Dra into source voltage)for MM1 CMOS	mV	888.9×10^{-3}mV
09	Saturation voltage (Drain to source voltage) for MM5CMOStransistor(VDS5)	mV	4.89mV≈5mV
10	Gain Bandwidth (GB)	Mhz	6Mhz
11	Minimum output voltage(Vminout)	µV	1.11690µV

Table : 2 Aspect Ratios of the Transistors (W/L)µm for the Two Stage Compensated Op-Amp.

Transistor	Aspect Ratios (W/L)µm
MM1	1/0.18µm = 5.55
MM2	1/0.18µm = 5.55
MM3	1.8/0.18 µm = 10
MM4	1.8/0.18 µm = 10
MM5	3.5/0.18 µm= 19.44
MM6	6/0.18 µm= 27.44
MM7	3.5/0.18µm= 19.44
MM8	4.5/0.18 µm=25

Which is less than required. At this point, the first-cut design is complete

3.1.3 Design of MPT stage Below are the design steps for of power transistor stage

Table 3: Design specification of power transistor

parameter	symbol	Quantity
Length	MPTL	180nm
Width	MPTW	5µm
Voltage reference	Vref	1 v
Output capacitance	Cout	20µf
Bias resistance	Rf1	50kΩ
Bias resistance	Rf2	100kΩ
Bias capacitance	Cf2	1pf

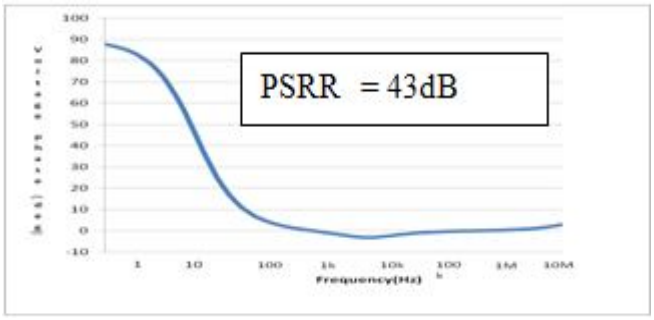
The output accuracy of the proposed LDO is high with regard to the effect of the offset voltage since there are only two pair of devices that require good matching(M2-M3 and M4-M5). The offset voltage due to large variations at the error amplifier Output, occurring in the classical LDOs, is reduced in the proposed LDO due to the gain stage formed by M6 and M7. Due to the simple circuit structure, the output noise of the proposed LDO is low. Moreover, there is no embedded capacitor or resistor to create poles and zeros for stability purpose, and therefore no coupling noise is imposed on the Error amplifier. Moreover, the output noise from the error amplifier can be minimised by large gm2 and gm3

IV. IMPLEMENTED RESULTS

The proposed LDO is designed using TSMS0.18µm CMOS technology. The LDO is capable of operating from 1V to 1.5 V, which covers a wide range of the typical battery voltage. A dropout voltage of 170mV at a 5uA maximum load current is achieved.The transient response is 1.01µs. power supply rejection is 0.64mV when operating at 1V.

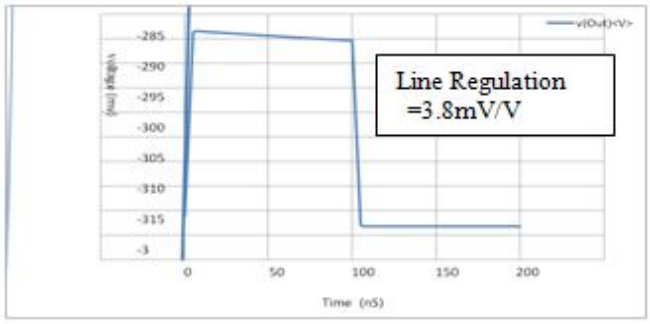
4.1 PSSR (Power Supply Rejection Ratio):

PSRR of proposed LDO 43Db



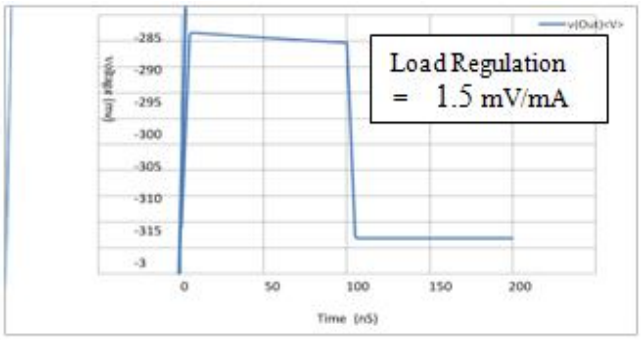
4.2 Line Regulation:

Line Regulation of proposed LDO is 1.8 mv.



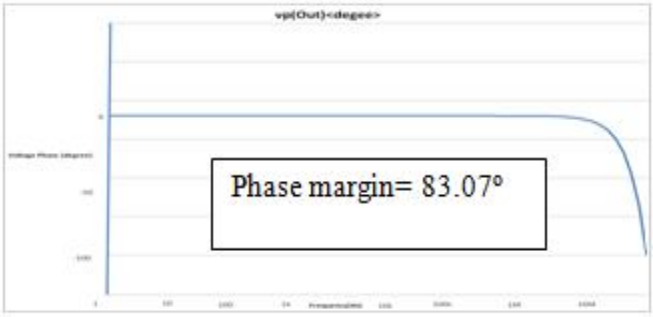
4.3 Load Regulation:

Load Regulation of proposed LDO 1.5mv/v



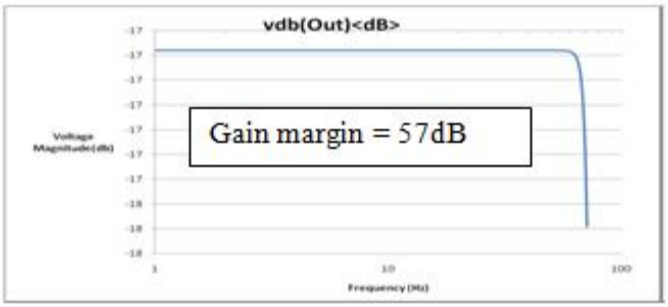
4.4 Phase Margin:

Phase Margin of proposed LDO 83.07º. which makes of stability of UHF range.



4.5 Gain Margin:

Gain margin of proposed LDO is 57dB.



4.6 Dropout:

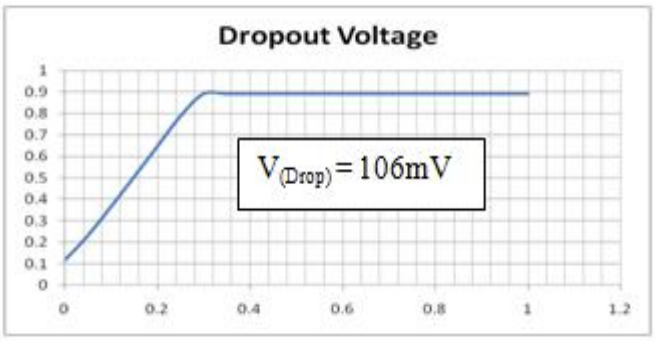


Table 4 : Implemented Results Summery

Technology	0.18 µCMOS	
Supply voltage	1v to 1.5v	
Quiescent current	0.0498µA	
Dropout voltage	106mV	
Load Current	5µA	
Line Regulation	3.8mv/v	5 µA
	2.087mv/v	10µA
	1.525mv/v	150 µA
Load regulation	1.5 mV/mA	
Full Load	60µV/mA	
Transient Response	40µs	
Phase margin	83 Degree	
PSSR	43dB	
Efficiency	90.01 % at 1v	

V. CONCLUSION

A low drop out regulation with a compensation capacitor has been proposed. The design is based on a simple but advanced structure ad proposes a double pole-zero cancellation schemes. It meets most of the typical specifications of a commercial LDO. Experimental results show that proposed LDO has small overshoots and undershoots while having excellent line and load regulations. The designed LDO is suitable for powering up low-voltage CMOS mixed-signal systems.

COMPARISON OF THE PROPOSED CAPACITOR-LESS LDO TOPOLOGY AGAINST THE STATE OF THE ART

	1998	2000	2003	2004	2005	2007	2012	2014	This work
Technology(µm)	2.0	1.0	0.6	0.5	0.09	0.35µm	0.25µm	0.18µm	0.18µm
Supply Voltage	3.8V	2.5V	1.3V	1.8V	1.5	1V	3v to 5v	1.8 V	1v to 1.5v
Dropout Voltage (V)	0.3	N.A.	0.2	N.A	0.3	0.2V	200mV	200 mV	106mV
Output Current (mA)	50	200	100	160	100	200mA	50mA	50 mA	5µA
Quiescent Current (mA)	0.023	.03	.038	.025	6	0.02mA	129µA	80 µA	0.0498µA
ΔVout mV	19 mV	220 mV	130 mV	200 mV	90mV	54mV	2.8V	100 mA	106mV
Line Regulation	4mV/3.8V	2mV/V	0.38µV/1.3V	2mV/V	0.54mV/V	2mV/V	1.85mV/V	2.6 V/V	3.8mv/v at 5 µA 2.087mv/v at 10µA 1.525mv/v at 150 µA
Load Regulation	19mV/50mA	0.275mV/mA	-200mV/100mA	10mV/20mA	0.2mV/100mA	170µV/mA	56µV/mA	13 mV/mA	1.5µV/mA
Full Load Transient Response	N.A	40 µs	38µs	44.51µs	0.54ns	40 µs	44.34 µs	58.07 µs	40µs
Phase Margin	N.A	N.A	60dB	>60dB	N.A	N.A	64.130	<50dB	83 Degree
PSRR	N.A	N.A	-65.38dB	-57dB	N.A	>-45dB	-68.35dB	-56dB	-43dB
Current Efficiency(%)	99.5	N.A	N.A	N.A	94.3%	99.8%	93.09% at 3v 55.85% at 5v	98.5%	99%
Output Capacitor	N.A	N.A	N.A	N.A	N.A	1µf	10pf		1pf
FOM(nS)	8.2ns	0.165ns	4.9ns	0.43ns	0.023ns	0.027ns	N.A	N.A	0.024 ns

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