Efficient and high speed vlsi modelling of fm0/manchester encoding using sols technique and clock gating technique for dedicated short range communication applications

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Abstract - *To promote intelligent and smart transportation services into our daily life the dedicated short range communication is an advanced technique. Data encoding techniques like FM0 and Manchester encoders are used to promote communication among vehicles. Manchester coding technique is a digital coding technique in which all the bits of the binary data are arranged in a particular sequence. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity. This integrated circuit is fully guaranteed to support the 1MHz data rate of MlL-STD-1553over both temperature and voltage. The circuit obtained is an integrated architecture of FM0, Manchester and Miller encoding to overcoming various drawbacks of traditional method. This deduced architecture of FM0 and Manchester coding would well support the DSRC standards. The performance of this paper is evaluated on Xilinx FPGA Spartan-3E kit. It interfaces with CMOS, TTL or N channel support circuitry. These encoding techniques generally works at transistor level hence the transmitted signal reach with dc-balance, enhance the signal reliability. In existing works the design has the limitation that it does not support fully reused VLSI architectures. To rectify these problems, the FM0 and Manchester encoders are designed with SOLS technique to achieve high speed and fully reused VLSI architectures for DSRC application systems. The performance of this paper is implemented on post layout simulation in 45nm CMOS technology. This model not only supports fully reused architecture but also provides high performance.*

Index Terms - *Dedicated Short Range Communication (DSRC), FM0, Manchester, Miller, Encoder, Decoder, Similarity Orientation Logic Simplification (SOLS).*

I. INTRODUCTION

The Dedicated Short-Range Communication (DSRC) is an emerging standard to push the intelligent communication into modern automotive industry. Several organizations in different countries start to develop the DSRC standards for electric-vehicular applications accidents and improve traffic flow. The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc-balance.

The DSRC standards generally adopt Manchester codes to make the transmitted achieving DC-balance that plays an important role in signal reliability. However, the coding-diversity Manchester makes their VLSI architecture with hardware utilization.

The fully reused VLSI architecture using the similarity oriented logic simplification (SOLS) technique for both FM0 and Manchester encodings is proposed in this project. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area – compact retiming and balance logic-operation sharing. The SOL technique improves the hardware utilization rate for both FM0 and Manchester encodings.

The system architecture of DSRC transceiver is shown in Fig1. Consists of three primary modules namely microprocessor, base band processing and RF front-end.

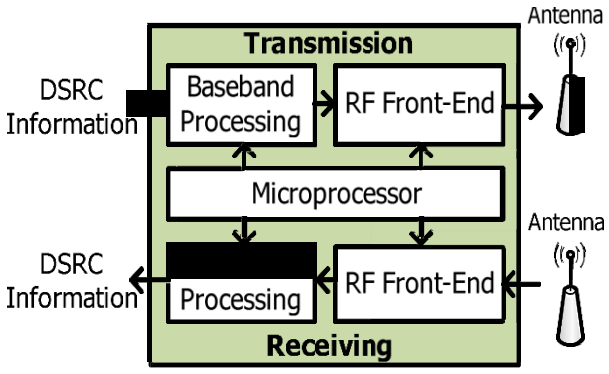

Fig1. DSRC transceiver

II. RELATED WORK

The literature [4] targets a VLSI architecture of Manchester encoder for optical communications, implemented by 0.35-µm CMOS technology and its operation frequency is 1 GHz. The literature [5] further replaces the architecture of switch in [4] by the nMOS device. It is realized in 90-nm,CMOS technology, and the maximum operation frequency is as high as 5 GHz. The literature [6] develops a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for RFID applications. This design is realized in 0.35-µm CMOS technology and the maximum operation frequency is 200 MHz. The literature [7] also proposes a Manchester encoding architecture for ultra high frequency (UHF) RFID tag emulator, realized into FPGA prototyping system, maximum operation frequency of this design is about 256 MHz. The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator [8]. Its maximum operation frequency is about 192 MHz. Furthermore, [9] combines frequency shift keying (FSK) modulation and demodulation with Manchester code in hardware implementation.

III. CODING PRINCIPLES OF FM0 CODE AND MANCHESTER CODE

In the following discussion ,the clocks ignaland the input data are abbreviated as CLK , and *X* , respectively .With the above parameters , the coding principles of FM0 and Manchestercodes are discussed as follows.

A. FM0 ENCODING

Foreach*X*,theFM0codeconsistsoftwoparts:oneforformer-halfcycleofCLK,*A*,andtheotheroneforlater-halfcycleofCLK,*B*.ThecodingprincipleofFM0islistedasthefollowingthreerules.

1) If *X* is the logic-0, the FM0 code must exhibita transition between *A* and *B*.
2) If *X*isthelogic-1,notransitionisallowedbetween*A*and*B*.
3) Thetransitionisallocatedamongeach FM0codenomatter whatthe*X*is.

AFM0codingexampleisshowninFig.2.Atcycle1,the*X*islogic-0;therefore,atransitionoccursonitsFM0code,accordingtorule1.Forsimplicity,thistransitionisinitiallysetfromlogic-0to-1.Accordingtorule3,atransitionisallocatedamongeach FM0 code, and thereby the logic-1 is changed tologic-0 in the beginning of cycle 2. Then, according to rule 2, this logic-level is hold without any transition inentire cycle 2 for the X of logic-1. Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

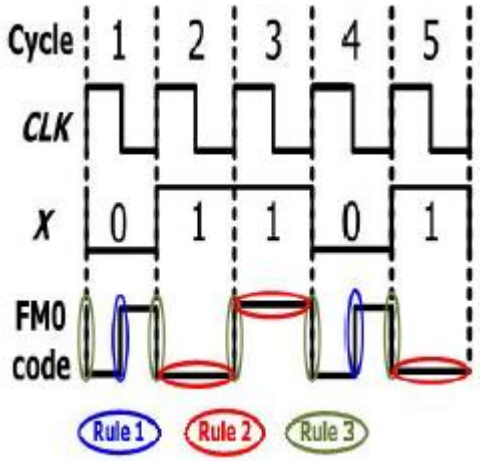

Fig 2. Illustration of FM0 coding Example

B. MANCHESTER ENCODING

The Manchester encoding is realized with a XOR operation for CLK and X. The clock always has a transition within one cycle, and so does the Manchester code no matter what the X is. The Manchester coding example is shown in Fig. 3.

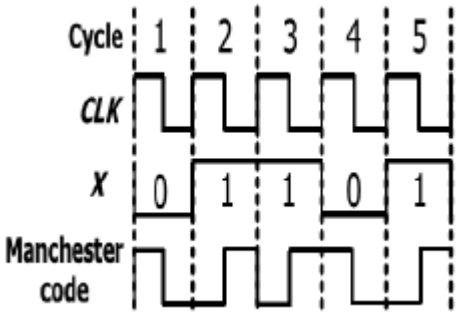

Fig 3. Illustration of Manchester Coding Example

IV DESIGN OF FM0 &MANCHESTER CODE

The need for SOLS technique is to design a fully reused VLSI architecture for FM0 and Manchester codes. SOLS technique is having two core concepts: area-compact retiming and balance logic operation sharing .The VLSI architecture of FM0 and Manchester code is shown in figure 4.

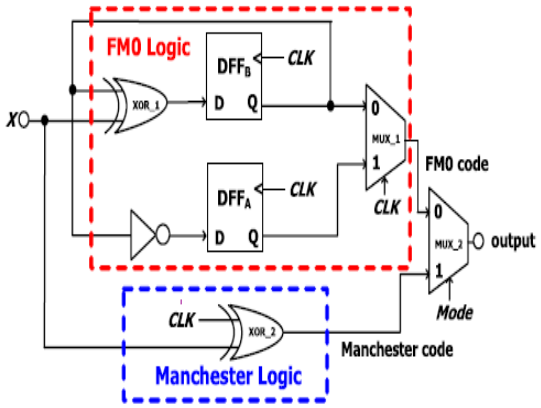

Fig 4. VLSI architecture of FM0 and Manchester

The SOLS technique improves the HUR from 57.14% to 100%, whether the FM0 or Manchester code is adopted. Thus, the SOLS technique provides a fully reused VLSI architecture for FM0 and Manchester encodings with the HUR of 100%. The logic functions of SOLS technique can be realized by various logic functions to optimize more performance such as area, power, speed. The proposed SOLS technique is developed from the architecture perspective to achieve 100% HUR. If the logic components in SOLS architecture are designed using static CMOS, the Manchester delay is seriously limited owing to too many transistors in the critical path of Manchester encoder. To further reduce the transistor count in Manchester encoding path, the transmission-gate logic is considered in the circuit designs of MUX−1, MUX−2 and XNOR. The propagation delay of transmission-gate logic is less than that of static CMOS. Applying the transmission gate logic can compact the transistor count to reduce the propagation delay.

V CONCLUSION

In this paper, the completely reused VLSI structural engineering utilizing SOLS strategy for both FM0 and Manchester encodings will be proposed.. This paper is acknowledged in 45nm CMOS innovation with extraordinary gadget proficiency and implemented by using Microwind3.1 for post layout synthesis. The timing analysis are verified on Xilinx simulator. The Xilinx9.2i software is utilized in the project and code is written on Verilog HDL. The target FPGA prototyping device is belongs to Spartan3E family and the device is XC3S100E which has speed grade of -5. The power consumption is 1.48mW and the delay is 5.776ns. The SOLS technique gives high performance when compared to existing articles. In future the design may implemented using high performance FPGA devices and the Nanometer may be reduced from 45nm to 32 nm CMOS technology.

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