Simulation of Continuous Current Source Drivers for 1MH Boost PFC Converters

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Abstract- *In this paper, an adaptive full-bridge CSD is proposed for the boost PFC converters. The proposed CSD can build adaptive drive current inherently depending on the drain current of the main power MOSFET. Current source drivers (CSDs) have been proposed to reduce the switching loss and gate drive loss in megahertz (MHz) dc–dc converters, in which the duty cycle normally has a steady-state value. The duty cycle of the power factor correction (PFC) converters is modulated fast and has a wide operation range during a half-line period in ac–dc applications. The adaptive CSD is able to realize better design tradeoff between the switching losses and drive circuit loss so that the efficiency can be optimized in a wide operation range. The experimental results verified the functionality and advantages. For that simulation results are verified on MATLAB/simulink software. The performance characteristics are described in simulation results.*

Keywords- Power Factor Correction (PFC), MOSFET, current source driver (CSD), Boost converter.

I. INTRODUCTION

The idea of the CSD circuit is to build a current source (CS) to charge and discharge the power MOSFET gate capacitance so that fast switching speed and reduced switching loss can be achieved. Owing to the CS inductor, the energy stored in the gate capacitance of the MOSFETs can be also recovered, similarly to the RGDs. Depending on the current types of the CS inductor, the CSD topologies can be categorized as continuous and discontinuous [1]. On the other hand, most of present work related to the CSDs is to investigate their applications in dc– dc converters, where the duty cycle normally has a steady-state value. In ac–dc applications, the power factor correction (PFC) technique is widely used. Different from dc–dc converters, the duty cycle of the

PFC converters needs to be modulated fast and has a wide operation. In ac–dc applications, the power factor correction (PFC) technique is widely used. Different from dc–dc converters, the duty cycle of the PFC converters needs to be modulated fast and has a wide operation range. Normally, the switching loss is proportional to the switching current and the drain-to- source voltage. For a boost PFC converter, the input line current follows the input line voltage in the same phase. When the line voltage reaches the peak value of the power MOSFET, the line current also reaches the peak and so does the drain current (i.e., the switching current). This means that the switching loss reaches its maximum value at this moment.

The objective of this paper is to present a new CSD with the capability to build an adaptive drive current inherently depending on the switching current of the power MOSFET for a boost PFC converter. When the input voltage and current reach the peak value and the switching loss is high, the proposed CSD can provide a stronger drive current to reduce the switching loss further [2]. On the other hand, when the input voltage and current are low, and as a result the switching loss is also low, the proposed CSD provides lower drive current to minimize the drive circuit loss. In this way, the proposed adaptive CSD improves the efficiency in a wide operation range for a boost PFC converter compared to other proposed CSDs previously.

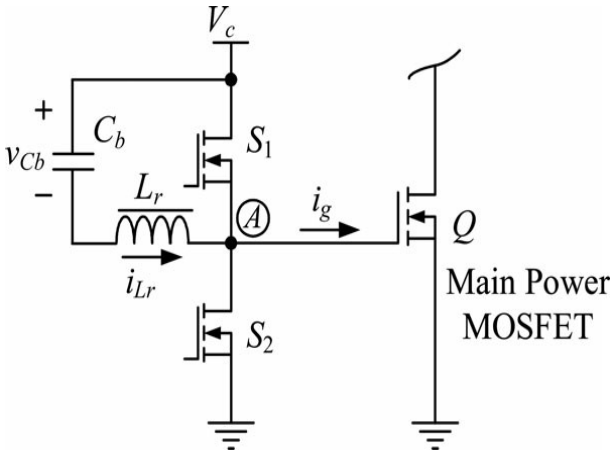


Fig.1. Current source drive topology

II. PROPOSED CSD DESIGN AND OPERATION

Proposed CSD for a Boost PFC Converter

Fig. 2 shows the proposed CSD circuit for the boost PFC converter. Compared to Fig. 1, *S*2 and *S*4 are used to remove the blocking capacitor *Cb* , which forms a FB CSD structure. Since there is no longer any blocking capacitor *Cb*

, the proposed CSD can be suitable for the boost PFC converters with the modulated duty cycle [3].

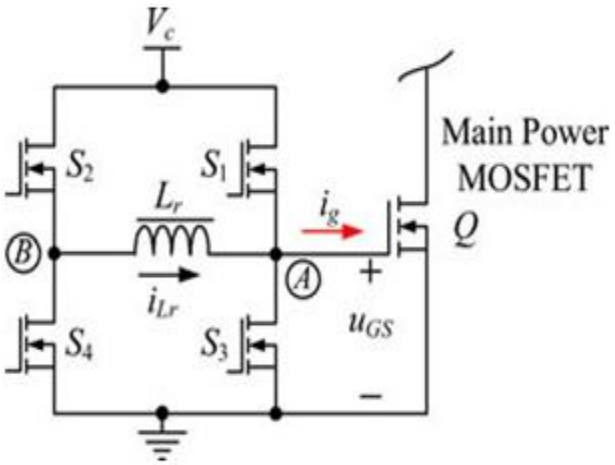


Fig 2. Proposed CSD Solution for PFC applications.

Operation principle

There are eight switching modes in one switching period [4]. The operation of principle is presented as follows. Fir the explanation of principle of operation of proposed CSD drive, from fig.2, for every switching device there is in- parallel diode and capacitor to be assumed.

Mode 1 [t_0, t_1]: Prior to t_0, $S3$ is ON and the gate of Q is clamped to ground. At t_0, S_3 turns OFF and the peak value Ipeak of the inductor current i_{Lr} charges C_3 plus Cgs and discharges C_1 simultaneously as a CS. Due to C_1 and C_3, S_3 achieves zero-voltage turnoff. The voltage of C_3 rises linearly and the voltage of C_1 decays linearly.

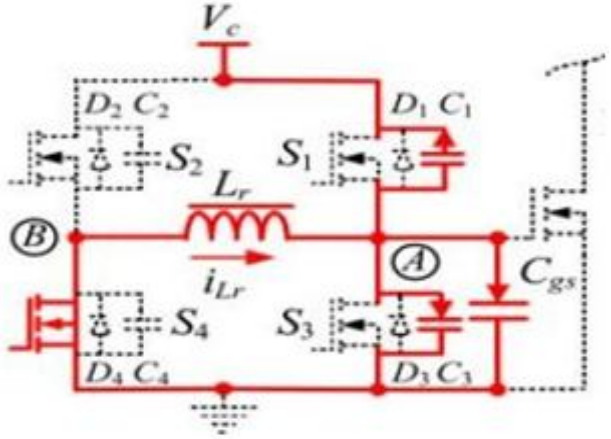


Fig. 3 (a) mode 1 (t_0, t_1)

Mode 2 [t_1, t_2]: At t_1, the body diode $D1$ conducts and $S1$ turns ON with the zero-voltage condition. The gate-to-source voltage of Q is clamped to Vc through $S1$. During this interval, iLr decreases and changes its polarity from I_{peak} to $-I_{peak}$.

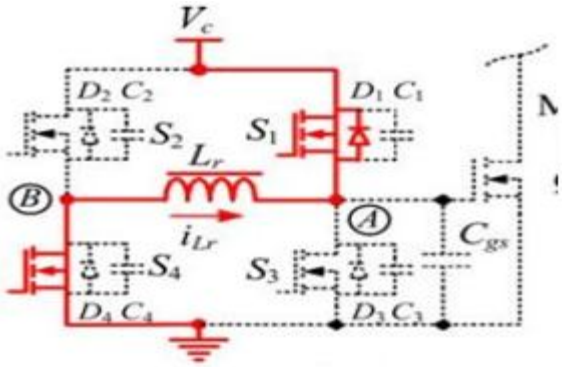


Fig. 3 (b): mode 2 (t_1, t_2)

Mode 3 [t_2, t_3]: At t_2, S_1 turns OFF and the negative peak value $-I_{peak}$ charges $C1$ and discharges $C3$ plus Cgs simultaneously as a CS. Due to $C1$ and $C3$, $S1$ achieves zero-voltage turnoff. The voltage of $C1$ rises and the voltage of $C3$ decreases linearly.

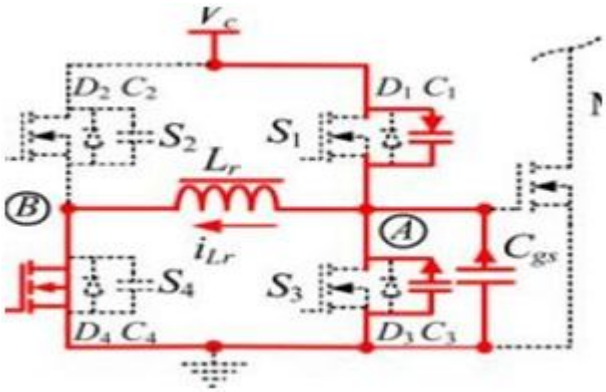


Fig.3(c): mode (t_2, t_3)

Mode 4 [t_3, t_4]: At t_3, $D3$ conducts and $S3$ turns ON with the zero-voltage condition. The gate to- source voltage of Q is clamped to ground through $S3$. The current path during this interval is $S3$–Lr –$S4$. iLr circulates through $S3$ and $S4$ and remains constant in this interval.

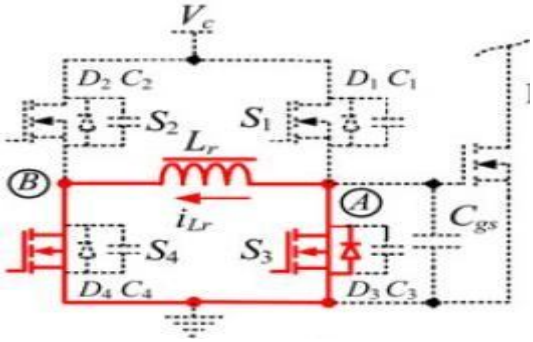


Fig.3 (d): mode 4 (t_3, t_4)

Mode 5 [t4, t5] [see Fig. 6(e)]: At t4, S4 turns OFF and the negative peak current -Ipeak chargesC4 and discharges C2

simultaneously. Due to C2 and C4, S4 achieves zerovoltage turnoff. The voltage of C4 rises linearly and the voltage of C2 decays linearly.

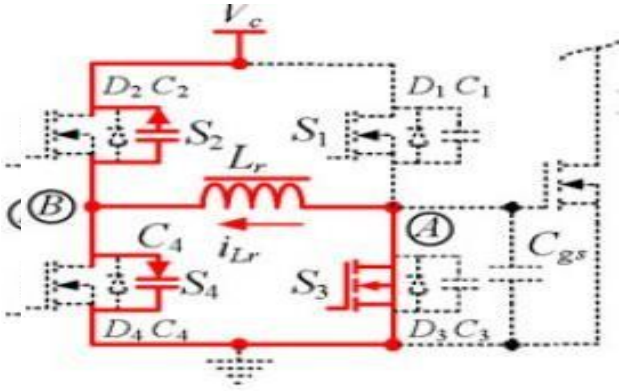


Fig.3 (e): mode 5 (t_4, t_5)

Mode 6 [t_5, t_6]: At t_5, D2 conducts and S2 turns ON with the zero-voltage condition. iLr decreases from- I_{peak} and changes its polarity to I_{peak}.

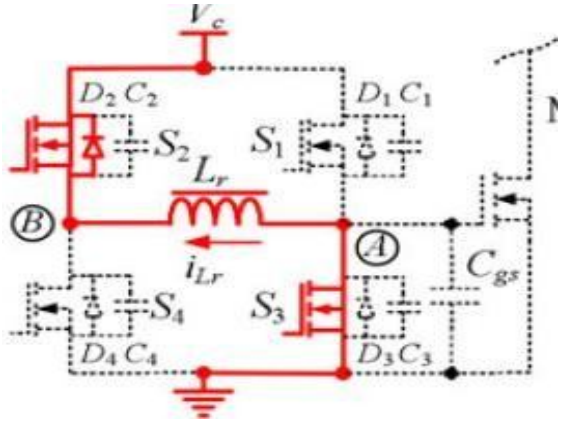


Fig.3 (f): mode 6 (t_5, t_6)

Mode 7 [t_6, t_7]: At t_6, S2 turns OFF. The peak drive current Ipeak charges C2 and discharges C4 . The voltage of C2 rises linearly and the voltage of C4 decays linearly.

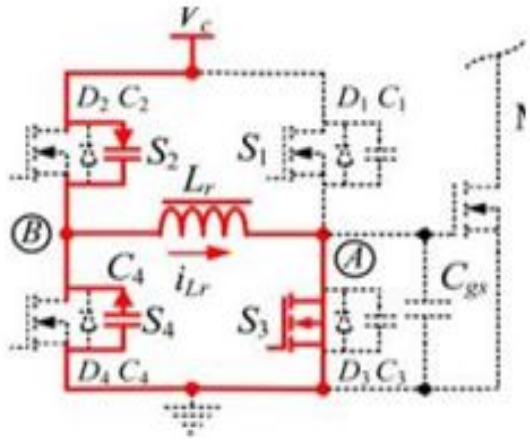


Fig.3 (g): mode 7 (t_6, t_7)

Mode 8 [t7, t8] [see Fig. 6(h)]: At t7,D4 conducts and S4 turnsONwith the zero-voltage condition. The current path during this interval is S4– Lr –S3 . iLr circulates through S3 and S4 and remains constant during this interval.

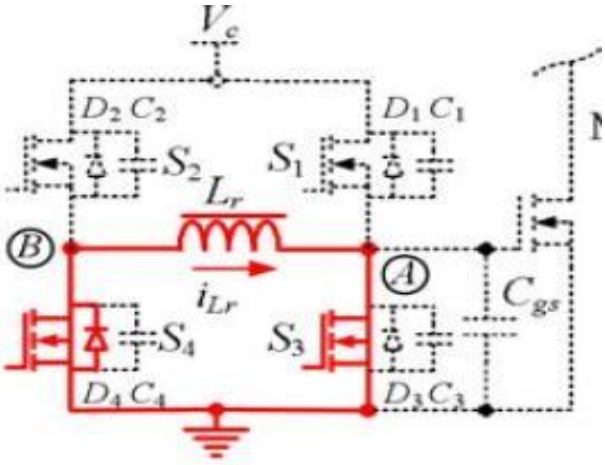


Fig.3 (h): mode 8 (t_7, t_8)

Proposed Adaptive Current Source Drive

The basic idea is to find the optimal solution on the basis of the object function that adds the switching loss and the CSD circuit loss together. The object function should be a U-shape curve as a function of the drive current Ig. The optimal design method proposed is for the dc–dc application with the steady-state duty cycle and the constant drive current [5]. However, for the boost PFC converter, the duty cycle modulates during the line period and the drive current is also adjusted to the switching current. Therefore, for the boost PFC converter, the optimal design current uses the maximum CS inductor current Ig max as the design variable.

It is noted that the optimal gate drive current is 2.4 A. Based on the selected gate drive current, the calculated CS inductor is

$$L_r = \frac{V_c V_{in\max}}{2 f_s V_o I_{g\max}} = 1\,\mu\text{H}$$

Where Vin = 110 V, fs = 1 MHz, Vo = 380 V, Po = 300 W, and Igmax = 2.4 A. As far as the common source inductance is concerned, the current diversion problem of the CSD results in the reduction of the effective drive current. Therefore, in the experimental prototype, the designed current is chosen as 2 A to optimize the overall efficiency.

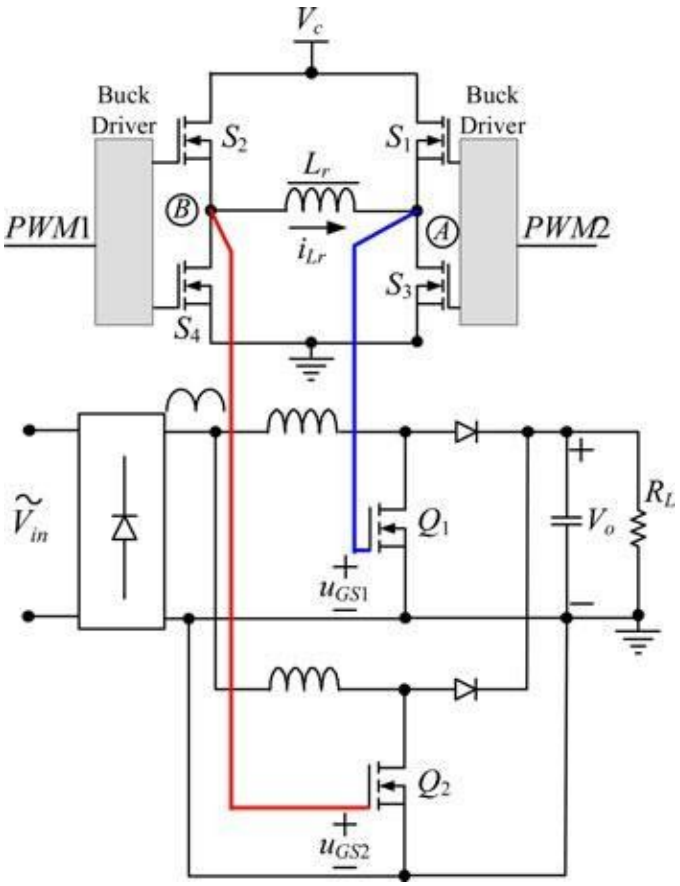


Fig.4. Interleaving boost PFC converters with the proposed adaptive CSD.

Direct torque control (DTC) is one method used in variable frequency drives to control the torque (and thus finally the speed) of three-phase AC electric motors. This involves calculating an estimate of the motor's magnetic flux and torque based on the measured voltage and current of the motor [6].

In order to find the optimized Ig max, the objective function F(Ig max) is established adding the switching loss and the CSD loss together as

$$F(I_{g\max}) = P_{\text{switching loss}}(I_{g\max}) + P_{\text{CSD}}(I_{g\max})$$

Load Conditions (W)	25% (75 W)	50% (150 W)	75% (225 W)	100% (300 W)
PF	0.992	0.994	0.998	0.999

Table 1: Measured PF values at different loads less than 100 Vac

III. SIMULATION RESULTS

To verify the proposed adaptive CSD, a 110 Vac input, 380 V/300 W output, and 1 MHz CCM boost PFC converter was built. The specifications are as follows: boost inductor L = 100 μH; output capacitance C = 220 μF; power MOSFET, the boost diode CSD06060, the CS inductor Lr = 1.5 μH (DS3316P), and the gate driver voltage Vc = 12 V. Fig. 12 illustrates the photograph of the prototype. Since there is no commercial IC available for MHz PFC applications, the discrete components were used to build the controller, saw tooth generator, and CSD circuit.

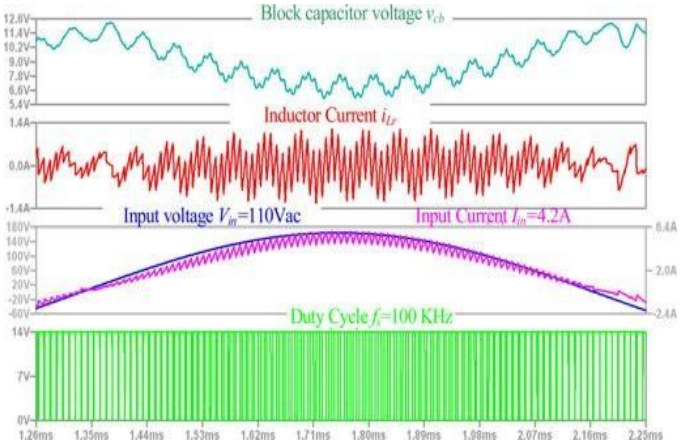


Fig.5.Simulated waveforms of the boost PFC converter with the HB CSD

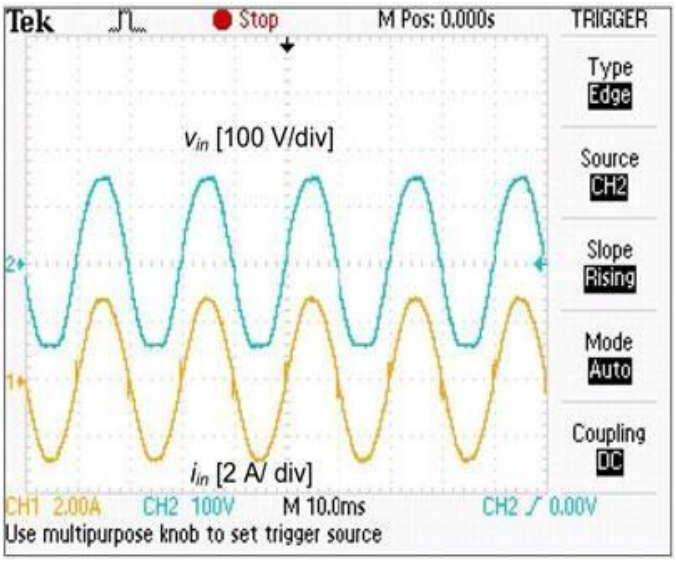
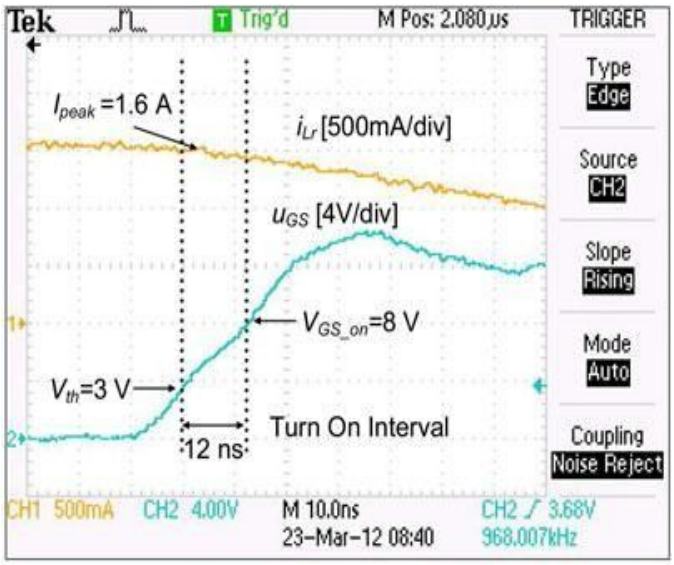
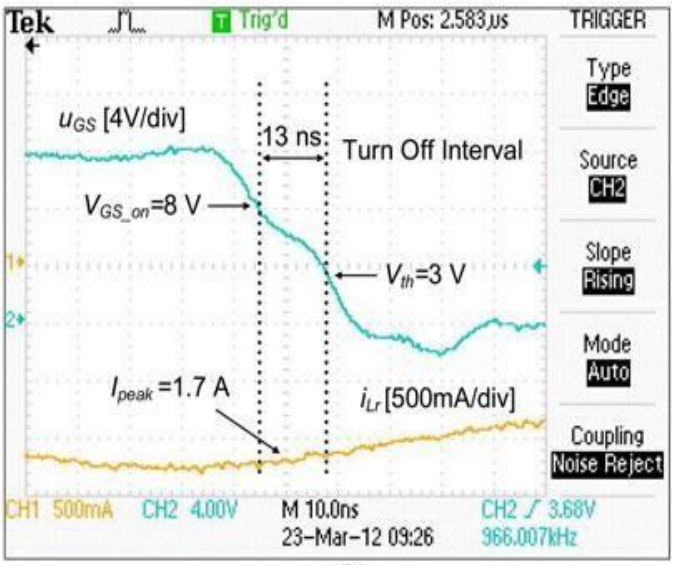


Fig.6. Input voltage and current of the power stage.

It is observed that the input line current is sinusoidal and is able to follow the input line voltage. During [t1, t2], the inductor current changes its polarity from the positive peak value to the negative peak value. During [t2, t3], the CS inductor current is circulating through S1 and S2 and remains constant in this interval. This provides a CS when the power MOSFET is turned OFF. During [t3, t4], the CS inductor current changes its polarity from the negative peak value to the positive peak value. At t4, the MOSFET can be turned ON with a CS again.



(a)



(b)

Fig.7. Turn-on and turn-off intervals: CSD.
(a) Turn-on interval. (b) Turn-off interval.

IV. CONCLUSION

Compared to other CSDs with the constant drive current, the advantage of the adaptive drive current can achieve further switching loss reduction when the power MOSFET is with a higher switching current while reduce the drive circuit loss when the MOSFET is with a lower switching current. This provides better optimal opportunity with the tradeoff between the switching loss reduction and CSD drive circuit loss during a wide operation range. With 110 Vac input and 380 V/300 W output, the CSD reduces the total loss by 12W, which translates into an efficiency improvement of 3.2% (from 89.0% to 92.2%). With 220 Vac input and 380 V/300 W output, an efficiency improvement of 1.5% is achieved over the conventional VSD.

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