Design and Analysis of NAND Gate Using 180nm and 90nm CMOS Technology

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Abstract-*real world signals are mostly based on Boolean Operators. Boolean Operators are simple words (AND, OR, NOT or AND NOT) used as conjunctions to combine or exclude keywords in a search, resulting in more focused and productive results. Especially, the work is focused NAND gate on reduction of power dissipation, which is showing the effect of transient fault on selected NMOS transistor and PMOS transistor duplication and scaling connected to the same input. After implementing the duplication and scaling circuits, power and delay analysis has been done on the bases of its power-delay product has been calculated. All the above circuits are implemented using 180nm and 90nm CMOS technology using a supply voltage of 1.8v and 1.1v in TANNER EDA TOOL.*

Keywords-NAND gate, Tanner EDA tool

I. INTRODUCTION

The NAND or "Not AND" function is a combination of the two separate logical functions, the AND function and the NOT function connected together in series.

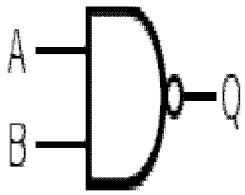

Figure 1: Symbol of NAND gate

Power consumption plays an important role and it affects proportionally to the performance of the circuit. The duplication and scaling means adding of transistors i.e connecting transistor in parallel or series to NAND gate. This paper is organized into four sections. Section I explains all basic about NAND gate. Section II discusses the design of a conventional NAND gate using 180nm and 90nm CMOS technology. Section III discusses the design of a duplication and scaling of NAND gate using 180nm and 90nm CMOS technology. Section IV deals with the implementation and results using TANNER EDA tool.

II. CONVENTIONAL NAND GATE USING 180NM AND 90NM CMOS TECHNOLOGY

Considering the truth table; Case:1) When A=B=0,both the NMOS are in OFF condition and PMOS are in ON condition. Therefore the output is connected to VDD 1.8v and 1.1v HIGH logic is present at the output terminal. Case:2) When A=0 and B=1, the upper NMOS are in OFF and lower NMOS in ON condition. Left PMOS are in ON and right PMOS in OFF condition. Therefore the output is connected to VDD and HIGH logic is present at the output terminal. Case:3) When A=1 and B=0, upper NMOS are in ON and lower NMOS in OFF condition. Left PMOS are in OFF and right PMOS in ON condition. Therefore the output is connected to VDD and HIGH logic is present at the output terminal. Case:4) When A=B=1,both the NMOS are in ON condition and PMOS are in OFF condition. Therefore the output is connected to VDD and LOW logic is present at the output terminal.

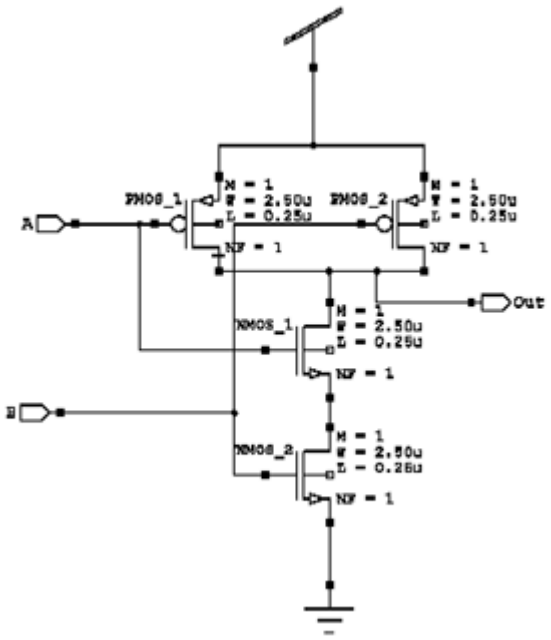

Figure 2: Conventional NAND gate

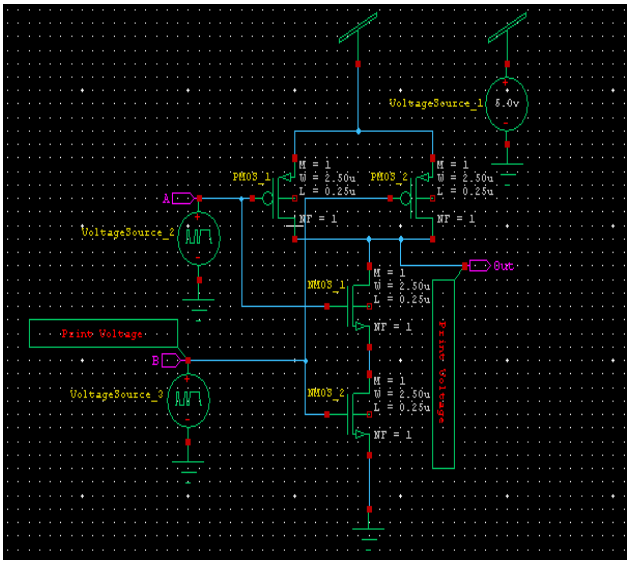

Figure 3: Conventional NAND gate with output

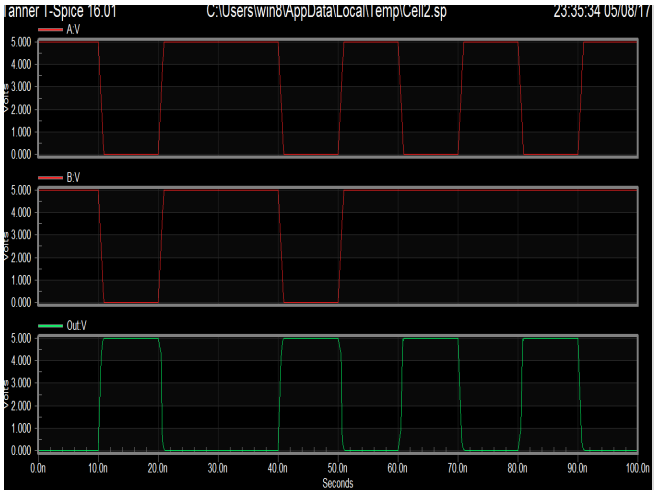

Figure 4: Transient Analysis of Conventional NAND gate Voltage

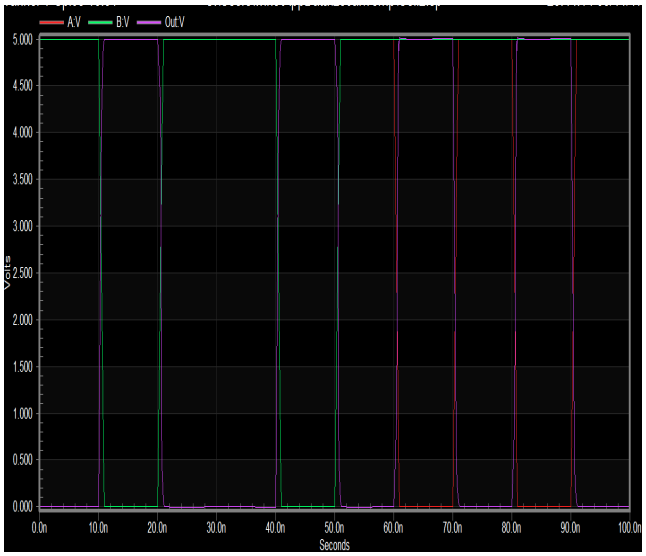

Figure 5: Transient Analysis of Conventional NAND gate Power

III. DUPLICATION AND SCALING NAND GATE USING 180NM AND 90NM CMOS TECHNOLOGY

Considering the truth table; Case:1) When p1.1=p1.2=p2=0,both the NMOS are in OFF condition and PMOS are in ON condition. Therefore the output is connected to VDD 1.8v and 1.1v HIGH logic is present at the output terminal. Case:2) When p1.1=p1.2=0 and p2=1, the upper NMOS are in OFF and lower NMOS in ON condition. Left PMOS are in ON and right PMOS in OFF condition. Therefore the output is connected to VDD and HIGH logic is present at the output terminal. Case:3) When p1.1=p1.2=1 and p2=0, upper NMOS are in ON and lower NMOS in OFF condition. Left PMOS are in OFF and right PMOS in ON condition. Therefore the output is connected to VDD and HIGH logic is present at the output terminal. Case:4) When p1.1=p1.2=p2=1,both the NMOS are in ON condition and PMOS are in OFF condition. Therefore the output is connected to VDD and LOW logic is present at the output terminal.

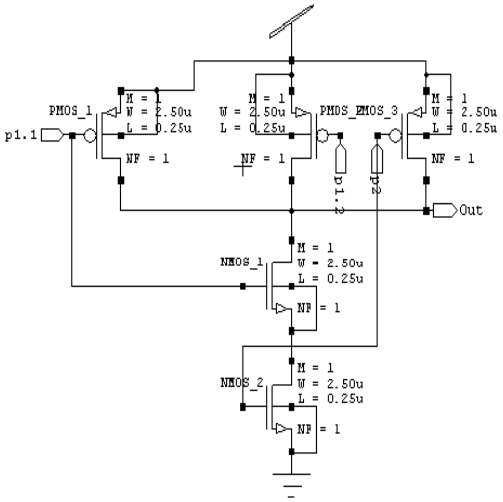

Figure 6: Duplication and scaling NAND gate

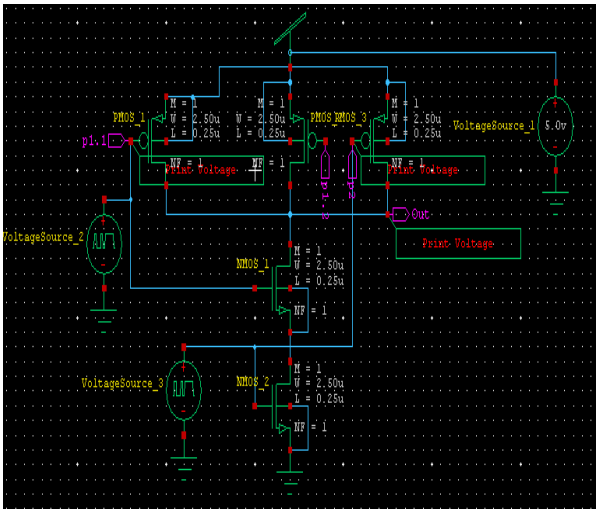

Figure 7: Duplication and scaling NAND gate with output

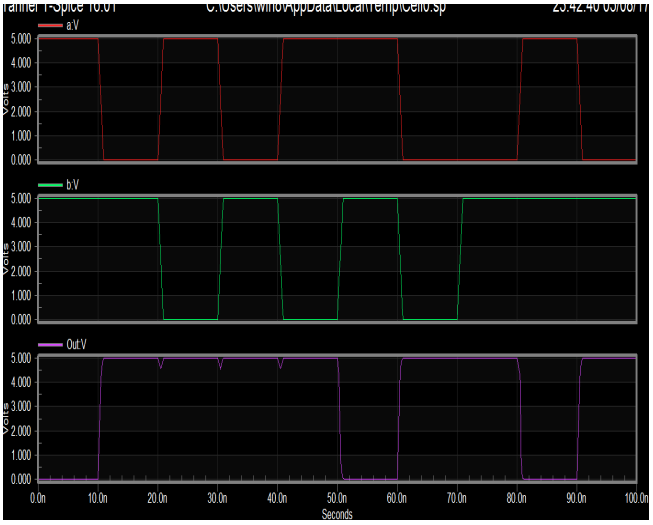

Figure 8: Transient Analysis Duplication and scaling NAND gate Voltage

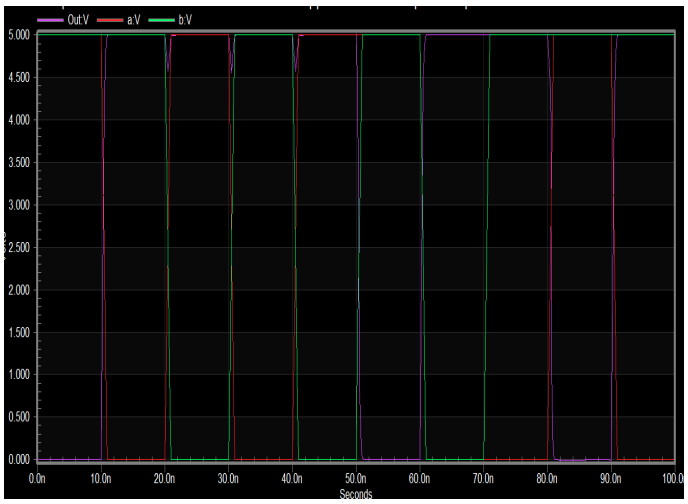

Figure 9: Transient Analysis Duplication and scaling NAND gate Power

IV. SIMULATION RESULTS

The Simulation of NAND gate is carried out with 180nm and 90nm CMOS technology. The CMOS technology parameters are taken for NMOS and PMOS in TSPICE tool. The . Conventional NAND gate is compared with Duplication and scaling NAND gate to get the difference between Average Power and Delay from the Transient Analysis.

NAND gate	DELAY	AVERAGE POWER
Conventional	84.5223p	2.910054e-004 watts
Duplication and scaling	74.1119p	1.647402e-004 watts

Table I: NAND gate result with 180nm CMOS Technology

NAND gate	DELAY	AVERAGE POWER
Conventional	81.8572p	2.815503e-004 watts
Duplication and scaling	15.4183p	1.569953e-004 watts

Table II: NAND gate result with 90nm CMOS technology

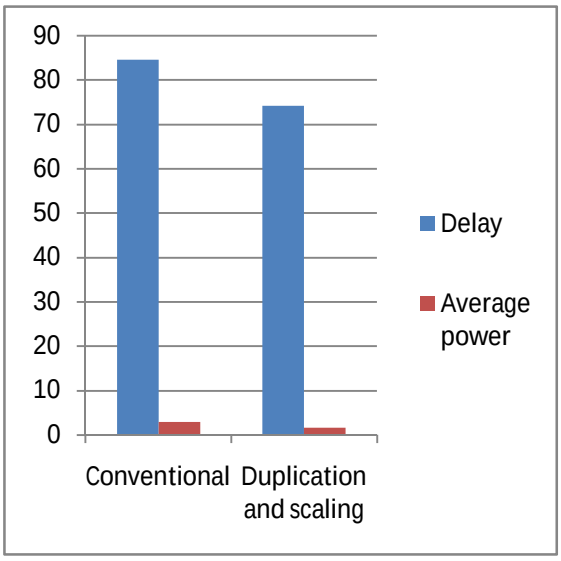

Chart I: NAND gate result with 180nm CMOS Technology Comparison of Delay and Average power of Conventional, Duplication and scaling

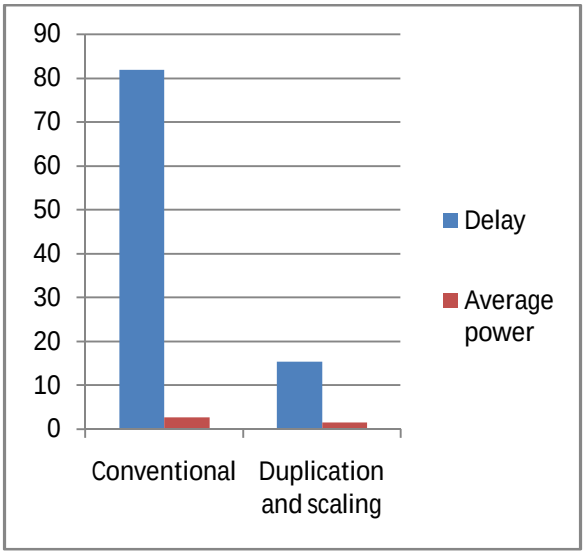

Chart II: NAND gate result with 90nm CMOS Technology Comparison of Delay and Average power of Conventional, Duplication and scaling

V. CONCLUSION

The Average power and Delay of NAND gate is represented in 180nm and 90nm CMOS technology using TANNER EDA tool.The Simulation results shows the Comparison of Delay and Average power of Conventional, Duplication and scaling with 1.8v VDD and 1.1v VDD. The Duplication and scaling can be used to minimize Average power and Delay in NAND gate.

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