FPGA Implementation of OFDM Transceiver for IEEE802.11a Wireless LAN

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Abstract- *Orthogonal Frequency Division Multiplexing, OFDM, technology is generally used in lots of high data-reception communication systems, such as Digital Audio Broadcasting (DAB), Power Line Communications (PLC), and satellite communication systems. In some WLAN specifications, e.g. IEEE 802.11a and Hiper LAN in European, or WiMAX (i.e. IEEE 802.16e, 2005 for mobile edition) in metropolitan networks, OFDM techniques are also applied. In broadband wireless communication, the delay spread caused by channel multi-path fading will usually introduce serious Inter-Symbol Interference (ISI) to the receiver. To counteract the ISI, the high-efficiency Orthogonal Frequency Division Multiplexing (OFDM) modulations first splits the high-rate data stream into a number of parallel sub-streams and modulates them onto different orthogonal sub- carriers and thus lower the symbol rate, and then add a Cyclic Prefix (CP) to the head of each symbol to reduce the influence of adjacent symbol interference. The advantages of OFDM systems are high spectrum efficiency, longer symbol duration against inter-symbols interference (ISI) effect in multi-path environments, and narrow transmission band of each sub-carrier within coherence bandwidth such that the communication channel can be viewed as flat and not frequency selective. The project is intended to design and implementation of OFDM System, which includes key blocks such as Viterbi Encoder/Decoder, IFFT/FFT, A/D, D/A, Parallel to Serial Converter and Serial to parallel Converter. The VHDL code can be simulated to verify its functionality. Then gate level design equivalent will be synthesized targeting FPGA device.*

Keywords- FPGA, VHDL, OFDM, IEEE 802.11a

I. INTRODUCTION

WLANs have become increasingly pervasive in recent years. IEEE 802.11 standard offers several is currently one of the most widely-used standards for implementing short- range WLANs The standard was designed to provide wireless connectivity and efficient data transfer for users who are either stationary or are moving with limited velocity. The first amendment to the standard, IEEE 802.11b, used Direct-Sequence Spread Spectrum (DSSS) modulation for transmitting data. Later amendments (specifically IEEE 802.11a and 802.11g) make use of OFDM, a modulation method which offers several important benefits.

Wireless communications standards and digital subscriber lines technology, in addition to other communication technologies, are utilizing the widely adopted Orthogonal Frequency Division Multiplex (OFDM) technique. This is due to the genuine advantage of OFDM over single carrier system in multi-path fading channels. Among the standards that are based on OFDM are the IEEE 802.11a&g for Wireless Local Area Networks (WLANs), WiFi, and the growing IEEE802.16 for Metropolitan Access, Worldwide Interoperability for Microwave Access (WiMAX). The fast growth of these standards has paved the way for OFDM to be among the widely adopted standards and to be as a fundamental candidate for the construction of the next generation telecommunication networks.

The aim of this work is to implement the digital baseband part of the physical layer of an OFDM transmitter that conforms to the 802.11a standard. The objective is to show FPGA's capability to accommodate such standards, and to emphasize on their programmability feature. The implementation is performed by utilizing VHDL (VHSIC Hardware Description Language), and targeting Xilinx Field Programmable Gate Arrays (FPGA). In this work, the developed IP cores, available on-line [8], could be easily extended to design other OFDM-based systems, for example fixed and mobile WiMAX.

II. WIRELESS LAN IEEE 802.11A STANDARD

The IEEE 802.11a standard document [1] specifies both the Medium Access Layer (MAC), as well as the PHYsical layer (PHY). The scope of this work is limited only to the PHY part, where in the next subsections the main blocks forming the baseband transmitter part will be discussed separately. The 802.11a standard is based on the OFDM technique of modulation, where several SCs, 52 in this standard, are used to spread the serial data stream on parallel slow rate streams. The main design parameters for the OFDM in the 802.11a standard are listed in table 1.

Table 1 OFDM Parameters in the IEEE802.11a Standard

Parameter	Value
Sampling Frequency	20MHz
Number of Sub-carriers	52(48 data and 4 pilots)
OFDM Symbol Period	4µs (80 samples)
Cyclic Prefix Period	0.8µs(16 samples)
Coding	½,2/3 and 3/4
Modulation Scheme	BPSK, QPSK, 16&64-QAM
Data rate	6,9,12,18,24,36,48&54Mbs
FFT Processor	64 point

Table 1 shows that the 802.11a standard can achieve variable data rates, starting with 6 Mbps and ending with 54 Mbps. This variation is achieved through the combination of the different coding rates and modulation schemes used. These different configurations (coding rate and modulation scheme) are used to produce the desired data rate.

III. OFDM TECNIQUE

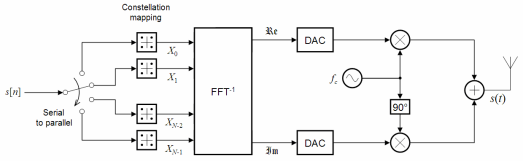
Orthogonal frequency-division multiplexing (OFDM), is identical to Coded OFDM (COFDM) and Discrete multi-tone modulation (DMT), is a frequency-division multiplexing (FDM) scheme utilized as a digital multi-carrier modulation method. Many of closely-spaced orthogonal sub-carriers are used to carry data. The data are divided into several parallel data streams or channels, one for each sub-carrier. Each sub- carrier is modulated with a conventional modulation scheme (such as quadrature amplitude modulation or phase shift keying) at a low symbol rate, keeping the total data rates similar to conventional single-carrier modulation schemes in the same bandwidth. OFDM has developed into a popular scheme for wideband digital communication, whether wireless or over copper wires, used in applications such as digital television and audio broadcasting, wireless networking and broadband internet access. The primary advantage of OFDM over single-carrier schemes is its ability to cope with severe channel conditions , for example, attenuation of high frequencies in a long copper wire, narrowband interference and frequency-selective fading due to multipath, without complex equalization filters. Channel equalization is simplified because OFDM may be viewed as using many slowly-modulated narrowband signals rather than one rapidly-modulated wideband signal. The low symbol rate makes the use of a guard interval between symbols affordable, making it possible to handle time-spreading and eliminate inter symbol interference (ISI). This mechanism also facilitates the design of single-frequency networks, where several adjacent transmitters send the same signal simultaneously at the same frequency, as the signals from multiple distant transmitters may be

combined constructively, rather than interfering as would typically occur in a traditional single- carrier system. In this project, The OFDM transeiver will be designed with VHDL language and implemented in Cyclone 2 FPGA device on DE2-70 board, which in cludes the OFDM transmitter(16 QAM modulator and length N IDFT) and receiver(length N DFT and 16 QAM demodulator).

Transmitter

An OFDM carrier signal is the sum of a number of orthogonal sub-carriers, with baseband data on each sub-carrier being independently modulated commonly using some type of quadrature amplitude modulation (QAM) in this project, This composite baseband signal is typically used to modulate a main RF carrier. Input signal of OFDM transmitter s[n] is a serial stream of binary digits. By inverse multiplexing, these are first demultiplexed into parallel streams, and each one mapped to a complex symbol stream using 16-QAM modulation

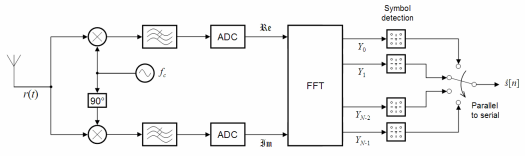
An inverse FFT is computed on each set of symbols, delievering a set of complex symbols. These symbols are then quadrature-mixed to passband by the DAC components outside of FGPA device in the standard way. The real and imaginary components are first converted to the analogue domain using digital-to-analogue converters (DACs); the analogue signals are then used to modulate cosine and sine waves at the carrier frequency, *fc*, respectively. These signals are then summed to give the transmission signal, *s(t).*



Receiver

In the receiver direction, antenner picks up the signal r(t), which is then quadrature-mixed down to baseband using cosine and sine waves at the carrier frequency. This also creates signals centered on 2fc, so low-pass filters are used to reject these. The baseband signals are then sampled and digitised using analogue-to-digital converters (ADCs) and then pass to the OFDM receiver in FPGA, inside the FPGA, a forward FFT is used to convert back to the frequency domain. This returns parallel streams, each of which is

converted to a binary stream using an 16-QAM demodulator. These streams are then re-combined into a serial stream, which is an estimate of the original binary stream at the transmitter



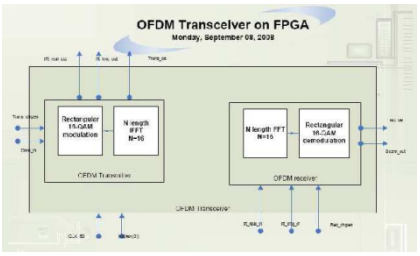
Goal of the project

The goal of the project is to design the OFDM transmitter(16 QAM modulator and length N IDFT) and receiver(length N DFT and 16 QAM demodulator) on Cyclone 2 device of DE2_70 board ultilizing the Quartus 2 FPGA developing tool and then demonstrate its function on DE2_70 board by utilizing the LCD and 7 segment display. In the demonstration, the input bit stream test vectors will be converted from the serial to parallel, pass to 16-QAM modulation, IFFT. Then these complex symbols will directly be converted from parallel to serial again and pass to OFDM receiver inside the FGPA. The receiver will convert the I, Q data back to the original binary data by going through the process of serail to paraller, FFT, 16-QAM demodulation, and parallel to serial conversion.

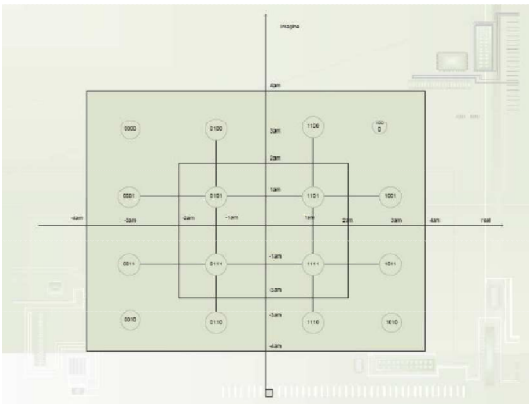
IV. FPGA DESIGN OF OFDM TRANSCEIVER

a. OFDM transceiver design

The OFDM transceiver block diagram is as follows.



In our design implementation, due to the need of changeable length N of DFT, we will use the length N DFT and IDFT depicted another project paper "ECE698 Length N DFT designs of OFDM for FPGA implementation" instead of using real FFT and IFFT modules. OFDM transmitter will be activated when "trans_chipen" signal is high, the input bit stream "Qam_in" will be mapped to complex symbols every 4 bits in 16-qam modulator which has the constellation map as follows



The complex symbols amplitude of QAM output could be adjust by "am" generic constant of the VHDL program, in our program, the default value of "am" is set to 16, e.g., for "0101" input, the output of 16_QAM is "(-1+j)*16". The default length of IFFT in our design is 16, the IFFT is actually the length N IDFT program, not the IFFT. It needs N clocks delays for the transforms.The Transmitter will send out the "trans_oe" as the enable signals to the next level component as well as the "ifft_real_out" and "ifft_img_out" for DAC which is real and imagine part of the IDFT results. OFDM receiver will be activated by the "rec_chipen" when it is high, the input of "fft_img_in" and "fft_real_in" is the imagine and real part of complex number from ADC, the receiver will pick up N=16 complex symbols every frame and converter to another batch of 16 complex symbols by length 16 DFT, then map them back to 4 bit binary signals in serial by 16- QAM demodulation. If we loop the transmitter output back to receiver input, we will get the original bit stream back. It is demonstrated in the function and timing simulation as follows. Also, it will be demonstrated on DE2-70 Demo board later In the function simulation, bit stream input "qam_in" to transmitter is set 0 to 15 repeatedly, we will get the "0, -18-14j, 0, -1-8j, -8+24j, -5, 0,-3-2j, 0, -3+2j, 0, -5, 8+24j, -1+8j, 0, -14+18j" 16 sets of complex symbols on "ifft_real_out" and "ifft_img_out" buses repeatedly after 18 clocks delays. For the loop test, we need to set the "fft_img_in" and "fft_real_in" of receiver input signals to the same value of transmitter output, which you will see as follows in the vector wave form input files for the function simulation.

V. STANDARD IMPLEMENTATION DETAILS

The used methodology is based on the divide-and-conquer approach. Each block in the architecture was designed and tested separately, and later those blocks were assembled and extra modules were added to compose the complete system The design makes use of pipelining, and this was mainly achieved through duplicating the memory elements

(registers or RAMs); that will buffer the incoming stream of bits while the previous stream is being processed. The design environment was based completely on the Xilinx Integrated Software Environment (ISE), and targeting the Xilinx Virtex-II Pro and Spartan-3E FPGAa. Each block design will now be discussed, focusing on the main design issues.

Next comes coding, which is divided into two substages. The final purpose of the coding stage is to provide the receiver with the capability to detect and correct errors through redundancy One of the widely used block interleaver designs is based on a RAM where the data is written in row order, and then read in column order ,However, during the implementation it was found that this technique will consume a lot of multiplexers, as well as the need to have RAMs with different sizes according to the interlever size The proposed design in this work is based on utilizing lookup tables; those were implemented as small read only memories (ROM). One ROM was generated for each interleaver size required.

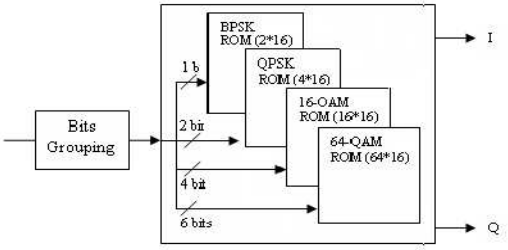


Figure : Mapper Architecture

To perform IFFT, the interleaved bits are translated or mapped into two components the In-phase and the Quadrature (I and Q) components. Depending on the PHY mode and the data rate selected, the OFDM sub-carriers aremodulated using BPSK, or 16-QAM The last 16 samples of the generated OFDM symbol are copied into the beginning to form the cyclic prefix. In the 802.11a standard, the last 16 samples of the IFFT output are replicated at the beginning to form an 80 sample complete OFDM symbol. These 3 samples correspond to a 0.3 μsperiod, which is considered as the maximum delay in the multipath environment. This stage was implemented by using single-port distributed RAMs. The first is of a size 16*16 bits, which is used to store the cyclic prefix samples., and it is used to hold the OFDM symbol samples. Again, another copy of each RAM (CP and Symbol RAMs) is added to provide pipelining.

VI. IMPLEMENTATION RESULTS

The work presented in this paper aimed to demonstrate the capability of a straight forward translation of a wireless communication standard into a pure VHDL implementation, and therefore to be implemented on a reconfigurable platform. The approach of divide and conquer was used to design and test each entity alone and later combine the complete system. The work has accomplished the task of designing the digital baseband part of an OFDM transmitter that conforms to the IEEE802.11a standard. As it was stated in the implementation details section, the design is based on two main processes. The first is bit manipulation in coding and interleaving stage, while the second process is mapping through utilizing both look-up tables and memory. Therefore, the most resources consumed by the design will be the pure LUTs available on the FPGA and the memory elements as well. However, the most complex part that requires digital signal processing function,

The design was targeted to be mapped on Xilinx FPGA [7], and two FPGAs were selected Xilinx Virtex-II Pro (XC2VP30-7ff896) and Xilinx Spartan-3E (XC3S500E). The selection was based on the availability of the IFFT and DCM cores in both FPGAs, and also to demonstrate the possibility and to compare the mapping on both chips. Table 2 presents the resources required by the IEEE802.11a standard transmitter after mapping it on the XC2VP30 chip. The table lists the number of resources utilized and the percentage of the used/available resources on the selected FPGA the IFFT block, was designed using the available IP core.

VII. CONCLUSION

The capability of designing and implementing an OFDM system was presented in this work. The design considered using a pure VHDL with the aid of available IPs to implement the IFFT and clock synthesis functions From the mapping results, the design can easily fit into Xilinx FPGA with an occupation percentage around 25 %. , the mapping results showed that smaller FPGAs such as Spartan-3E were not able to accommodate the complete design where the placing and routing phase has failed to finish. In addition, the results were compared to previous work and showed improved results in certain resources.. The project is intended to design and implementation of OFDM System, which includes key blocks such as Viterbi Encoder/Decoder, IFFT/FFT, A/D, D/A, Parallel to Serial Converter and Serial to parallel Converter. The VHDL code can be simulated to verify its functionality. Then gate level design equivalent will be synthesized targeting FPGA device.

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