A Reliable Low Power Merged LNA and Mixer for Medical Implant Communication Services

G. GovindaGiri [1], K.RamakarishnaReddy[2]
[1, 2] Department of Electronics and Communication Engineering
[1, 2] TKRCET

Abstract- *This project investigates low-power design of an LNA and a down-conversion mixer of a receiver for MICS applications. The key idea is to stack an LNA and a mixer, while the LNA operates in the normal super-threshold region and the mixer in the subthreshold region. In addition, a gm-boosting technique with a capacitor cross-coupled at the LNA input stage is also adopted to achieve a low noise figure (NF) and high linearity, which is critical to the overall performance of the receiver. The mixer operating in the sub-threshold region significantly reduces power dissipation and relaxes the voltage headroom without sacrificing the LNA performance. The relaxed voltage headroom enables stack of the LNA and the mixer with a low supply voltage of 1.2 V. The proposed circuit is designed in 0.18 μm RF CMOS technology. The merged LNA and mixer consumes only 1.83 mW, and achieves 21.6 dB power gain. The NF of the block is 3.55 dB at 1 MHz IF, and the IIP3 is -6.08 dB*

Keywords- Face detection, Face Recognition, Eye Detection

I. INTRODUCTION

The FCC allocated the spectrum of 402-405 MHz for MICS (Medical Implant Communication Services) applications in . The regulations apply to transceivers that support the diagnostic and/or therapeutic functions associated with implanted medical devices such as implantable cardioverters, and drug infusion/dispensing. Recently, IEEE developed the draft IEEE 802.15.6 standard for Wireless Body Area Network (WBAN), which designated seven candidate frequency bands including the MICS band. The WBAN standard can play a prominent roll to promote wireless medical implantable devices. The basic requirements for the transceiver specially designated for the purpose are low power consumption, minimum external components, and small device size. A key design challenge for implantable devices is to prolong the device operation time typically powered by batteries. More specifically, minimization of the power consumption for the RF circuitry poses a critical design issue while achieving good performance. Many works on low power circuit design of RF building blocks such as LNAs and mixers are reported in [5]-[8]. Those papers. specially investigated a merged LNA and mixer structure. [6] and [8] adopt stacking to reuse DC current in multiple blocks while [5] and [7] choose a folded structure. In addition, a gm-boosting technique, and sub-threshold operation is used in [3], [5]. Few literatures present a transceiver or a receiver design for MICS applications [1], [2]. However, the power dissipation is still high in [1], or noise performance is notably poor as a result of subthreshold operation in [2]. In this paper, we investigate stacking of a LNA and a down-mixer for MICS applications. A key idea adopted for our circuit is to operate the LNA in the normal saturation region while the mixer in sub-threshold region. Besides that, a gm-boosting technique is implemented with capacitors cross-coupled at the LNA input stage. Hence, the LNA achieves low noise figure (NF) and high linearity, which is critical to the overall performance of a receiver. The mixer operating in sub-threshold region reduces the power dissipation. The proposed circuit was designed in TSMC 0.18 ȝm RF CMOS technology. The paper is organized as follows. Section II describes key specifications for the MICS band of the WBAN standard and reviews sub-threshold circuit operation. Section III describes the proposed circuit design. Section IV presents simulation results and the performance such as power consumption, noise, power gain, and linearity. Section V summarizes the paper.

II. PRELIMINARY

A. MICS band and WBAN standards

The major specifications of the WBAN standard for MICS band are as follows

- Frequency: 402-405 MHz
- Symbol rate: 187.5 kbps
- Date rate: 57.5 ~ 455.4 kbps
- Pulse shape: Squared Root Raised Cosine (SRRC) To comply with the modulation method among the draft standards, the RF receiver has to manage quadrature signals (I/Q).

B. Sub-threshold RF circuit

The sub-threshold biasing technique has been widely adopted in digital, analog, and even RF circuits [1], [3]. The main advantage of sub-threshold operation is the significant

power saving. The drain current under the weak inversion of MOSFET is given by

$$Id = (w/l)Idoe^{n(vgs/(kt/q)}$$

where IDO is a process-dependent factor, n a sub-threshold slope factor, k the Boltzmann constant, T the temperature (K), and q the charge of an electron. Since vGS in (1) is a gate-source voltage, which is smaller than the subthreshold voltage of MOSFET, sub-threshold circuits require low voltage headroom and so favorable to stack circuits under a low supply voltage. However, the sub-threshold operation also induces challenges to the circuit designer. First, the magnitude of gm is notably small compared to that under the strong inversion operation. As we consider designing a common gate (CG) amplifier as an input stage of the LNA, a large gm contributes a better noise performance. Moreover, the gate-induced noise of the MOSFET is dominant under the sub-threshold operation. As a consequence, the subthreshold operation might not be beneficial for the input stage of the LNA. Secondly, the ft in the weak inversion is much lower [3] than that in the strong inversion.

The front-end circuit is designed to supplement an IF (intermediate frequency) super-heterodyne receiver. The low IF down-conversion avoids the flicker noise and DC offset associated with a direct-conversion. It contributes reliability, and a simple filter design following by the LNA and mixer. The proposed merged LNA and mixer circuit is designed in CMOS RF 0.18 ȝm technology. The overall circuit schematic is shown in Fig. 2.

A. LNA design

As the LNA is the first circuitry of the receiver, the main considerations of LNA are input matching, low noise figure, and high gain. In Fig. 1, transistor M1 and M2 realize a CG LNA. The main advantage of a CG amplifier is a simple input matching with 1/gm method [4], typically to 50 :. However, the opposite contribution of gm value to a noise performance requires some remedy to the circuit. In this work, the capacitor cross-coupled method with CC1,

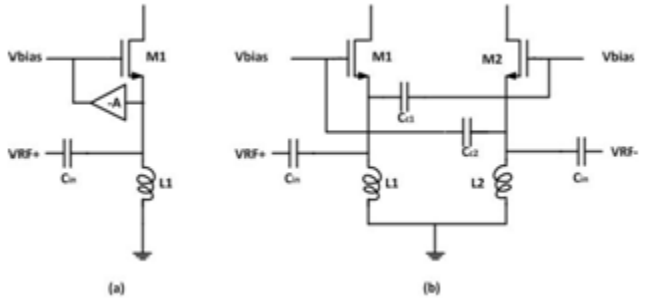
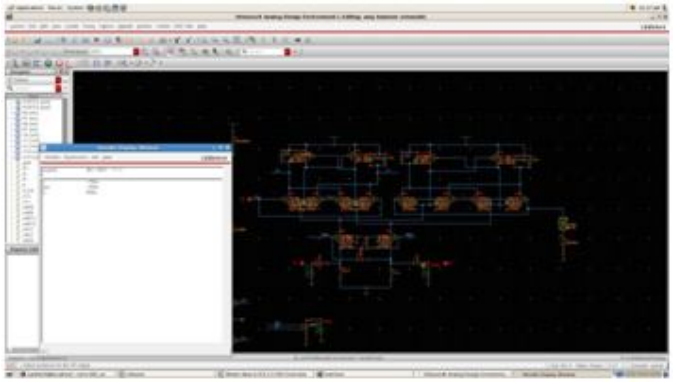


Figure 1. (a) gm-boosted CG LNA topology, and (b) gm-boosted CG LNA implemented with capacitors cross-coupled is adopted as a gm-boosting scheme to solve the contradiction [4], [5], which is shown in Fig. 1. The capacitor between a gate to a source provides an inverting gain A, and decouples the link between the input matching and the noise performance. As a consequence, the Rin and Noise Factor, F, of the CG amplifier can be calculated as where 0 , and ¥ are empirical process- and biasdependent parameters [4]. As can be seen in the (2), and (3), choosing a proper value of CC1,2, which determines A value enhances the noise performance while keeping the input matching.

B. Mixer design

To support BPSK modulation, two double-balanced mixers are implemented on the top of the LNA as shown in Fig. 2. Transistors from M3 to M10 work like switching pairs with LO signals, and produces In (I) and Quadrature (Q) phases of IF signals. The RC tank considered with load capacitors at the mixer output builds a low pass filter that filters out the high order harmonics. The merged LNA and mixer does not require an interstate matching network, thus save chip area and cost. Moreover, the reused current from LNA to Mixer saves DC power consumption through the overall circuit. In this circuit, fully differential structure is adopted, which contributes the noise performance by suppressing the common-mode noise. Our strategy of the mixer is a sub-threshold operation while the input LNA stage operates in strong inversion. In consequence, the noise performance of the LNA is not degraded, and the output swing of the mixer has enough margins even though with a low supply voltage of 1.2 V. As addressed in the preliminary, transistors under weak inversion has a lower ft comparing to that under strong inversion. However, it does not affect in our design because MICS band is allocated between 402-405 MHz.



LNA and MIXER design circuit

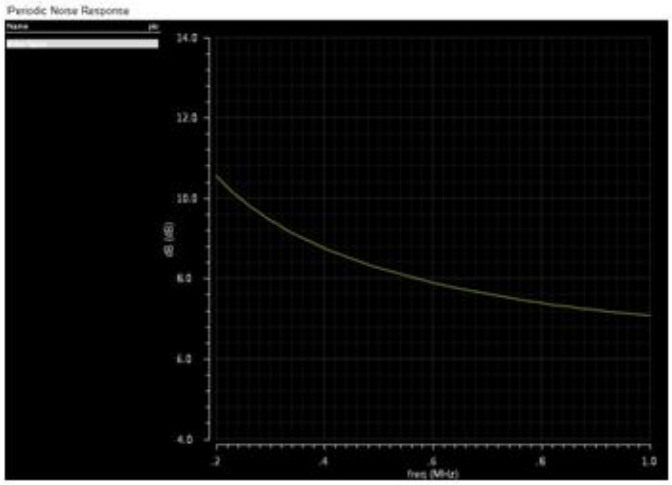


Figure 3. Noise Figure vs IF frequencies

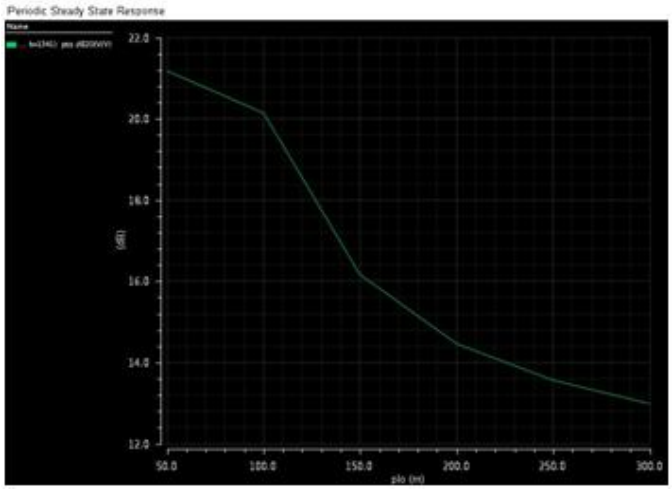
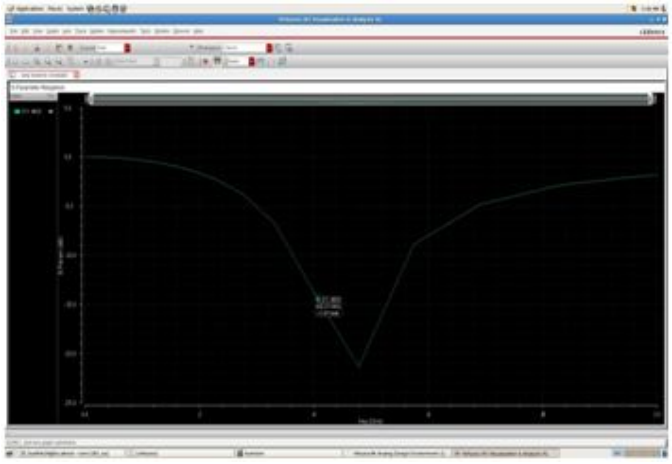


Figure 4. Conversion Gain vs operating frequencies



IV. SIMULATION RESULTS

The merged LNA and Mixer is designed in RF CMOS 0.18 um technology and simulated with SpectreRF. The overall circuit consumes 1.84 mW with a supply voltage of 1.2 V. Thanks to the gm-boosting strategy, the noise figure is measured as less than 3.6 dB over the IF frequency up to 50 MHz except DC point shown in Fig. 3. Fig. 4 illustrates the conversion gain. The maximum gain of 21.6 dB is obtained at the 404 MHz with a fixed IF frequency of 1 MHz. S11 is less than -25 dB through the MICS band shown in Fig. 5, which means the subthreshold operation of switching transistors does not degrade the input matching. To analyze linearity performance, the two-tone test is held. P1dB is obtained at the input power of -19.214 dBm while an input RF power is given between -85 dBm to -50 dBm. IIP3 is measured at the input power of -6.8 dBm shown in Fig. 6. The performance of this proposed circuit is summarized and compared with other works in Table 1. All works listed in the Table 1 are merged LNA and mixer designs [5]-[8]. The NF of [8] is comparable with that of our design, however the power consumption of the work is unacceptably high for the MICS applications.

V. CONCLUSION

The sub-threshold merged LNA and mixer circuit is designed and simulated in the RF CMOS 0.18ɜm technology. The circuit is specially targeted for MICS applications complying with the WBAN standards, therefore the operating frequency residues in 402-405are implemented. MHz and the mixer provide I/Q signals. The main key feature of this design is that transistors in the input amplifier stage operate in strong-inversion while transistors consisting mixer are optimized to operate in weak inversion. With obtained results of a super low power consumption and reliable noise performance, this work proves it is well suited for MICS applications

REFERENCES

[1] M.R. Nezhad-Ahmadi, G. Weale, A. El-Agha1, D. Griesdorf, G. Tumbush, A.Hollinger, M.Matthey, H.Meiners, S. Asgaran, “A 2mW 400MHz RF Transceiver SoC in 0.18um CMOS Technology for Wireless Medical Applications’,

[2] ν Peter D. Bradley “An Ultra-Low Power, High Performance Medical Implant Communication System (MICS) Transceiver for Implantable Devices”, Zarlink Semiconductor (ULP Communications).

[3] H. S. Savci, Z. Wang, N. S. Dogan, E. Arvas, “MICS transceivers: regulatory standards and applications [medical implant communications service].