Design Of Low-Power High-Gain Serializer/ Deserializer Using GDI Technique

Nirmaladevi J[1], V. Annpoorani[2]
[1, 2] Dept of Electronics and Communication Engineering
[1, 2] Mahendra Institute of Technology Mahendrapuri, Namakkal, India

Abstract- *CMOS technology is evolving Propose and demonstrate a serializer/deserializer (SerDes) toward the testing of large scale GDI circuits with delay-line clocking. A SerDes, a pair of a serializer (parallel-to-serial converter) and a deserializer (serial-to-parallel converter), is an important circuit block in cryogenic experiments. For instance, the number of available Input/Output (I/O) cables is limited by equipment such as a cryostat and cryoprobe, so that it is crucial to reduce the number of I/O cables as much as possible using a Ser/Des, especially when testing a large scale superconductor circuit. In RSFQ logic, serializers and deserializers are implemented by shift registers, which store data during Serial-to-Parallel (S2P) and Parallel-to-Serial (P2S) conversion. As for GDI logic, we previously proposed and demonstrated the feedback type SerDes , where an GDI buffer chain with feedback paths operates in a similar way to a shift register. However, this Ser/Des was developed for four-phase clocking and does not operate in delay-line clocking, because feedback paths are difficult to make in delay-line clocking due to the low latency. Therefore, we develop a novel SerDes for testing delay-line-clocked GDI circuits by combining GDI and RSFQ technologies, which we refer to as the GDI hybrid SerDes.*

Keywords- Adiabatic logic, GDI technique, Low power, high frequency, SerDes.

I. INTRODUCTION

The advancement of semiconductor processing technology has facilitated processors to compute huge amount of data. To fully utilize this effort IO link should also scale up in terms of bandwidth with minimal effect on pin count, area and power. Traditional parallel links has been used in circuits for long time, where the skew between clocks and data lanes in the link become difficult to control with faster data rate. The alternate is to go with faster serial links. Serial IO communication comes with set of challenges namely channel loss, ISI, crosstalk, added complexity in the receiver to facilitate clock recovery from data streams.

Data transmission is the transfer of data between two chips on the same board orinter circuit board. Nowadays there are two common methods of data transmission: parallel communication and serial communication. As technology advanced and data rate increased to multi gigabits range, serial communication has become a preferred method compare to parallel communication, due to less number of pin count, area and power.

A device called SerDes (Serializer/Deserializer) allows transfer data serially and it is playing a very important role in high-speed applications. It is capable of converting parallel data to serial and vice versa.

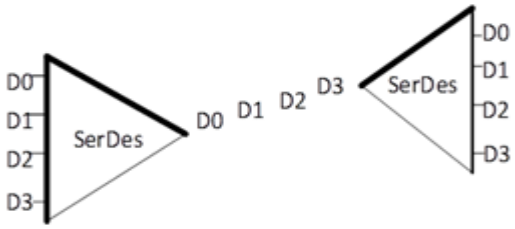


Fig.1. SerDes Link

The purpose of the transmitter to send high-speed data stream through a channel to a receiver by delivering high-speed voltage swing at the pins of the transmitter shows a typical block diagram of the transmitter block. Four major functions are performed in the transmitter, parallel to serial conversion, clock generation, feed-forward equalization and line driving. The transmitter input is n bit parallel data stream, following serializer block which will convert n bit low-speed parallel data into high-speed serial data. PLL will generate a multi-phase clock based on an external reference clock. FFE in a transmitter is used to cancel ISI (Inter-symbol interference) effect. The driver is used to match the output impedance of the transmitter to channel (Transmission line) impedance.

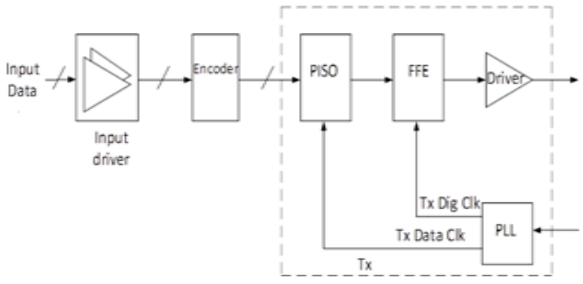


Fig.2. Block Diagram of Transmitter

The main function of receiver is to perform equalization and recover data and clock.

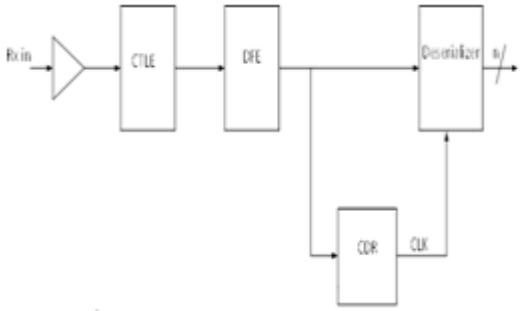


Fig.3. Block Diagram of Receiver

II. GDI TECHNIQUE

Gate Diffusion input (GDI) a new technique of designing low-power digital combinational circuit is described. This technique allows reduction in power consumption, transistor count, propagation delay and area of digital circuits. This approach allows implementation of a wide range of complex logic functions using only two transistors. GDI proposes and compared with traditional CMOS. Comparison of GDI transistor count with CMOS is presented. . Simulation result shows that the propose GDI has better performance in terms of power consumption and transistor count in compared to CMOS design.

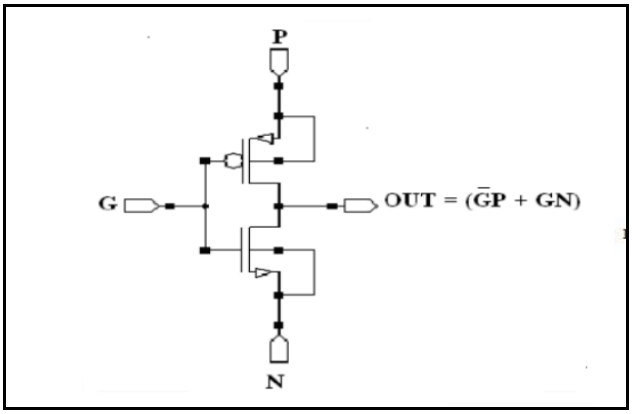


Fig.4. GDI Based Design

III. DESIGN AND IMPLEMENTATION OF SERIALIZER/DESERIALIZER

The block diagram of proposed PISO (Serializer) and SIPO (Deserializer) along with the detail description of each block. This PISO is designed to convert 40 bit parallel data into 28 Gbps serial data and SIPO is designed to convert 28 Gbp serial data into 40 bit parallel data.

PISO Architecture

In this design both single and multi-phase architecture are used. Here 40-bit parallel data from PMA will be loaded in serializer block for every rising edge of the clock Tx par clk in. Tx par clk in and sync en are used to enable the synchronizer block to generate sync 2p and sync 2nsignals, which will be used to enable shift registers, dividers. Parallel to serial convers on happens successively 40→20→4→2→1.

First stage of PISO is 40→20 which is lows peed stage and implemented using single phase clock-based architecture. Second stage 20→4is implemented using multi-phase clock and shift registers-based architecture. Final stages 4→2→1, which are high speed and most power consuming stages are implemented using Differential D flip-flop which has very low timing requirements and less power-hungry compare to other flip-flop topologies.

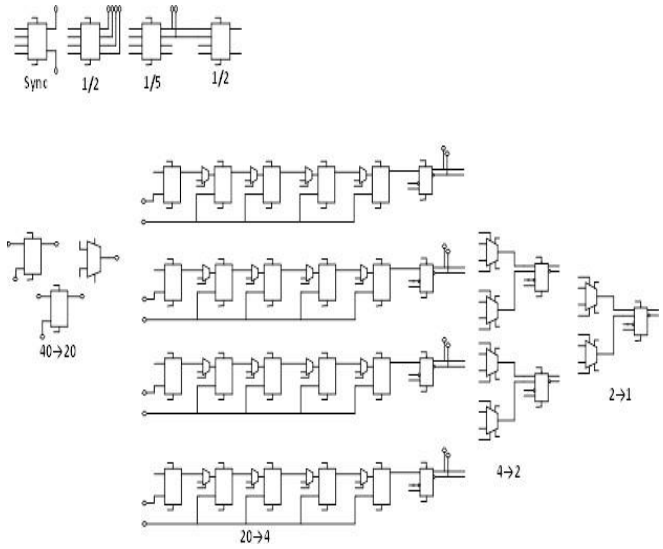


Fig.5. Top Level Block Diagram of Proposed PISO

SIPO Architecture

The top-level architecture of proposed Deserializer. Binary stage-based architecture has been used to convert high speed serial data into 40-bit parallel data. Here high speed data from CDR will be loaded in deserializer block for every rising edge of the clock Rx par clk in.Rx par clkin and sync are used to enable the synchronizer block to generate sync 2p and sync 2n signals, which will be used to enable shift registers, dividers. Serial to parallel conversion happens successively 1→2→ 4→8→40.

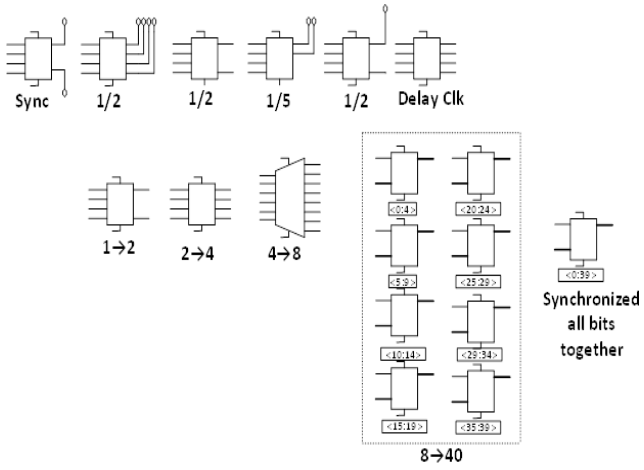


Fig.6. Top Level Block Diagram of SIPO

IV. RESULT ANALYSIS AND DISCUSSION

Tanner Tools Pro is a software suite for the design, layout and verification of analog, mixed-signal, RF and MEMS ICs. Tanner Tools Pro consists of fully-integrated front end and back end tools, from schematic capture, circuit simulation, and waveform probing to physical layout and verification.

T-Spice Pro, Tanner EDA's design entry and simulation system includes S-Edit for schematic capture, T-Spice for circuit simulation and W-Edit for waveform probing.

SIMULATION RESULT

Designing of op-amp The Op-Amp design process mainly involves the two major steps. First one is called Design conception while another one is termed as Design optimization. Architecture is proposed to meet the given specifications in design conception. This step is usually done to calculate the design values by hand calculations which are necessary for choices that must be made.

The "first-cut" design is taken & verified for the specifications and then optimized in the second step of the design optimization. The optimization can include different environmental influences or process variations and is usually done by using Computer simulation.

T-Spice is a complete design capture and simulation solution that provides accuracy and convergence with market-proven reliability. To transform your ideas into designs, you must be able to simulate large circuits quickly and with a high degree of accuracy. That means you need a simulation tool that offers fast run times, integrates with your other design tools, and is compatible with industry standards. To transform your ideas into designs, you must be able to simulate large circuits quickly and with a high degree of accuracy.

S-EDIT (SCHEMATIC CAPTURE)

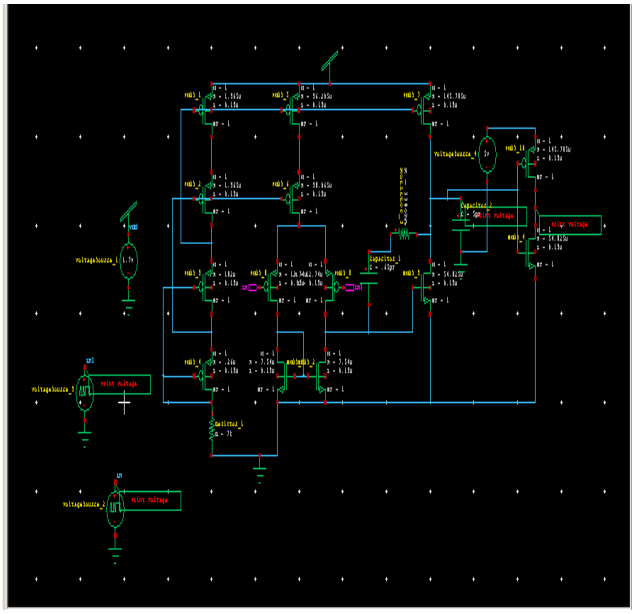
Tightly integrated with Tanner EDA's T-Spice™ simulation, L-Edit™ layout, and HiPer™ verification tools, S-Edit gives you the power you need to handle your most complex full custom IC design capture. Its efficient design capture process integrates easily with third-party tools and legacy data. S-Edit enables you to explore design choices and provides an easy-to-use view into the consequences of those choices.

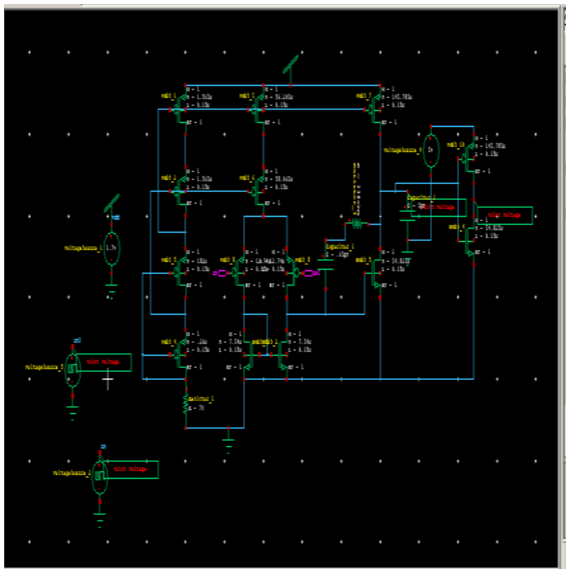
W-EDIT (WAVEFORM VIEWING & ANALYSIS)

The W-Edit waveform analysis tool is a comprehensive viewer for displaying, comparing, and analyzing simulation results. W-Edit provides an intuitive multiple-window, multiple-chart interface for easy viewing of waveforms and data in highly configurable formats.

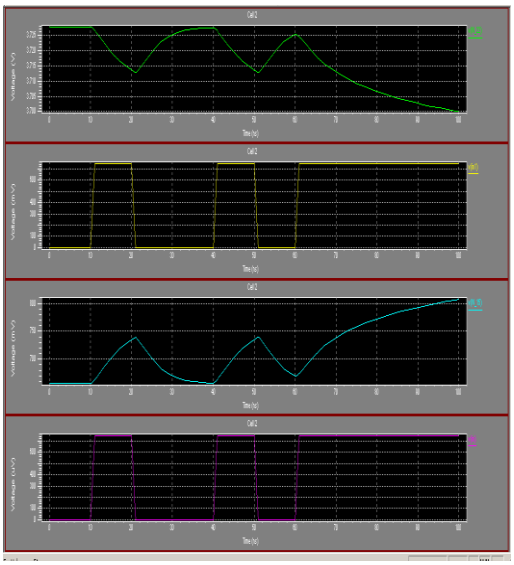
Tanner EDA's L-Edit Pro is a comprehensive physical layout and verification system that accelerates design cycles by combining the fastest rendering available with powerful features that exceed the needs of the most demanding user. This leading analog/mixed signal IC design tool enables you to get started with minimal training. You can draw and edit quickly, with fewer keystrokes and mouse clicks than other layout tools. Using powerful features such as interactive DRC, object snapping, and alignment, you can work more efficiently to save time and money.

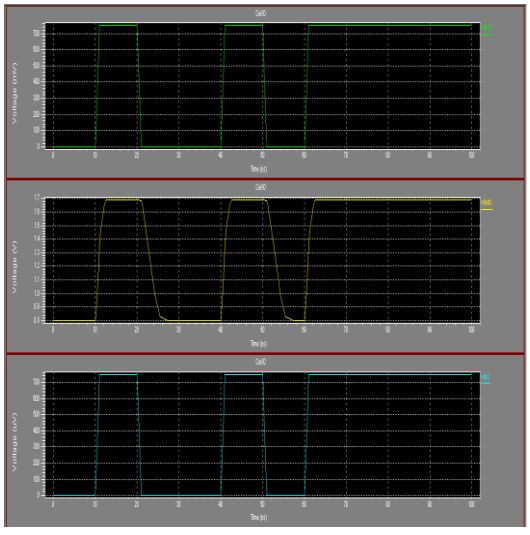
S-EDIT DESIGN





W-EDIT DESIGN





IV. CONCLUSION

In this paper the proposed the GDI hybrid SerDes toward the testing of large-scale GDI circuits with delay-line clocking. The hybrid SerDes comprises RSFQ shift registers for storing data during S2P and P2S conversion and GDI interfaces for transmitting data between the shift registers and the GDI CUT. Moreover, all the component circuits in the hybrid SerDes are seamlessly clocked by a single excitation current to synchronize the GDI and RSFQ parts.

We fabricated and tested an 8-to-3 encoder integrated with the hybrid SerDes, which is the largest delay-line-clocked GDI circuit ever designed, at 4.2 K up to 4.5 GHz, there by demonstrating that the hybrid SerDes enables the testing of delay-line-clocked GDI circuits with only a few I/O cables at high clock frequencies. Our next step is to demonstrate even larger GDI circuits using the hybrid SerDes

REFERENCES

[1] YUKI HIRONAKA 1, TAIKI YAMAE 1,2, CHRISTOPHER L. AYALA 3, (Senior Member, IEEE), NOBUYUKI YOSHIKAWA 1,3, (Senior Member, IEEE), AND NAOKI TAKEUCHI 4,1. “Low-Latency Adiabatic Quantum-Flux-Parametron Circuit Integrated With a Hybrid Serializer/Deserializer” Department of Electrical and Computer Engineering, Yokohama National University, Yokohama, Kanagawa 240-8501, Japan 2022.

[2] T. R. Daram, B. N. Sri, D. Indhuja, G. Manisha, and A. K. Rao, “Low Power Design Of Carry Look Ahead Adder By Using Adiabatic Logic,” *Int. J. Adv. Sci. Technol.*, vol. 29, no. 7, pp. 5271–5282, 2020.

[3] M. Chen and C. K. Yang. A 5064 gb/s “serializing transmitter with a 4-tap, lc-ladder-filter-based ffe in 65 nm cmos technology” IEEE J. Solid-State Circuits, 50(8):1903–19016, 2015.

[4] Rishi Ratan.”Design of a phase locked loop based clocking circuit for high speed serial link applications” University of Illinois at Urbana-Champaign, 2014.

[5] K. Mangla and N. Mangla, “Power Dissipation of Combinational Circuits By Adiabatic Technique for 180nm CMOS Technology,” *IJLTEMAS*, vol. III, no. Vi, pp. 179–186.

[6] Akshitha and N. Rajan, “Power reduction of half adder and half subtractor using different partial adiabatic logic styles,” in *Proceedings of the International Conference on Intelligent Sustainable Systems, ICISS 2019*, 2019, no. Iciss, pp. 87–92, doi: 10.1109/ISS1.2019.8908104.

[7] D. B, “Design and Implementation of Low Power Efficient 8-bit Carry Look Ahead Adder using Adiabatic

Technique," *Int. J. Res. Appl. Sci. Eng. Technol.*, vol. 7, no. 5, pp. 2857–2862, 2019, doi: 10.22214/ijraset.2019.5471.

[8] R. Khanai and S. Mavinkattimath, "Partial Adiabatic Logic," *Int. J. Comput. Appl.*, vol. 182, no. 14, pp. 10–15, Sep. 2018, doi: 10.5120/ijca2018917653.

[9] Amr Elshazly Yan-Yu Huang Hang Song Kai Yu Frank O Mahony Jihwan Kim, Ajay Bal-ankutty. "A 16-to-40gb/s quarter-rate nrz/pam4 dual-mode transmitter in 14nm cmos . IEEE International Solid-State Circuits Conference, pages60–63,2015.

[10] G. S. Rao, P. Vaseem, A. L. I. Khan, and C. Dist, "Design of Power Efficient Digital Systems Using Adiabatic Techniques," vol. 16, pp. 89– 100.

[11] N. Anuar, Y. Takahashi and T. Sekine, " Adiabatic Logic ver- sus CMOS for Low Power Applications", in ITC-CSCC, 2009.

[12] S. P. S. Kushawaha and T. N. Sasamal, "Modified positive feedback adiabatic logic for ultra low power adder," in *2nd International Conference on Computational Intelligence and Communication Technology, CICT 2016*, Aug. 2016, pp. 378–381, doi: 10.1109/CICT.2016.80.

[13] A. Agrawal, T. K. Gupta, and A. K. Dadoria, "Ultra low power adiabatic logic using diode connected DC biased PFAL logic," *Adv. Electr. Electron. Eng.*, vol. 15, no. 1, pp. 46–54, Mar. 2017, doi: 10.15598/aeee.v15i1.1974.